


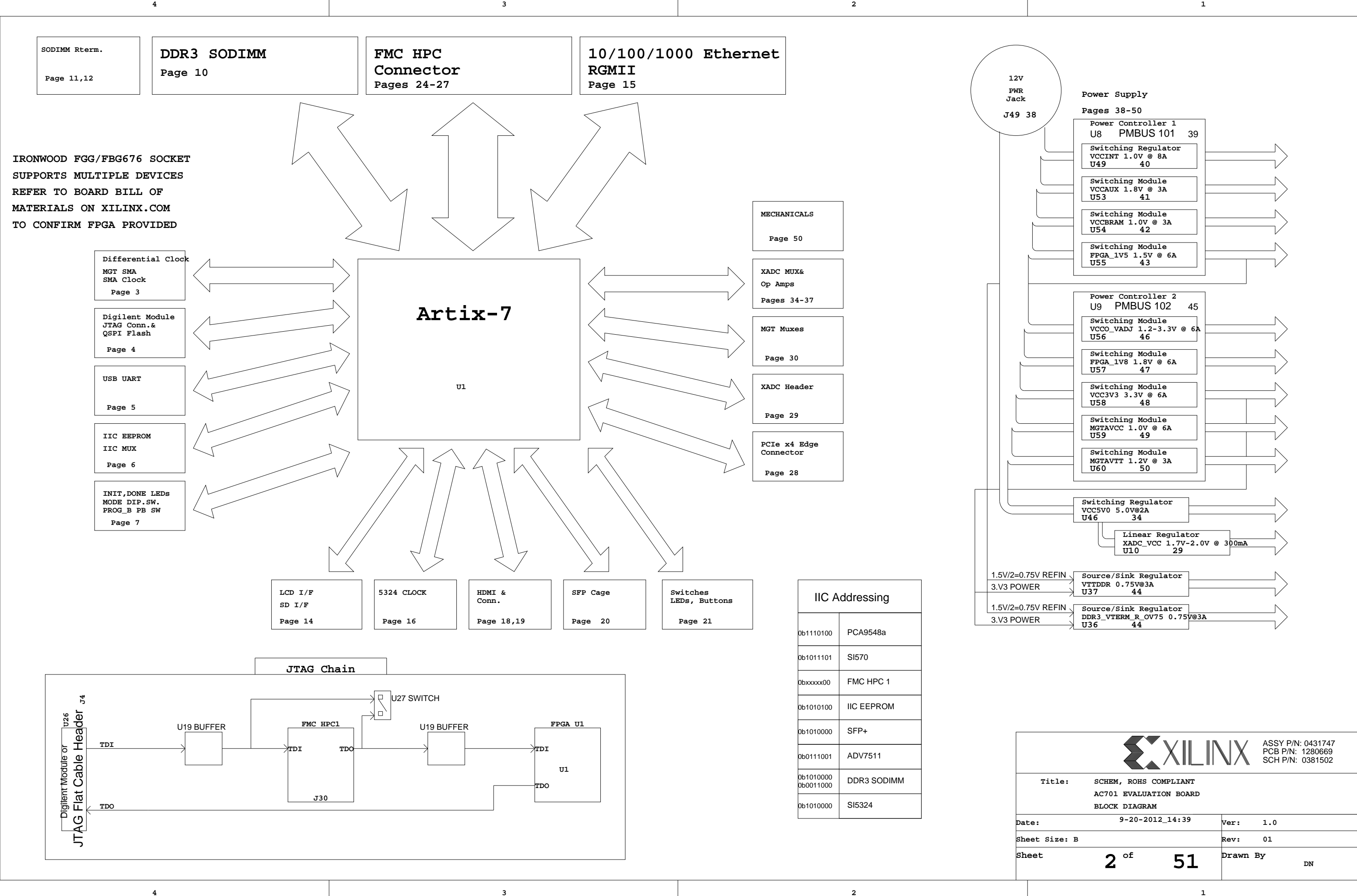
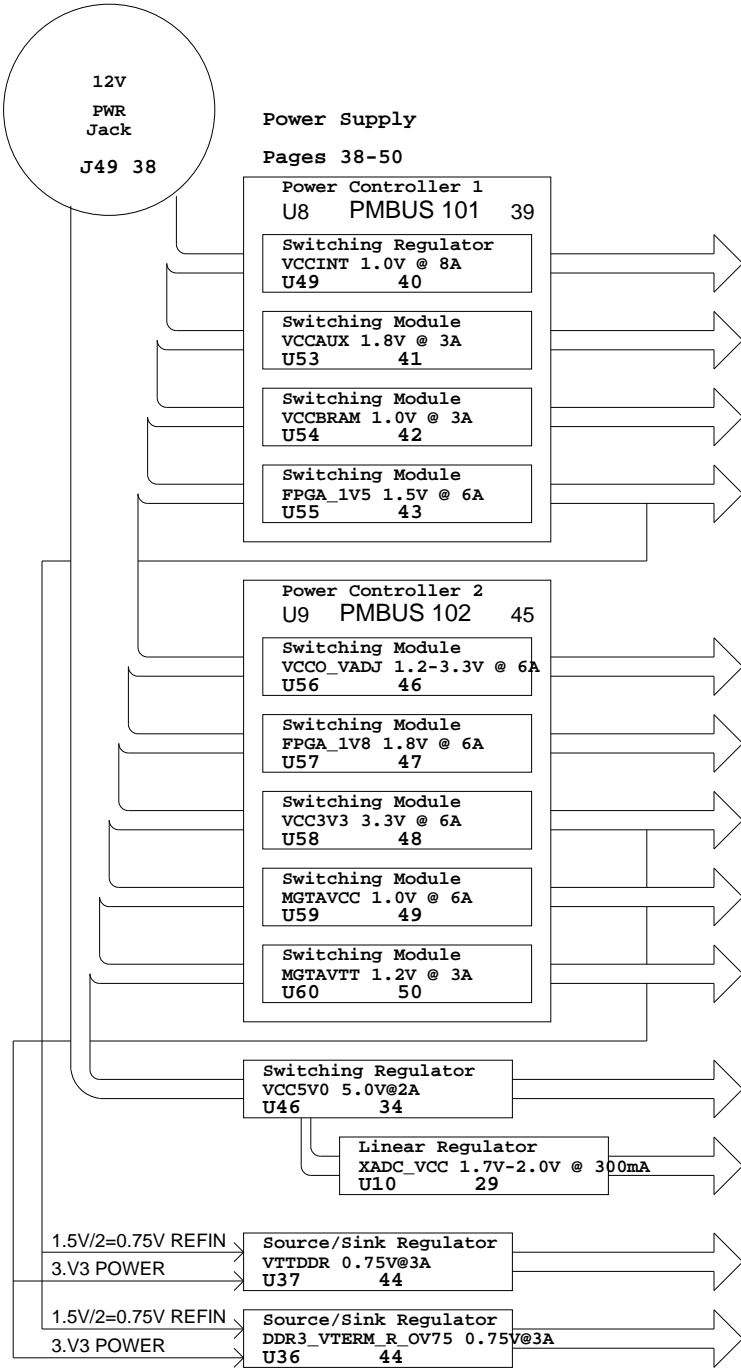


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D	AC701 EVALUATION BOARD HW-A7-AC701 (XC7A200T-FBG676)																						
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C																							
B																							
A			<table><tr><td colspan="2"></td><td colspan="2">ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502</td></tr><tr><td colspan="2">Title:</td><td colspan="2">SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DISCLAIMER</td></tr><tr><td>Date:</td><td>9-20-2012_14:39</td><td>Ver:</td><td>1.0</td></tr><tr><td colspan="2">Sheet Size: B</td><td>Rev:</td><td>01</td></tr><tr><td>Sheet</td><td>1 of 51</td><td>Drawn By</td><td>DN</td></tr></table>			ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502		Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DISCLAIMER		Date:	9-20-2012_14:39	Ver:	1.0	Sheet Size: B		Rev:	01	Sheet	1 of 51	Drawn By	DN
		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502																					
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DISCLAIMER																					
Date:	9-20-2012_14:39	Ver:	1.0																				
Sheet Size: B		Rev:	01																				
Sheet	1 of 51	Drawn By	DN																				
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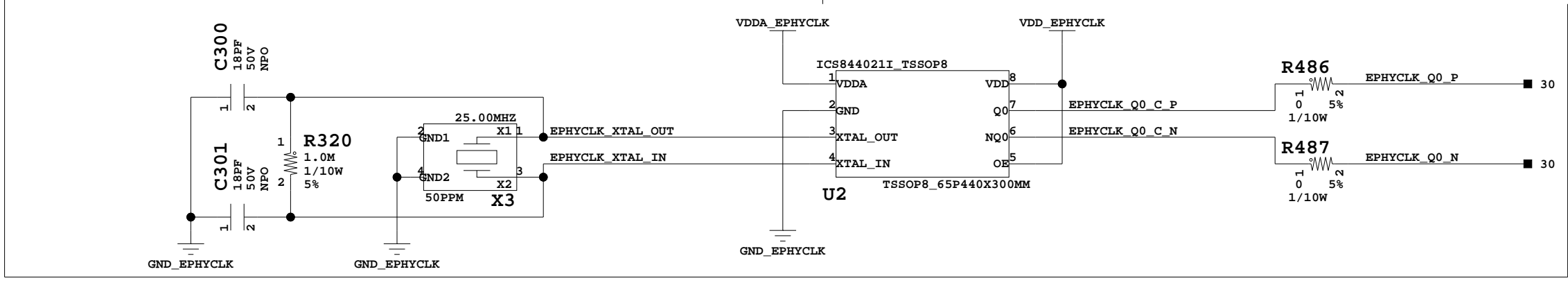
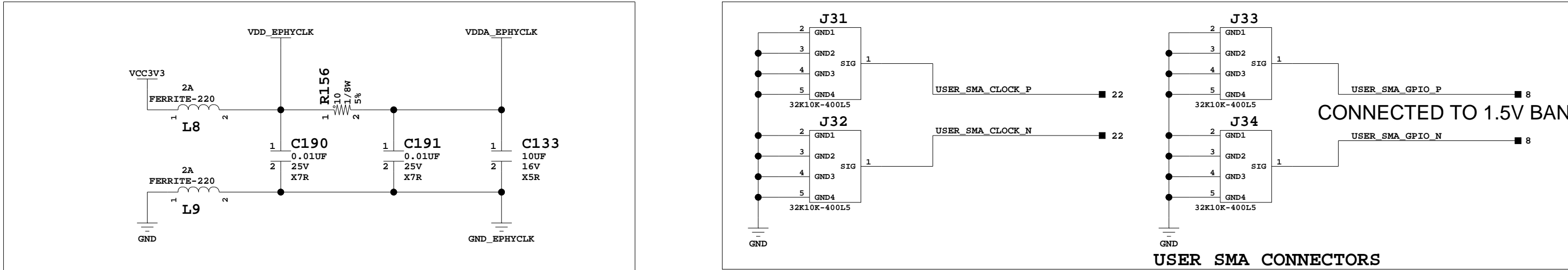
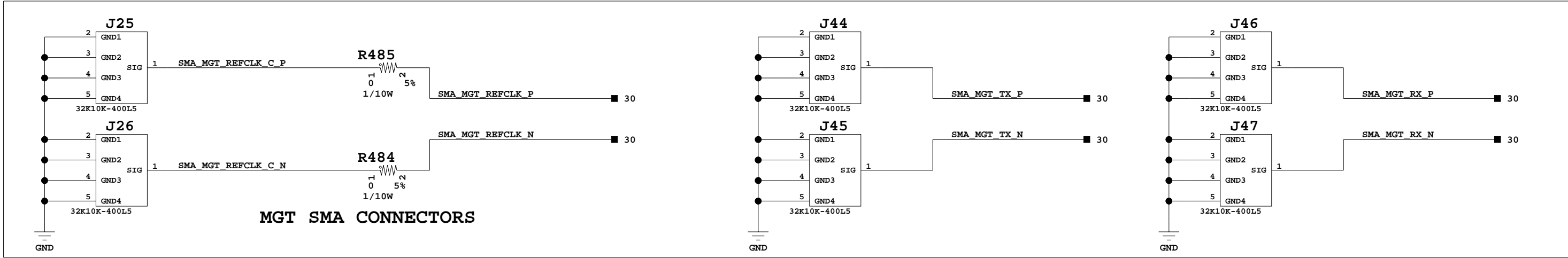
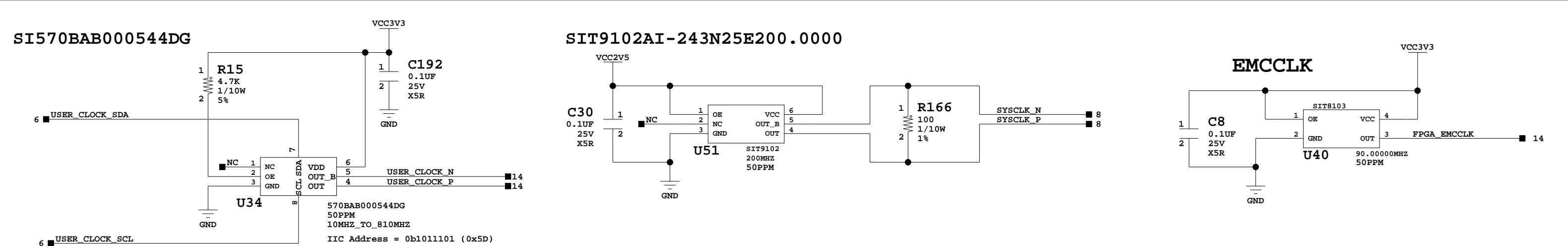


IRONWOOD FGG/FBG676 SOCKET  
SUPPORTS MULTIPLE DEVICES  
REFER TO BOARD BILL OF  
MATERIALS ON XILINX.COM  
TO CONFIRM FPGA PROVIDED



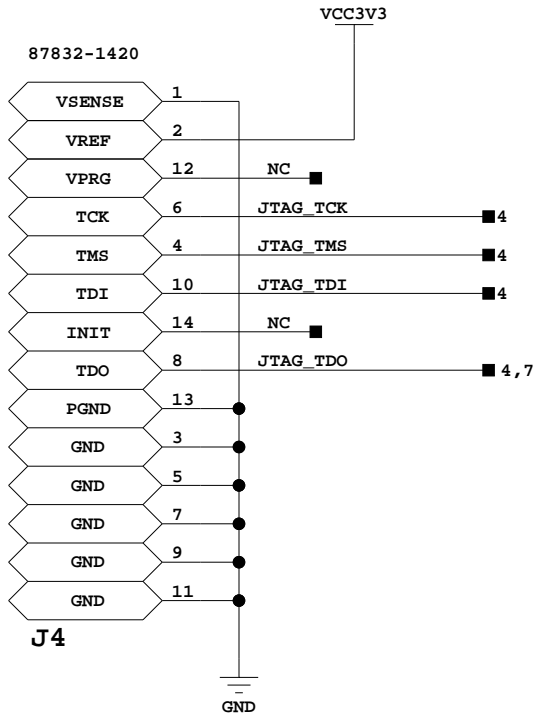
IIC Addressing	
0b1110100	PCA9548a
0b1011101	SI570
0bxxxxx00	FMC HPC 1
0b1010100	IIC EEPROM
0b1010000	SFP+
0b0111001	ADV7511
0b1010000 0b0011000	DDR3 SODIMM
0b1010000	SI5324

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BLOCK DIAGRAM	
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	2 of 51	Drawn By	DN

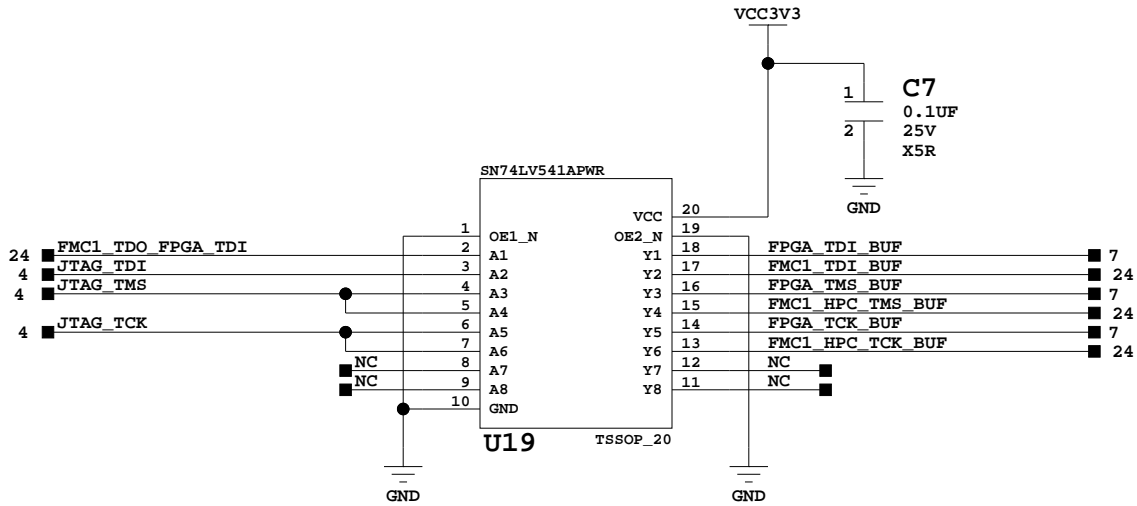
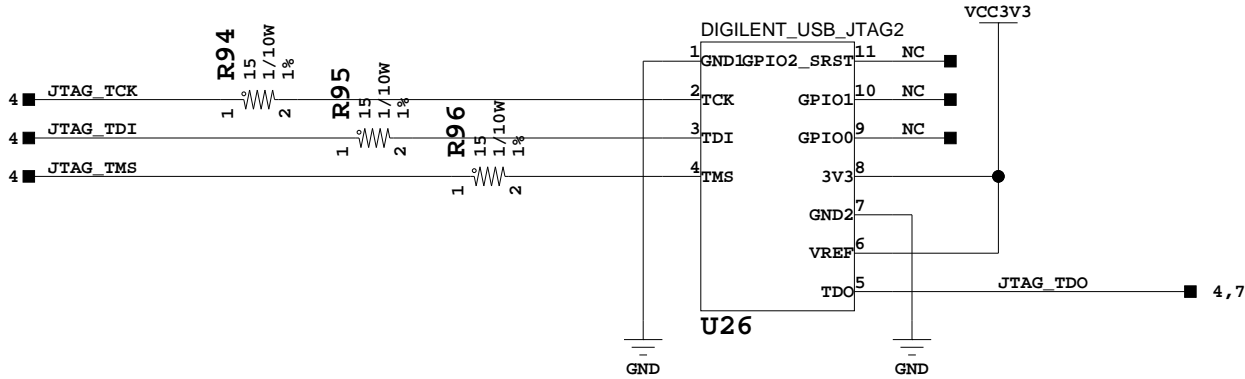


		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD CLOCKS	
Date:	10-9-2012_13:53	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	3 of 51	Drawn By	DN

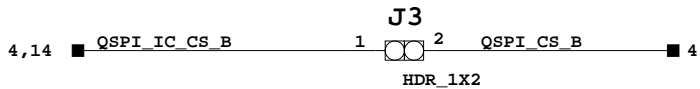
JTAG FLAT-CABLE HEADER



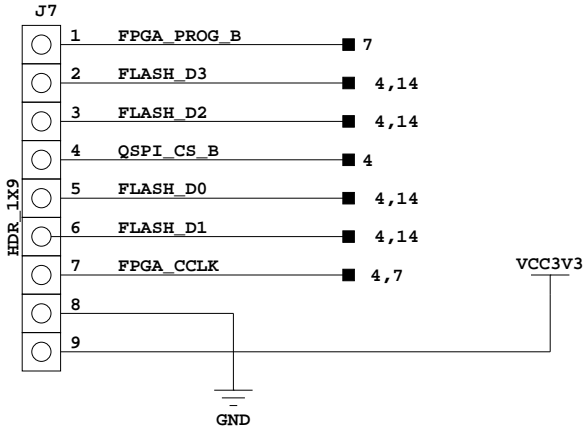
USB JTAG DIGILENT MODULE



ON = SPI DEVICE  
OFF = SPI EXTERNAL



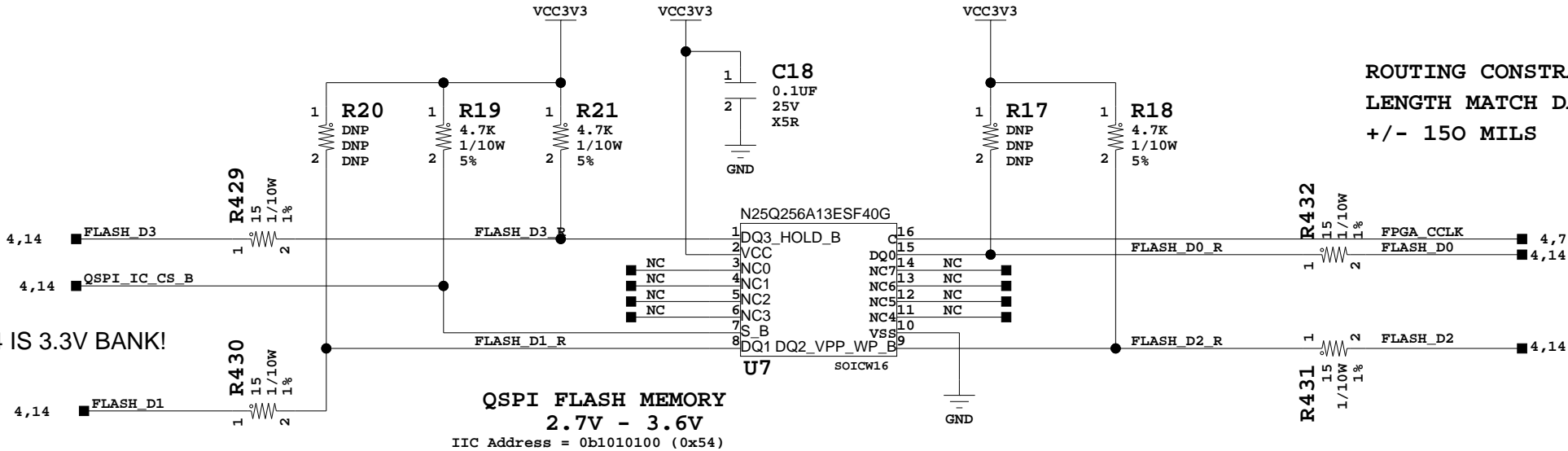
SPI SELECT JUMPER



SPI EXTERNAL  
PROGRAMMING HEADER

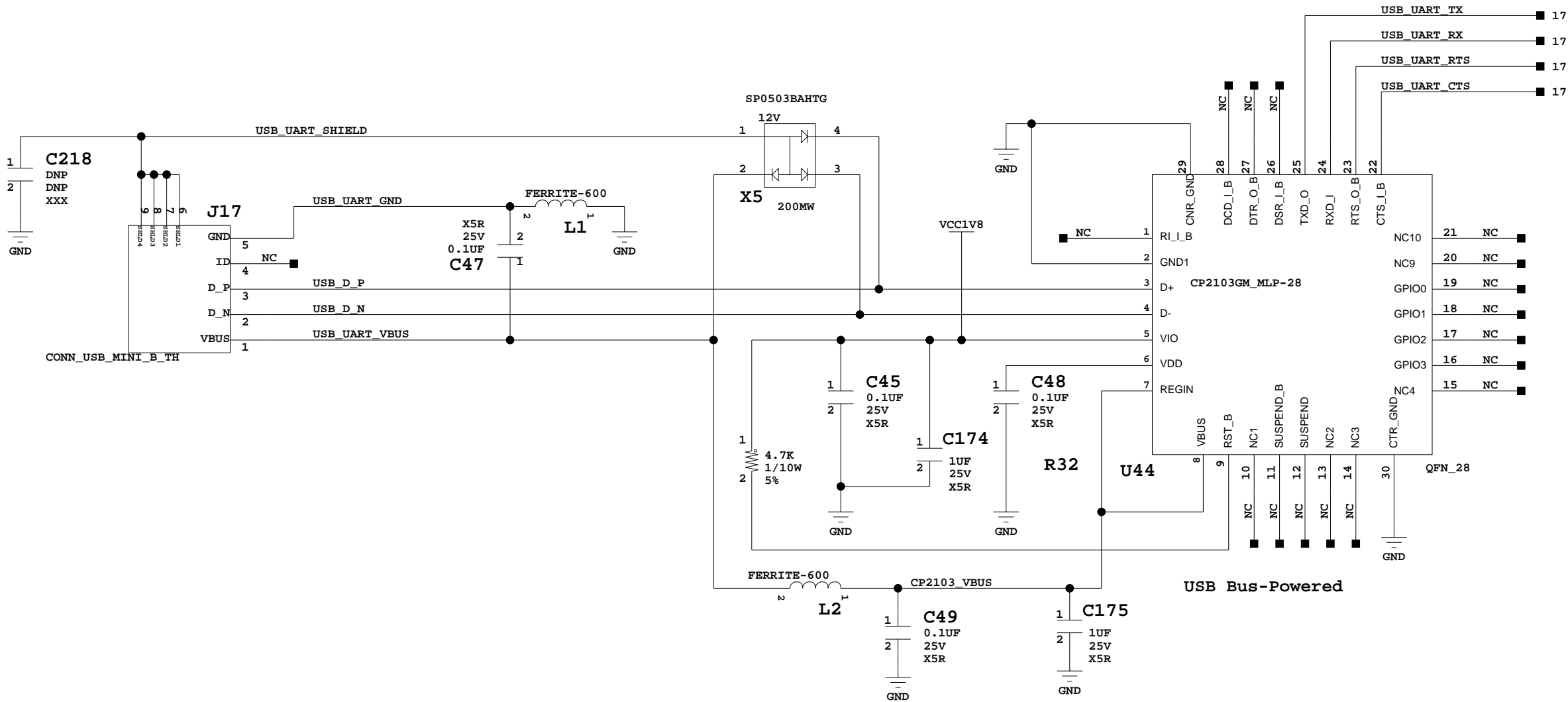
ROUTING CONSTRAINT:  
LENGTH MATCH DATA AND CLOCK  
+/- 150 MILS

PG.14 IS 3.3V BANK!




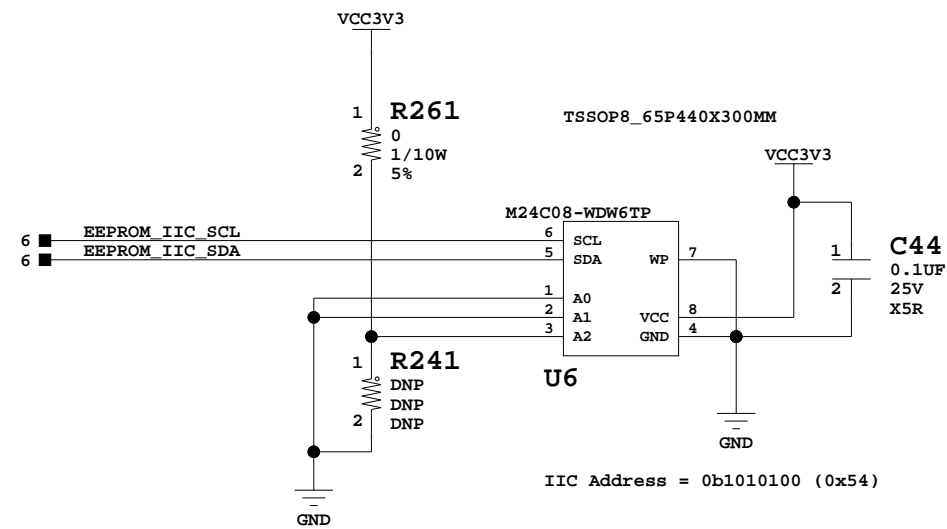
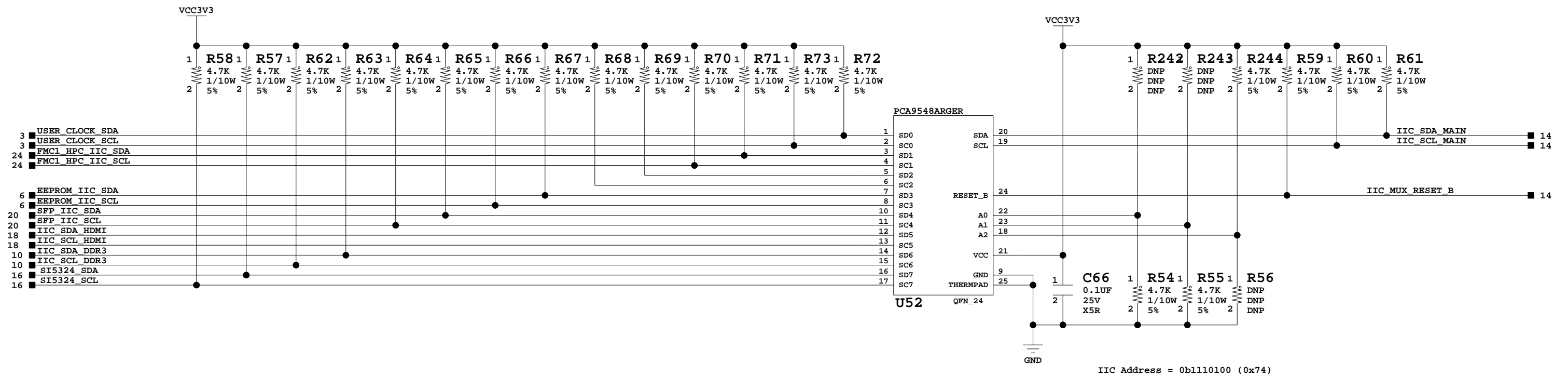
FPGA Configuration Options

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Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD CONFIGURATION	
Date:	9-20-2012_14:39	Ver:	1.0
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USB UART

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD USB-to-UART BRIDGE			
Date: 9-20-2012_14:39		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 5 of 51		Drawn By DN	



## IIC MUX, EEPROM



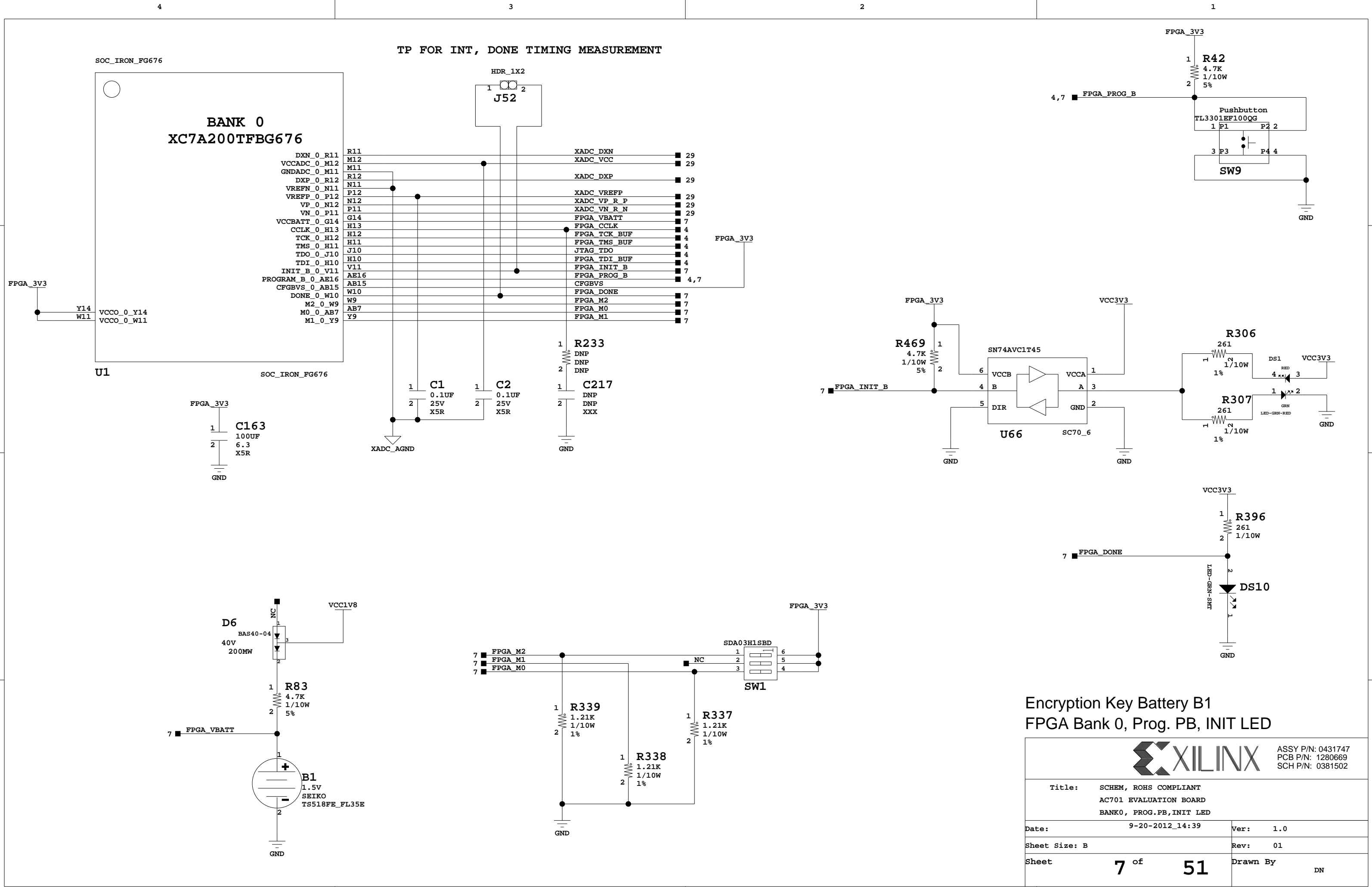
ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
IIC MUX and EEPROM

Date:	9-20-2012_14:39	Ver:	1.0
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Sheet Size: B	Rev: 01
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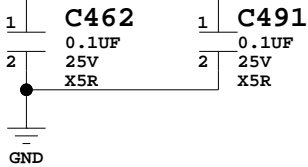


SOC\_IRON\_FG676

BANK 34  
XC7A200TFBG676

IO_0_34_N8	N8	DDR3_RESET_B	10
IO_L1P_T0_34_K3	K3	DDR3_A9	10
IO_L1N_T0_34_J3	J3	DDR3_A1	10
IO_L2P_T0_34_M7	M7	DDR3_A5	10
IO_L2N_T0_34_L7	L7	DDR3_A12	10
IO_L3P_T0_DQS_34_M4	M4	DDR3_A0	10
IO_L3N_T0_DQS_34_L4	L4	DDR3_A3	10
IO_L4P_T0_34_L5	L5	DDR3_A11	10
IO_L4N_T0_34_K5	K5	DDR3_A4	10
IO_L5P_T0_34_N7	N7	DDR3_A10	10
IO_L5N_T0_34_N6	N6	DDR3_A13	10
IO_L6P_T0_34_M6	M6	DDR3_A7	10
IO_L6N_T0_VREF_34_M5	M5		
IO_L7P_T1_34_K1	K1	DDR3_A6	10
IO_L7N_T1_34_J1	J1	DDR3_A2	10
IO_L8P_T1_34_L3	L3	DDR3_A14	10
IO_L8N_T1_34_K2	K2	DDR3_A15	10
IO_L9P_T1_DQS_34_N1	N1	DDR3_BA0	10
IO_L9N_T1_DQS_34_M1	M1	DDR3_BA1	10
IO_L10P_T1_34_H2	H2	DDR3_BA2	10
IO_L10N_T1_34_H1	H1	DDR3_A8	10
IO_L11P_T1_SRCC_34_M2	M2	DDR3_CLK0_P	10
IO_L11N_T1_SRCC_34_L2	L2	DDR3_CLK0_N	10
IO_L12P_T1_MRCC_34_N3	N3	DDR3_CLK1_P	10
IO_L12N_T1_MRCC_34_N2	N2	DDR3_CLK1_N	10
IO_L13P_T2_MRCC_34_R3	R3	SYSCLK_P	3
IO_L13N_T2_MRCC_34_P3	P3	SYSCLK_N	3
IO_L14P_T2_SRCC_34_P4	P4	DDR3_CKE0	10
IO_L14N_T2_SRCC_34_N4	N4	DDR3_CKE1	10
IO_L15P_T2_DQS_34_R1	R1	DDR3_WE_B	10
IO_L15N_T2_DQS_34_P1	P1	DDR3_RAS_B	10
IO_L16P_T2_34_T4	T4	DDR3_CAS_B	10
IO_L16N_T2_34_T3	T3	DDR3_S0_B	10
IO_L17P_T2_34_T2	T2	DDR3_S1_B	10
IO_L17N_T2_34_R2	R2	DDR3_ODT0	10
IO_L18P_T2_34_U2	U2	DDR3_ODT1	10
IO_L18N_T2_34_U1	U1	DDR3_TEMP_EVENT	10
IO_L19P_T3_34_P6	P6	GPIO_SW_N	21
IO_L19N_T3_VREF_34_P5	P5		
IO_L20P_T3_34_T5	T5	GPIO_SW_S	21
IO_L20N_T3_34_R5	R5	GPIO_SW_W	21
IO_L21P_T3_DQS_34_U6	U6	GPIO_SW_C	21
IO_L21N_T3_DQS_34_U5	U5	GPIO_SW_E	21
IO_L22P_T3_34_R8	R8	GPIO_DIP_SW0	21
IO_L22N_T3_34_P8	P8	GPIO_DIP_SW1	21
IO_L23P_T3_34_R7	R7	GPIO_DIP_SW2	21
IO_L23N_T3_34_R6	R6	GPIO_DIP_SW3	21
IO_L24P_T3_34_T8	T8	USER_SMA_GPIO_P	3
IO_L24N_T3_34_T7	T7	USER_SMA_GPIO_N	3
IO_25_34_U4	U4	CPU_RESET	21

VTTVREF



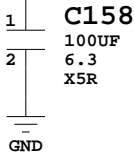
FPGA\_1V5

T6	VCCO_34_T6
P2	VCCO_34_P2
N5	VCCO_34_N5
M8	VCCO_34_M8
L1	VCCO_34_L1
K4	VCCO_34_K4

U1

SOC\_IRON\_FG676

FPGA\_1V5

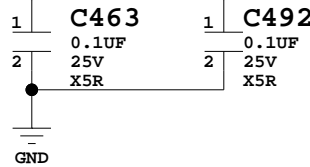


SOC\_IRON\_FG676

BANK 35  
XC7A200TFBG676

IO_0_35_J8	J8	NC	
IO_L1P_T0_AD4P_35_E6	E6	DDR3_D63	10,12
IO_L1N_T0_AD4N_35_D6	D6	DDR3_D62	10,12
IO_L2P_T0_AD12P_35_H8	H8	DDR3_D61	10,12
IO_L2N_T0_AD12N_35_G8	G8	DDR3_D60	10,12
IO_L3P_T0_DQS_AD5P_35_H7	H7	DDR3_DQS7_P	10,12
IO_L3N_T0_DQS_AD5N_35_G7	G7	DDR3_DQS7_N	10,12
IO_L4P_T0_35_F8	F8	DDR3_D59	10,12
IO_L4N_T0_35_F7	F7	DDR3_D58	10,12
IO_L5P_T0_AD13P_35_H6	H6	DDR3_D57	10,12
IO_L5N_T0_AD13N_35_G6	G6	DDR3_D56	10,12
IO_L6P_T0_35_H9	H9	DDR3_DM7	10
IO_L6N_T0_VREF_35_G9	G9		
IO_L7P_T1_AD6P_35_J6	J6	DDR3_D55	10,12
IO_L7N_T1_AD6N_35_J5	J5	DDR3_D54	10,12
IO_L8P_T1_AD14P_35_L8	L8	DDR3_D53	10,12
IO_L8N_T1_AD14N_35_K8	K8	DDR3_D52	10,12
IO_L9P_T1_DQS_AD7P_35_J4	J4	DDR3_DQS6_P	10,12
IO_L9N_T1_DQS_AD7N_35_H4	H4	DDR3_DQS6_N	10,12
IO_L10P_T1_AD15P_35_K7	K7	DDR3_D51	10,12
IO_L10N_T1_AD15N_35_K6	K6	DDR3_D50	10,12
IO_L11P_T1_SRCC_35_G4	G4	DDR3_D49	10,12
IO_L11N_T1_SRCC_35_F4	F4	DDR3_D48	10,12
IO_L12P_T1_MRCC_35_F5	G5	DDR3_DM6	10
IO_L12N_T1_MRCC_35_F5	F5	NC	
IO_L13P_T2_MRCC_35_E5	E5	DDR3_D47	10,12
IO_L13N_T2_MRCC_35_D5	D5	DDR3_D46	10,12
IO_L14P_T2_SRCC_35_D4	D4	DDR3_D45	10,12
IO_L14N_T2_SRCC_35_C4	C4	DDR3_D44	10,12
IO_L15P_T2_DQS_35_B5	B5	DDR3_DQS5_P	10,12
IO_L15N_T2_DQS_35_A5	A5	DDR3_DQS5_N	10,12
IO_L16P_T2_35_B4	B4	DDR3_D43	10,12
IO_L16N_T2_35_A4	A4	DDR3_D42	10,12
IO_L17P_T2_35_D3	D3	DDR3_D41	10,12
IO_L17N_T2_35_C3	C3	DDR3_D40	10,12
IO_L18P_T2_35_F3	F3	DDR3_DM5	10
IO_L18N_T2_35_E3	E3	NC	
IO_L19P_T3_35_C2	C2	DDR3_D39	10,12
IO_L19N_T3_VREF_35_B2	B2		
IO_L20P_T3_35_A3	A3	DDR3_D38	10,12
IO_L20N_T3_35_A2	A2	DDR3_D37	10,12
IO_L21P_T3_DQS_35_C1	C1	DDR3_DQS4_P	10,12
IO_L21N_T3_DQS_35_B1	B1	DDR3_DQS4_N	10,12
IO_L22P_T3_35_F2	F2	DDR3_D36	10,12
IO_L22N_T3_35_E2	E2	DDR3_D35	10,12
IO_L23P_T3_35_E1	E1	DDR3_D34	10,12
IO_L23N_T3_35_D1	D1	DDR3_D33	10,12
IO_L24P_T3_35_G2	G2	DDR3_D32	10,12
IO_L24N_T3_35_G1	G1	DDR3_DM4	10
IO_25_35_H3	H3	NC	

VTTVREF



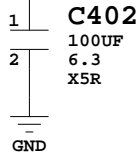
FPGA\_1V5

J7	VCCO_35_J7
G3	VCCO_35_G3
F6	VCCO_35_F6
D2	VCCO_35_D2
C5	VCCO_35_C5
A1	VCCO_35_A1

U1

SOC\_IRON\_FG676

FPGA\_1V5



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
BANKS34,35 DDR3 SODIMM IF

Date: 9-20-2012\_14:39 Ver: 1.0

Sheet Size: B Rev: 01

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J1

9,11	DDR3_D4	129	DDR3_D32	8,12
9,11	DDR3_D0	130	DDR3_D36	8,12
9,11	DDR3_D5	131	DDR3_D33	8,12
9,11	DDR3_D1	132	DDR3_D37	8,12
9,11	DDR3_DM0	136	DDR3_DM4	8
9	DDR3_DQ0	135	DDR3_DQ04_N	8
9,11	DDR3_DQ0_N	137	DDR3_DQ04_P	8,12
9,11	DDR3_D6	140	DDR3_D38	8,12
9,11	DDR3_D7	141	DDR3_D34	8,12
9,11	DDR3_D2	142	DDR3_D39	8,12
9,11	DDR3_D3	143	DDR3_D35	8,12
9,11	DDR3_D12	146	DDR3_D44	8,12
9,11	DDR3_D13	147	DDR3_D40	8,12
9,11	DDR3_D8	148	DDR3_D45	8,12
9,11	DDR3_D9	149	DDR3_D41	8,12
9	DDR3_DM1	153	DDR3_DM5	8
9,11	DDR3_DQ01_N	152	DDR3_DQ05_N	8,12
9,11	DDR3_DQ01_P	154	DDR3_DQ05_P	8,12
9,11	DDR3_D10	157	DDR3_D42	8,12
9,11	DDR3_D14	158	DDR3_D46	8,12
9,11	DDR3_D11	159	DDR3_D43	8,12
9,11	DDR3_D15	160	DDR3_D47	8,12
9,11	DDR3_D16	163	DDR3_D48	8,12
9,11	DDR3_D20	164	DDR3_D52	8,12
9,11	DDR3_D17	165	DDR3_D49	8,12
9,11	DDR3_D21	166	DDR3_D53	8,12
9,11	DDR3_DQ02_N	169	DDR3_DQ06_N	8,12
9,11	DDR3_DQ02_P	171	DDR3_DQ06_P	8,12
9	DDR3_DM2	170	DDR3_DM6	8
9,11	DDR3_D18	175	DDR3_D50	8,12
9,11	DDR3_D22	174	DDR3_D54	8,12
9,11	DDR3_D19	177	DDR3_D51	8,12
9,11	DDR3_D23	176	DDR3_D55	8,12
9,11	DDR3_D24	181	DDR3_D56	8,12
9,11	DDR3_D28	180	DDR3_D60	8,12
9,11	DDR3_D25	183	DDR3_D57	8,12
9,11	DDR3_D29	182	DDR3_D61	8,12
9	DDR3_DM3	187	DDR3_DM7	8
9,11	DDR3_DQ03_N	186	DDR3_DQ07_N	8,12
9,11	DDR3_DQ03_P	188	DDR3_DQ07_P	8,12
9,11	DDR3_D26	191	DDR3_D58	8,12
9,11	DDR3_D30	193	DDR3_D59	8,12
9,11	DDR3_D27	192	DDR3_D62	8,12
9,11	DDR3_D31	194	DDR3_D63	8,12

Silkscreen:  
"DDR3 SO-DIMM"

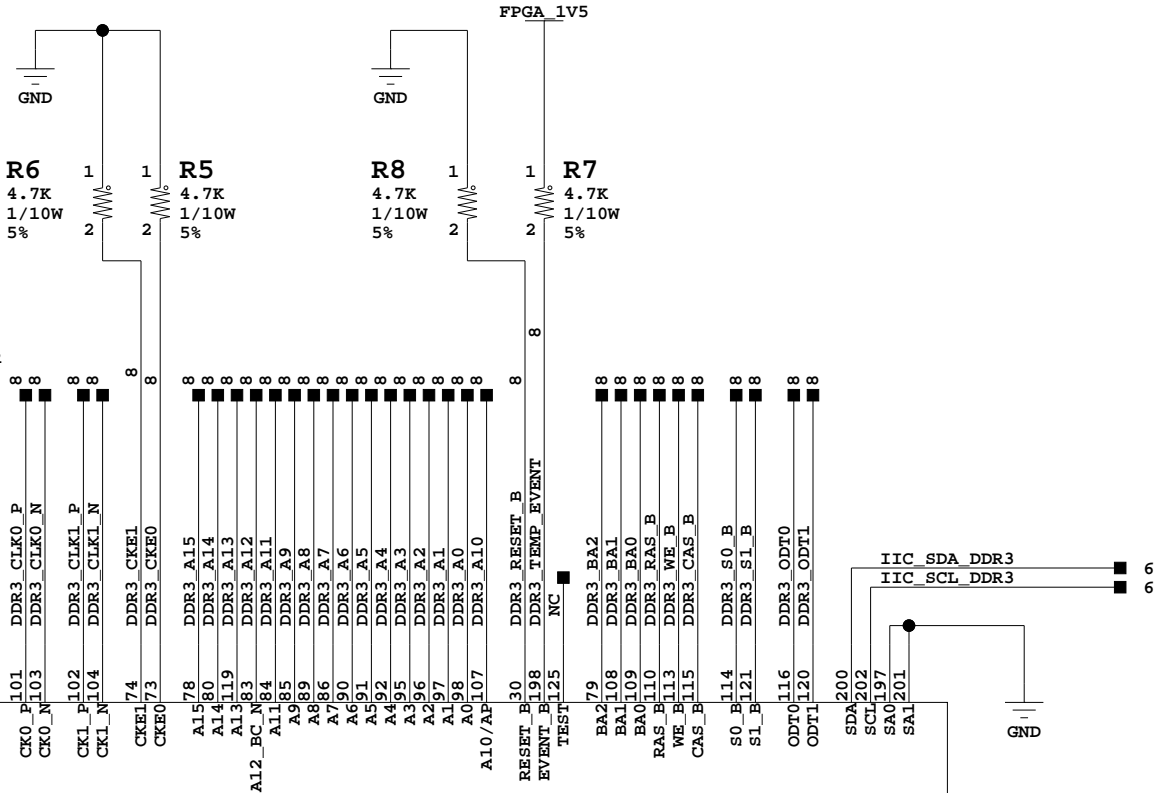
DDR3\_SO-DIMM\_SHIELDED

FPGA\_1V5

VTTVREF

VCC3V3

VTTDDR



### DDR3 SO-DIMM

IIC Address = 0b1010000 (0x50)  
0b0010000 (0x18)



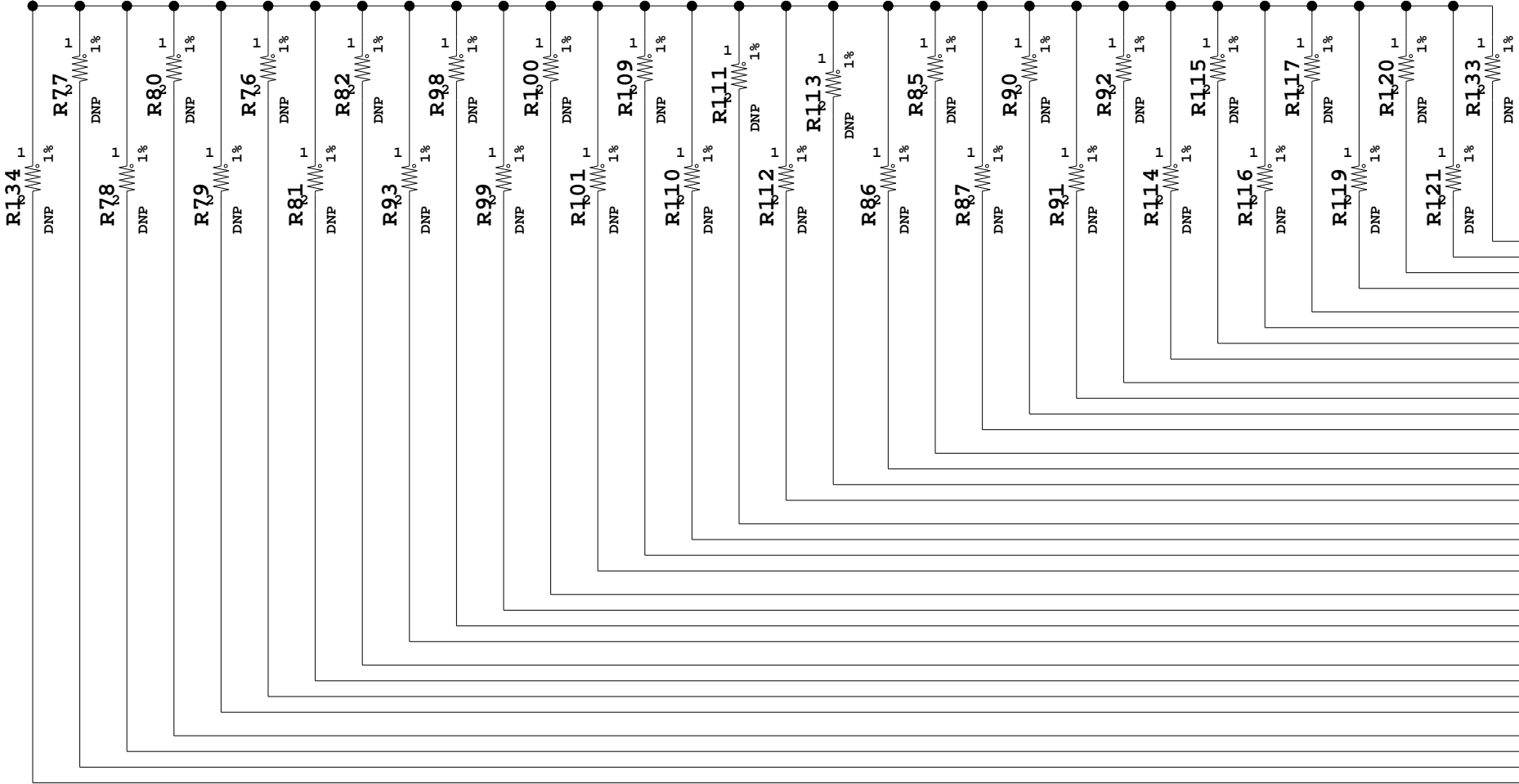
ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM SOCKET J1	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 10 of 51	Drawn By DN

# DDR3 SODIMM J1 MEMORY TERMINATION RESISTORS

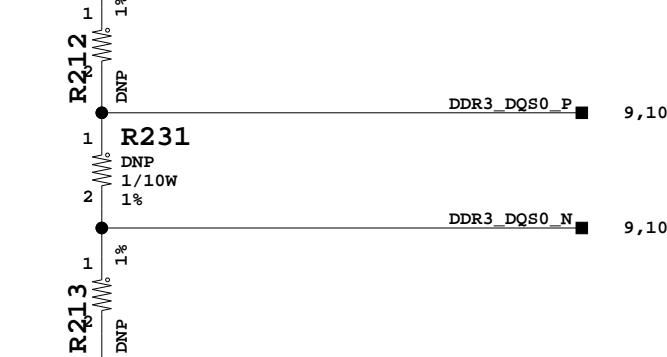
ALL R's ARE DNP  
PLACE AT FPGA

DDR3\_VTERM\_R\_0V75

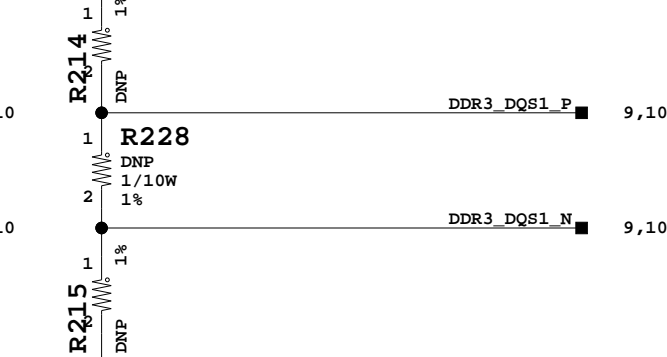


DDR3_D31	9,10
DDR3_D30	9,10
DDR3_D29	9,10
DDR3_D28	9,10
DDR3_D27	9,10
DDR3_D26	9,10
DDR3_D25	9,10
DDR3_D24	9,10
DDR3_D23	9,10
DDR3_D22	9,10
DDR3_D21	9,10
DDR3_D20	9,10
DDR3_D19	9,10
DDR3_D18	9,10
DDR3_D17	9,10
DDR3_D16	9,10
DDR3_D15	9,10
DDR3_D14	9,10
DDR3_D13	9,10
DDR3_D12	9,10
DDR3_D11	9,10
DDR3_D10	9,10
DDR3_D9	9,10
DDR3_D8	9,10
DDR3_D7	9,10
DDR3_D6	9,10
DDR3_D5	9,10
DDR3_D4	9,10
DDR3_D3	9,10
DDR3_D2	9,10
DDR3_D1	9,10
DDR3_D0	9,10

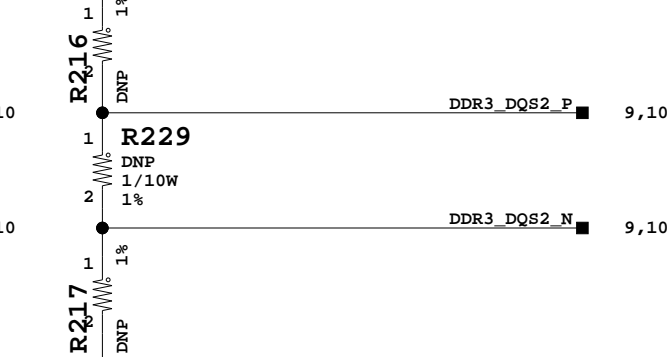
DDR3\_VTERM\_R\_0V75



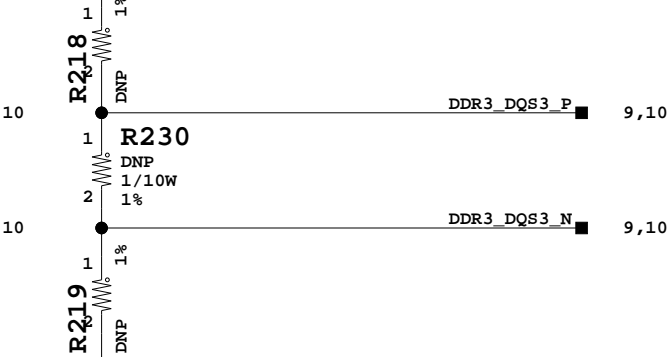
DDR3\_VTERM\_R\_0V75



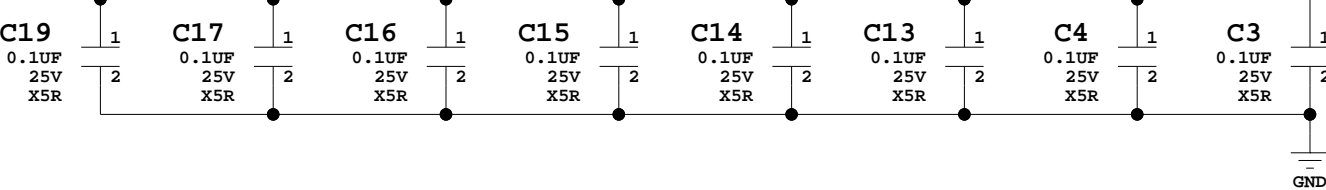
DDR3\_VTERM\_R\_0V75



DDR3\_VTERM\_R\_0V75



DDR3\_VTERM\_R\_0V75



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
DDR3 SODIMM TERM. RESISTORS

Date: 9-20-2012\_14:39 Ver: 1.0

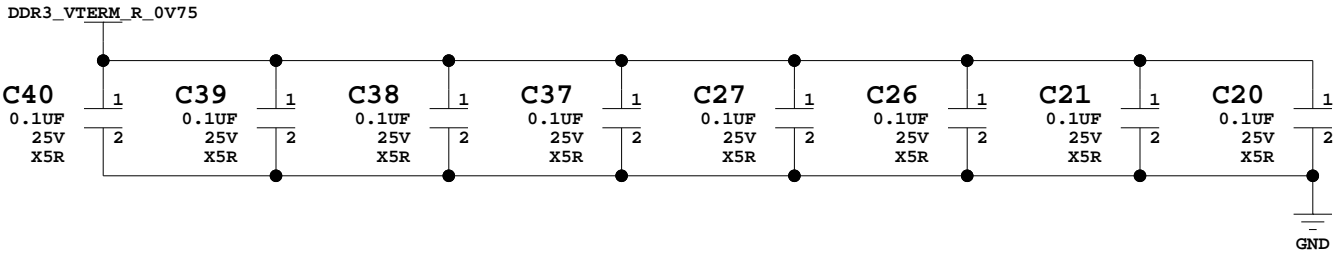
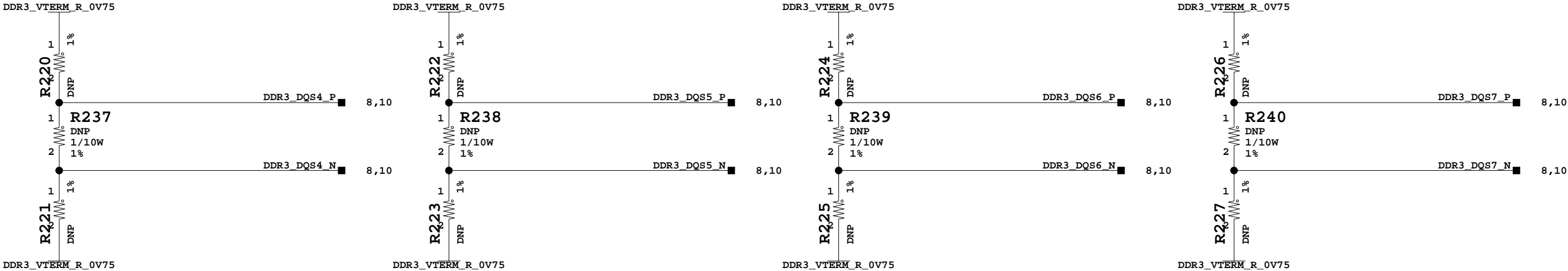
Sheet Size: B Rev: 01

Sheet 11 of 51 Drawn By DN

# DDR3 SODIMM J1 MEMORY TERMINATION RESISTORS

ALL R's ARE DNP  
PLACE AT FPGA

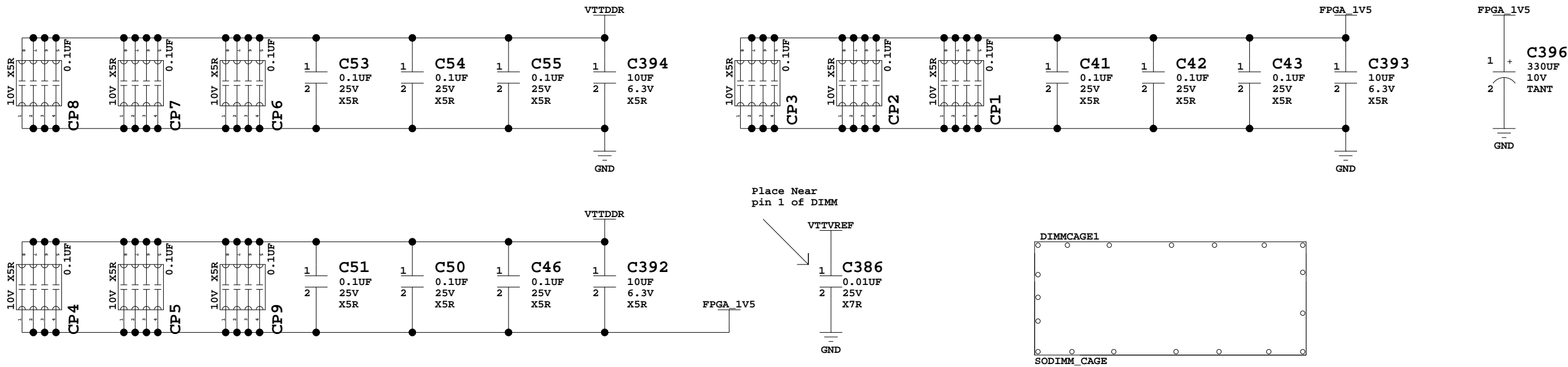
- DDR3\_D63 8,10
- DDR3\_D62 8,10
- DDR3\_D61 8,10
- DDR3\_D60 8,10
- DDR3\_D59 8,10
- DDR3\_D58 8,10
- DDR3\_D57 8,10
- DDR3\_D56 8,10
- DDR3\_D55 8,10
- DDR3\_D54 8,10
- DDR3\_D53 8,10
- DDR3\_D52 8,10
- DDR3\_D51 8,10
- DDR3\_D50 8,10
- DDR3\_D49 8,10
- DDR3\_D48 8,10
- DDR3\_D47 8,10
- DDR3\_D46 8,10
- DDR3\_D45 8,10
- DDR3\_D44 8,10
- DDR3\_D43 8,10
- DDR3\_D42 8,10
- DDR3\_D41 8,10
- DDR3\_D40 8,10
- DDR3\_D39 8,10
- DDR3\_D38 8,10
- DDR3\_D37 8,10
- DDR3\_D36 8,10
- DDR3\_D35 8,10
- DDR3\_D34 8,10
- DDR3\_D33 8,10
- DDR3\_D32 8,10



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM TERM. RESISTORS	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 12 of 51	Drawn By DN

# DDR3 SODIMM J1 MEMORY DECOUPLING CAPACITORS



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
DDR3 SODIMM DECOUPLING

Date: 9-20-2012\_14:39 Ver: 1.0

Sheet Size: B Rev: 01

Sheet 13 of 51 Drawn By DN

BANK 14  
XC7A200TFBG676

IO_0_14_M19	M19	SI5324_INT_ALM_B	16
IO_L1P_T0_D00_MOSI_14_R14	R14	FLASH_D0	4
IO_L1N_T0_D01_DIN_14_R15	R15	FLASH_D1	4
IO_L2P_T0_D02_14_P14	P14	FLASH_D2	4
IO_L2N_T0_D03_14_N14	N14	FLASH_D3	4
IO_L3P_T0_DQS_PUDC_B_14_P15	P15	CTRL2_PWRGOOD	24, 39, 45
IO_L3N_T0_DQS_EMCCLK_14_P16	P16	FPGA_EMCCLK	3
IO_L4P_T0_D04_14_N16	N16	FMC1_HPC_PRSENT_M2C_B	24, 26
IO_L4N_T0_D05_14_N17	N17	FMC1_HPC_PG_M2C	25
IO_L5P_T0_D06_14_R16	R16	FMC_VADJ_ON_B	45
IO_L5N_T0_D07_14_R17	R17	IIC_MUX_RESET_B	6
IO_L6P_T0_FCS_B_14_P18	P18	QSPI_IC_CS_B	4
IO_L6N_T0_D08_VREF_14_N18	N18	IIC_SCL_MAIN	6
IO_L7P_T1_D09_14_K25	K25	IIC_SDA_MAIN	6
IO_L7N_T1_D10_14_K26	K26	PCIE_WAKE_B	28
IO_L8P_T1_D11_14_M20	M20	PCIE_PERST	28
IO_L8N_T1_D12_14_L20	L20	LCD_E_LS	14
IO_L9P_T1_DQS_14_L24	L24	LCD_RW_LS	14
IO_L9N_T1_DQS_D13_14_L25	L25	LCD_DB4_LS	14
IO_L10P_T1_D14_14_M24	M24	LCD_DB5_LS	14
IO_L10N_T1_D15_14_M25	M25	LCD_DB6_LS	14
IO_L11P_T1_SRCC_14_L22	L22	LCD_DB7_LS	14
IO_L11N_T1_SRCC_14_L23	L23	LCD_RS_LS	14
IO_L12P_T1_MRCC_14_M21	M21	USER_CLOCK_P	3
IO_L12N_T1_MRCC_14_M22	M22	USER_CLOCK_N	3
IO_L13P_T2_MRCC_14_N21	N21	ROTARY_PUSH	21
IO_L13N_T2_MRCC_14_N22	N22	ROTARY_INCA	21
IO_L14P_T2_SRCC_14_P20	P20	ROTARY_INCB	21
IO_L14N_T2_SRCC_14_P21	P21	SDIO_CD_DAT3	14
IO_L15P_T2_DQS_RDWR_B_14_N23	N23	SDIO_CMD	14
IO_L15N_T2_DQSDOUT_CSOB_14_N24	N24	SDIO_CLK	14
IO_L16P_T2_CSI_B_14_P19	P19	SDIO_DAT0	14
IO_L16N_T2_A15_D31_14_N19	N19	SDIO_DAT1	14
IO_L17P_T2_A14_D30_14_P23	P23	SDIO_DAT2	14
IO_L17N_T2_A13_D29_14_P24	P24	SDIO_SDDDET	14
IO_L18P_T2_A12_D28_14_R20	R20	SDIO_SDWP	14
IO_L18N_T2_A11_D27_14_R21	R21	PMBUS_CLK_LS	14
IO_L19P_T3_A10_D26_14_R25	R25	PMBUS_DATA_LS	14
IO_L19N_T3_A09_D25_VREF_14_P25	P25	PMBUS_CTRL_LS	14
IO_L20P_T3_A08_D24_14_N26	N26	PMBUS_ALERT_LS	14
IO_L20N_T3_A07_D23_14_M26	M26	GPIO_LED_0	21
IO_L21P_T3_DQS_14_T24	T24	GPIO_LED_1	21
IO_L21N_T3_DQS_A06_D22_14_T25	T25	GPIO_LED_2	21
IO_L22P_T3_A05_D21_14_R26	R26	GPIO_LED_3	21
IO_L22N_T3_A04_D20_14_P26	P26	PMOD_0	21
IO_L23P_T3_A03_D19_14_T22	T22	PMOD_1	21
IO_L23N_T3_A02_D18_14_R22	R22	PMOD_2	21
IO_L24P_T3_A01_D17_14_T23	T23	PMOD_3	21
IO_L24N_T3_A00_D16_14_R23	R23	SFP_LOS	20
IO_25_14_R18	R18	SFP_TX_DISABLE	20

FPGA\_3V3

R19 VCCO\_14\_R19  
P22 VCCO\_14\_P22  
N25 VCCO\_14\_N25  
N15 VCCO\_14\_N15  
L21 VCCO\_14\_L21  
K24 VCCO\_14\_K24

U1

SOC\_IRON\_FG676

FPGA\_3V3

C155  
100UF  
6.3  
X5R

GND

14 SDIO\_CD\_DAT3  
14 SDIO\_CMD  
  
14 SDIO\_CLK  
  
14 SDIO\_DAT0  
14 SDIO\_DAT1  
14 SDIO\_DAT2  
  
14 SDIO\_SDDDET  
14 SDIO\_SDWP

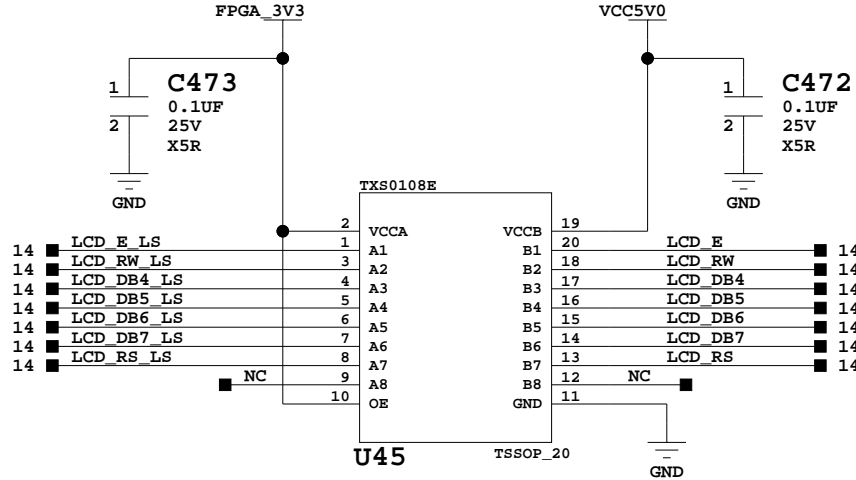
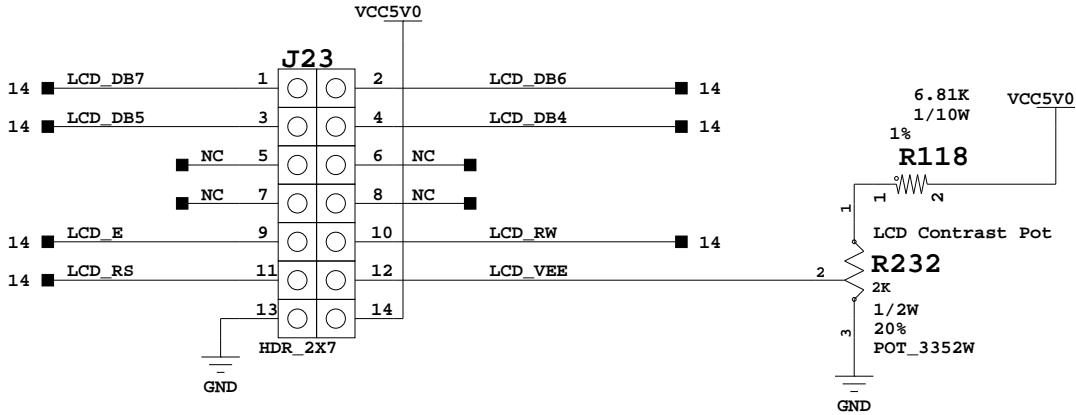
R325 51.1K  
R322 51.1K  
R321 51.1K  
R318 51.1K  
R324 51.1K  
R317 51.1K  
C52 0.1UF  
25V  
X5R

67840-8001  
1 CD\_DAT3  
2 CMD  
3 VSS1  
4 VDD  
5 CLK  
6 VSS2  
7 DAT0  
8 DAT1  
9 DAT2  
10 DETECT  
11 PROTECT  
12 DETECT\_PROTECT

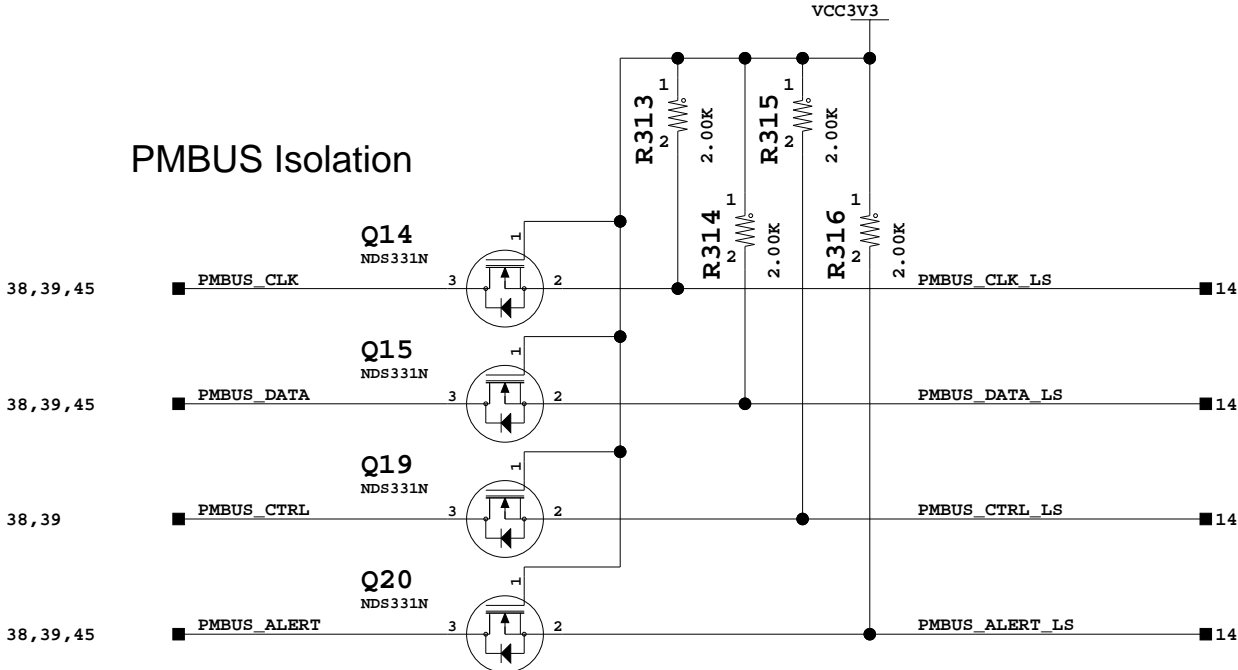
IOGND2  
IOGND1  
GNDTAB4  
GNDTAB3  
GNDTAB2  
GNDTAB1

U29

PWRCTL1\_VCC4B\_PG  
CTRL2\_PWRGOOD from TI controller U9  
indicates both VCC3V3 and VCCO\_VADJ  
FMC power rails are OK



PMBUS Isolation



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
GPIO BANK14, SD SOCKET, LCD IF

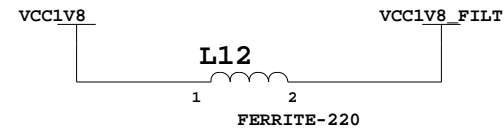
Date: 9-20-2012\_14:39 Ver: 1.0

Sheet Size: B Rev: 01

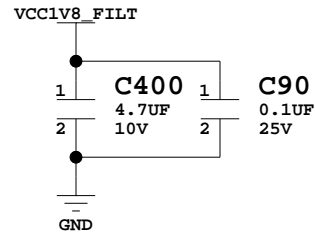
Sheet 14 of 51 Drawn By DN

CONFIGURATION MAPPING			
PIN	SETTING	CONFIGURATION	
CONFIG0	VCCO_MIO1	PHYAD[1]=1	PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2	GND	ENA_XC=0	PHYAD[4]=0
	EPHY_LED0	ENA_XC=0	PHYAD[4]=1
CONFIG3	VCCO_MIO1	ENA_XC=1	PHYAD[4]=1
	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=0	RGMII_RX=1
	EPHY_LED1	RGMII_TX=1	RGMII_RX=0
		VCCO_MIO1	RGMII_TX=1
		RGMII_RX=1	

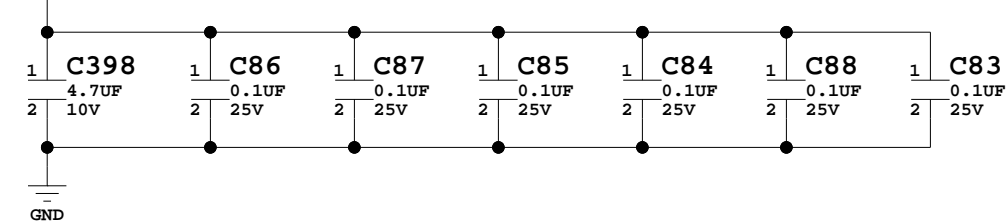
GEM / MDIO - POWER & DECOUPLING



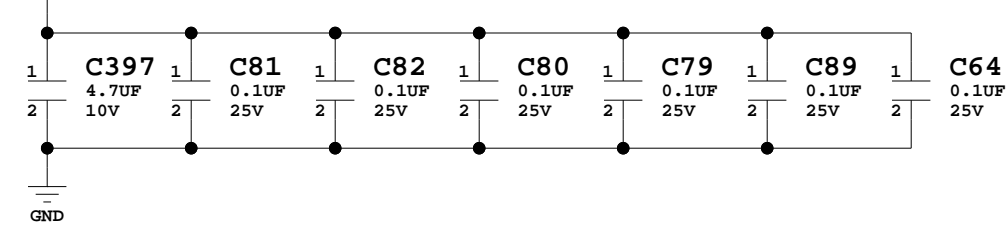
MAGNETICS / RJ45



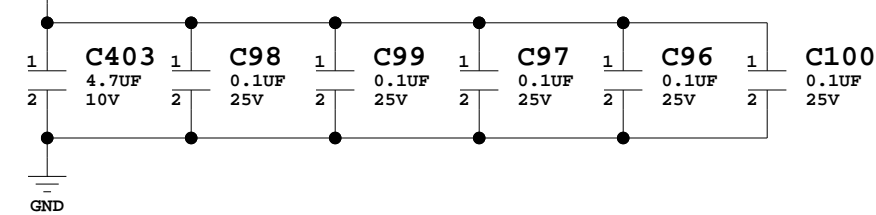
AVDDX, AVDDR, AVDDC



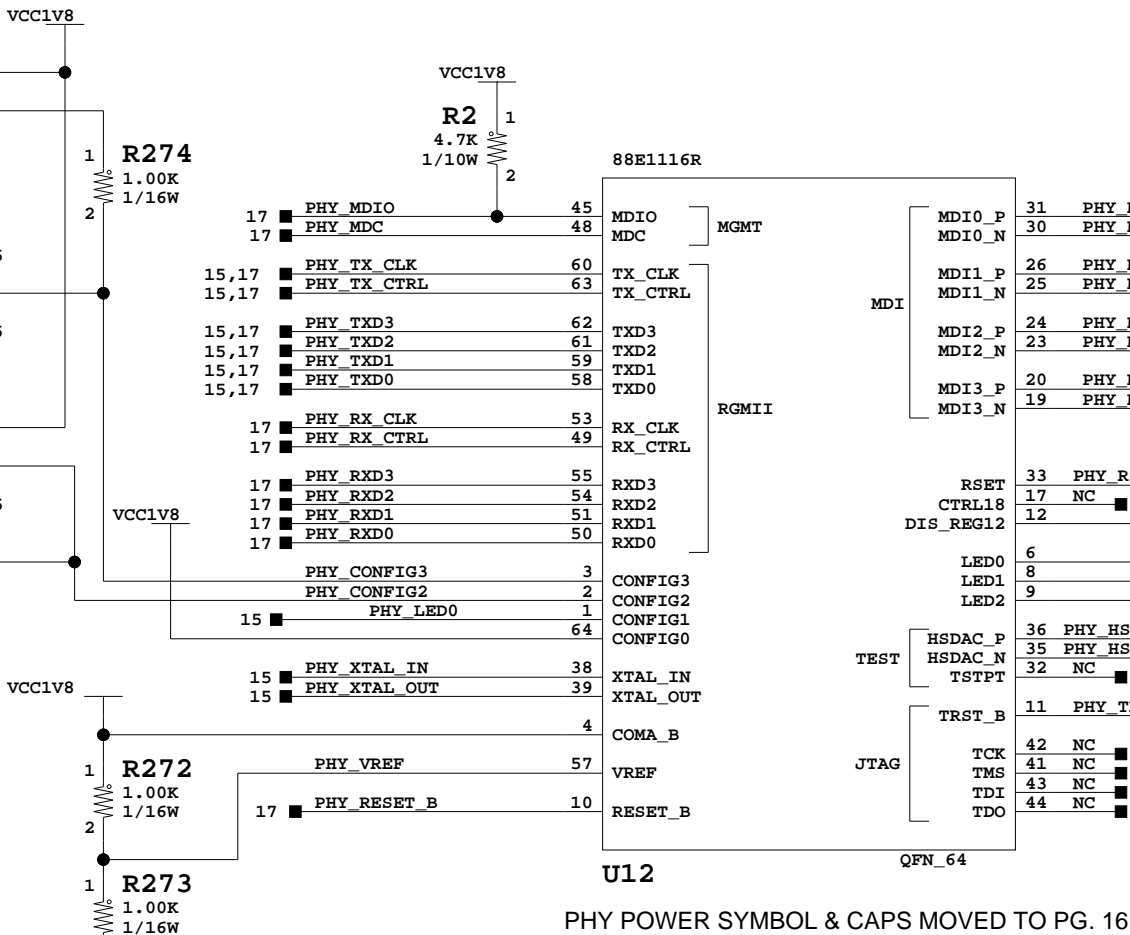
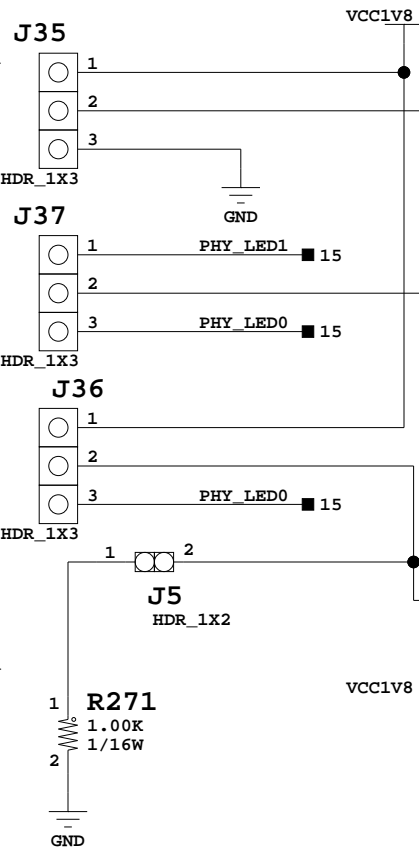
AVDD



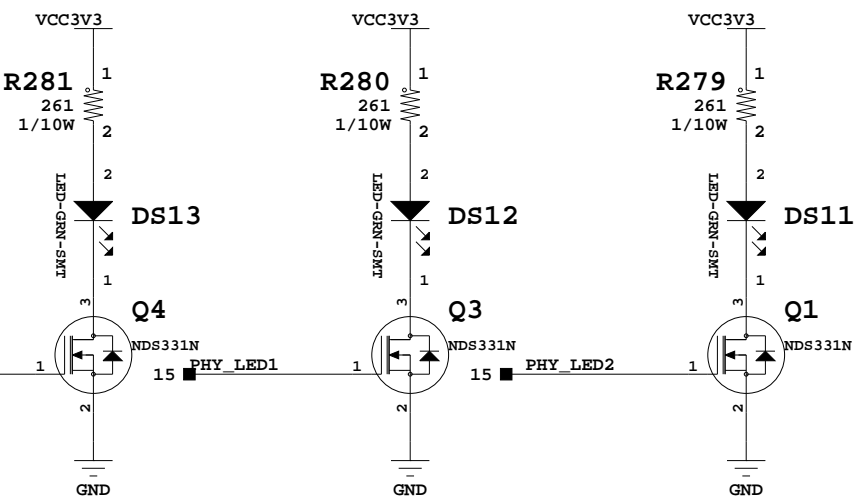
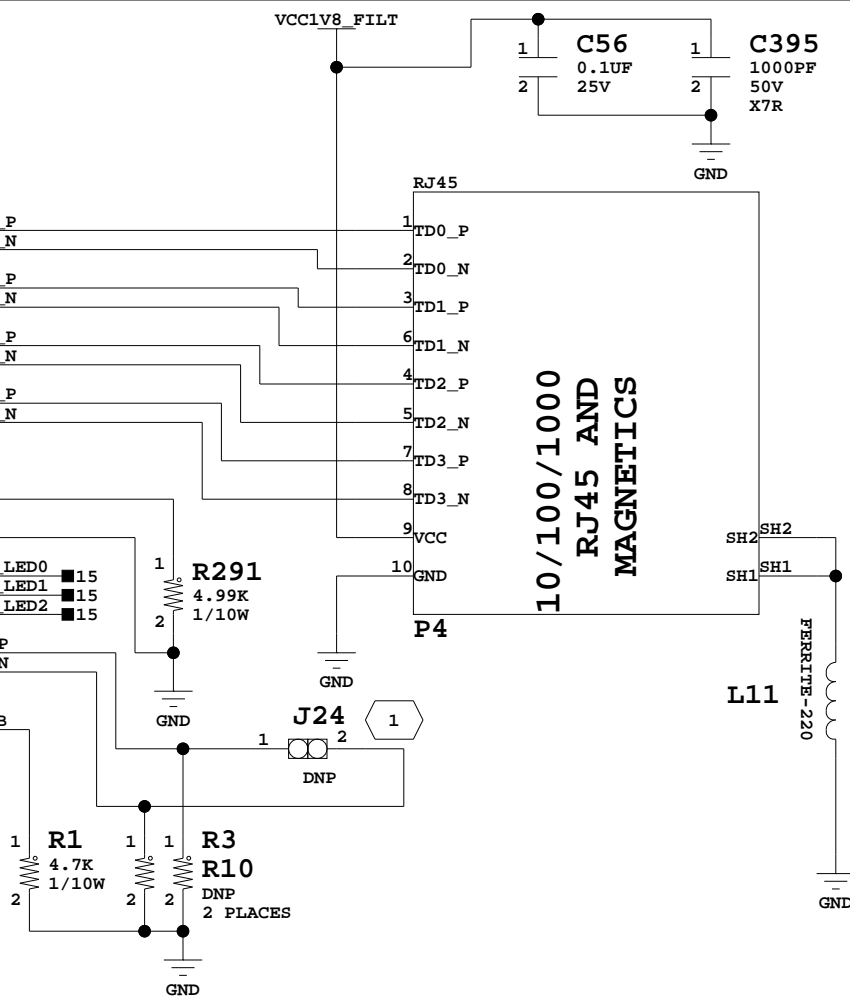
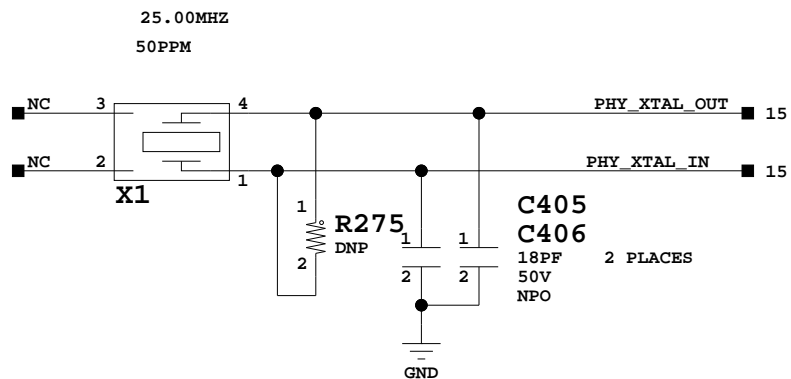
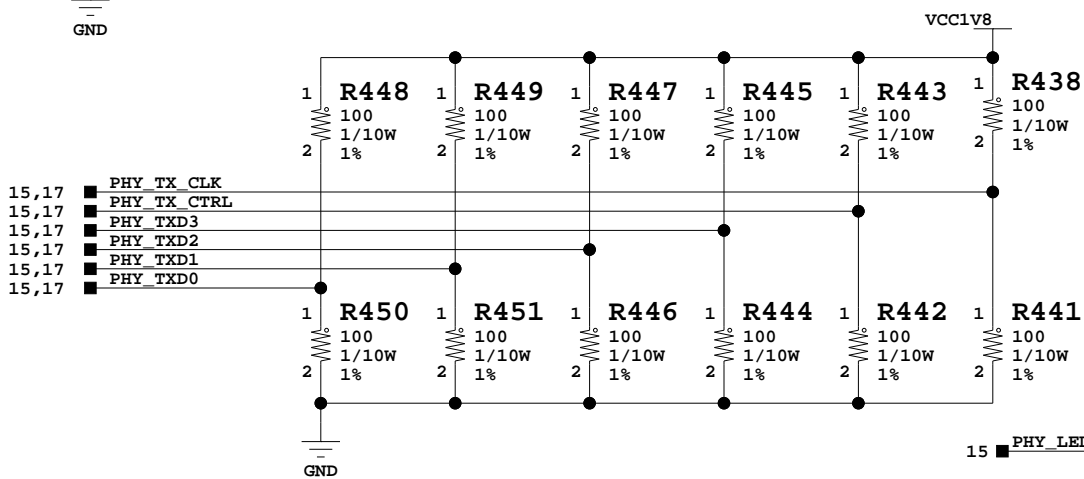
VDDO, VDDOR



- 1 TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESISTORS ON HSDAC\_P AND HSDAC\_N.
- 2 SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

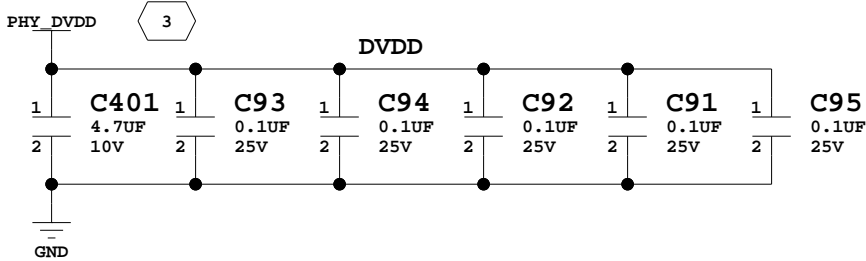
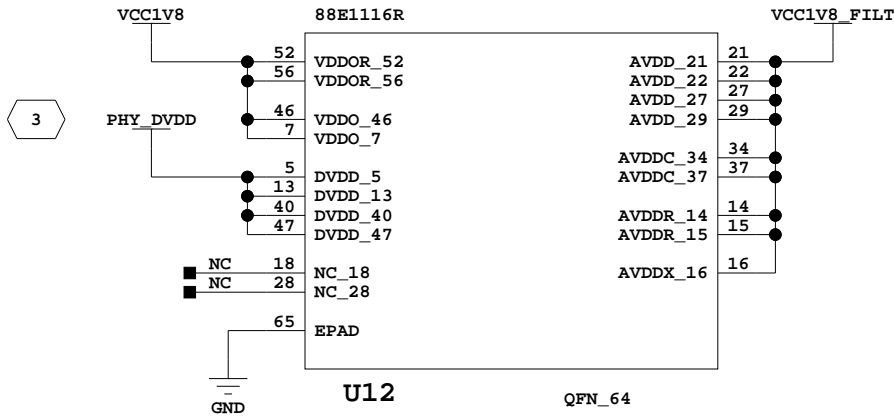


PHY POWER SYMBOL & CAPS MOVED TO PG. 16

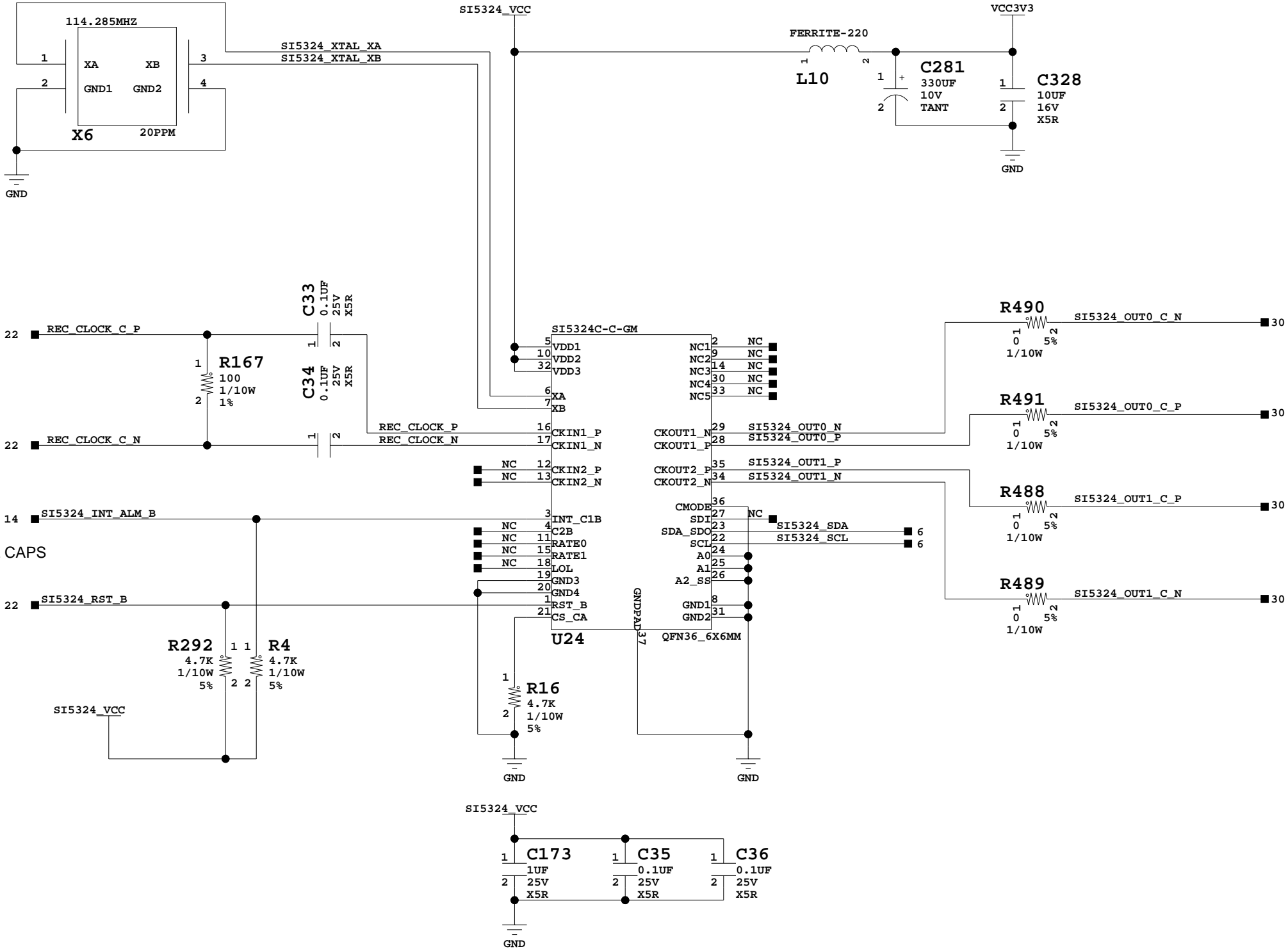


GEM / MDIO

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD 10/100/1000 PHY	
Date:	10-9-2012_15:53	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	15 of 51	Drawn By	DN



3 DVDD 1.2V IS SUPPLIED INTERNALLY. DVDD PINS 5,13,40,47 ARE FOR EXTERNAL CAPS



## 5324 Clock Recovery



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD SI5324 CLOCK RECOVERY
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Date:	9-20-2012_14:39	Ver:	1.0
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Sheet Size: B	Rev:	01
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Sheet	16 of 51	Drawn By	DN
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SOC\_IRON\_FG676

BANK 13  
XC7A200TFBG676

IO_0_T0_13	U24
IO_L1P_T0_13	U25
IO_L1N_T0_13	U26
IO_L2P_T0_13	V26
IO_L2N_T0_13	W26
IO_L3P_T0_DQS_13	AB26
IO_L3N_T0_DQS_13	AC26
IO_L4P_T0_13	W25
IO_L4N_T0_13	Y26
IO_L5P_T0_13	Y25
IO_L5N_T0_13	AA25
IO_L6P_T0_13	V24
IO_L6N_T0_VREF_13	W24
IO_L7P_T1_13	AA24
IO_L7N_T1_13	AB25
IO_L8P_T1_13	AA22
IO_L8N_T1_13	AA23
IO_L9P_T1_DQS_13	AB24
IO_L9N_T1_DQS_13	AC24
IO_L10P_T1_13	V23
IO_L10N_T1_13	W23
IO_L11P_T1_SRCC_13	Y22
IO_L11N_T1_SRCC_13	Y23
IO_L12P_T1_MRCC_13	U22
IO_L12N_T1_MRCC_13	V22
IO_L13P_T2_MRCC_13	U21
IO_L13N_T2_MRCC_13	V21
IO_L14P_T2_SRCC_13	W21
IO_L14N_T2_SRCC_13	Y21
IO_L15P_T2_DQS_13	T20
IO_L15N_T2_DQS_13	U20
IO_L16P_T2_13	W20
IO_L16N_T2_13	Y20
IO_L17P_T2_13	T19
IO_L17N_T2_13	U19
IO_L18P_T2_13	V19
IO_L18N_T2_13	W19
IO_L19P_T3_13	V18
IO_L19N_T3_VREF_13	W18
IO_L20P_T3_13	T14
IO_L20N_T3_13	T15
IO_L21P_T3_DQS_13	T17
IO_L21N_T3_DQS_13	T18
IO_L22P_T3_13	U15
IO_L22N_T3_13	U16
IO_L23P_T3_13	U14
IO_L23N_T3_13	V14
IO_L24P_T3_13	V16
IO_L24N_T3_13	V17
IO_25_T3_13	U17

U24	HDMI_R_D21	19
U25	HDMI_R_D16	19
U26	HDMI_R_D11	19
V26	HDMI_R_D7	19
W26	HDMI_R_D8	19
AB26	HDMI_R_DE	19
AC26	HDMI_R_VSYNC	19
W25	HDMI_R_D9	19
Y26	HDMI_R_D6	19
Y25	HDMI_R_D5	19
AA25	HDMI_R_D29	19
V24	HDMI_R_D17	19
W24	HDMI_R_D10	19
AA24	HDMI_R_D4	19
AB25	HDMI_R_D30	19
AA22	HDMI_R_HSYNC	19
AA23	HDMI_R_D28	19
AB24	HDMI_R_D32	19
AC24	HDMI_R_D31	19
V23	HDMI_R_D23	19
W23	HDMI_R_D19	19
Y22	HDMI_R_D33	19
Y23	HDMI_R_D34	19
U22	PHY_TX_CLK	15
V22	HDMI_R_D35	19
U21	PHY_RX_CLK	15
V21	HDMI_R_CLK	15
W21	HDMI_INT	19
Y21	HDMI_R_SPDIF	18
T20	HDMI_SPDIF_OUT_LS	19
U20	HDMI_R_D18	17
W20	HDMI_R_D20	19
Y20	HDMI_R_D22	19
T19	USB_UART_TX	19
U19	USB_UART_RX	5
V19	USB_UART_RTS	5
W19	USB_UART_CTS	5
V18	PHY_RESET_B	5
W18	PHY_MDC	15
T14	PHY_MDIO	15
T15	PHY_TX_CTRL	15
T17	PHY_TXD3	15
T18	PHY_TXD2	15
U15	PHY_TXD1	15
U16	PHY_TXD0	15
U14	PHY_RX_CTRL	15
V14	PHY_RXD3	15
V16	PHY_RXD2	15
V17	PHY_RXD1	15
U17	PHY_RXD0	15

FPGA\_1V8

Y24	VCCO_13_Y24
V20	VCCO_13_V20
U23	VCCO_13_U23
T26	VCCO_13_T26
T16	VCCO_13_T16
AC25	VCCO_13_AC25

U1

SOC\_IRON\_FG676

FPGA\_1V8

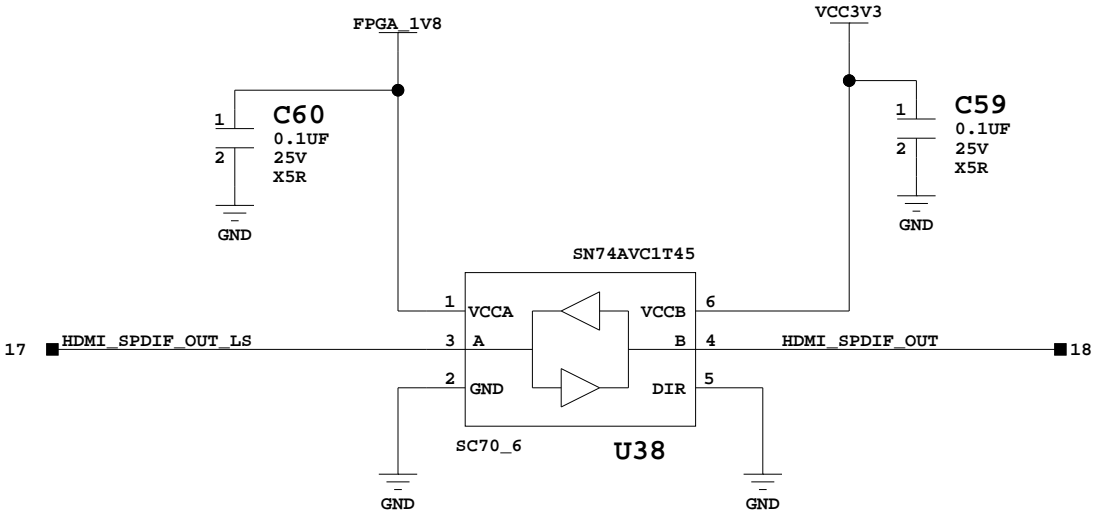
1	C156
2	100UF
	6.3
	X5R
	GND

FPGA\_1V8

1	C60
2	0.1UF
	25V
	X5R
	GND

VCC3V3

1	C59
2	0.1UF
	25V
	X5R
	GND



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
BANK13 HDIM/EPHY IF

Date: 9-20-2012\_14:39 Ver: 1.0

Sheet Size: B Rev: 01

Sheet 17 of 51 Drawn By DN

D

C

B

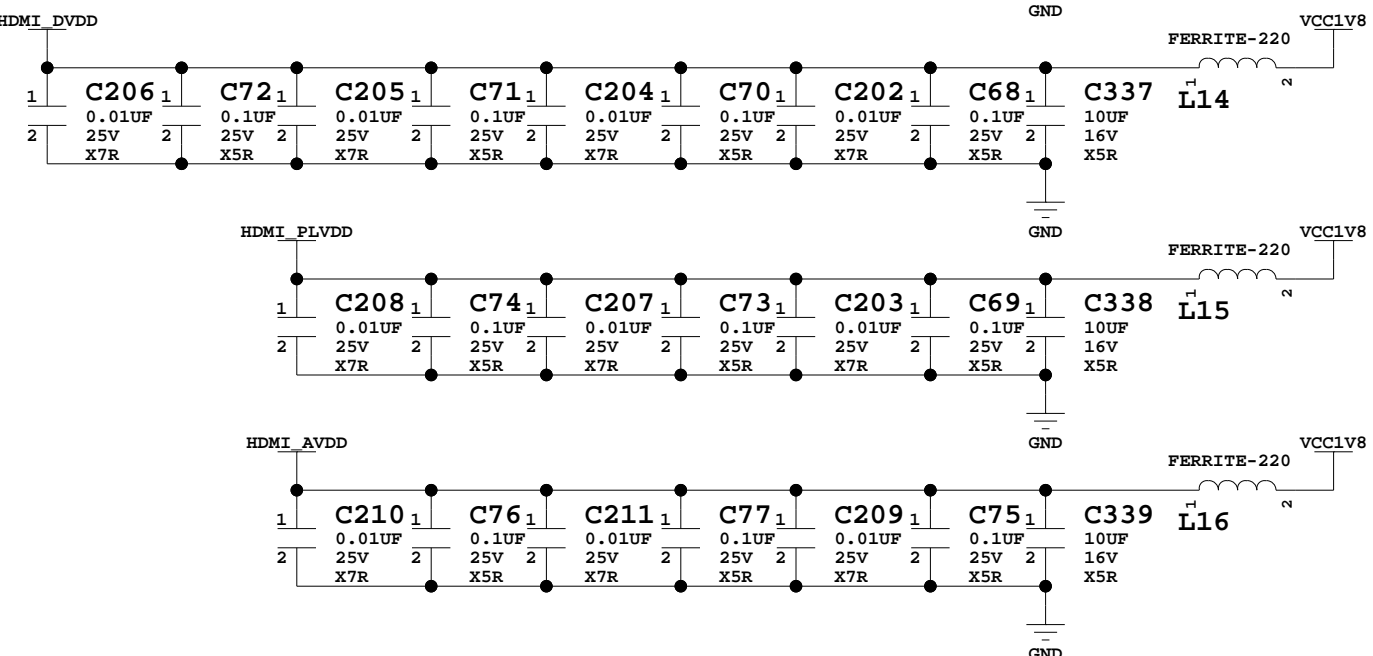
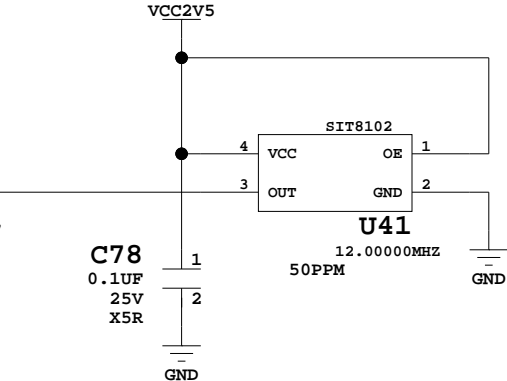
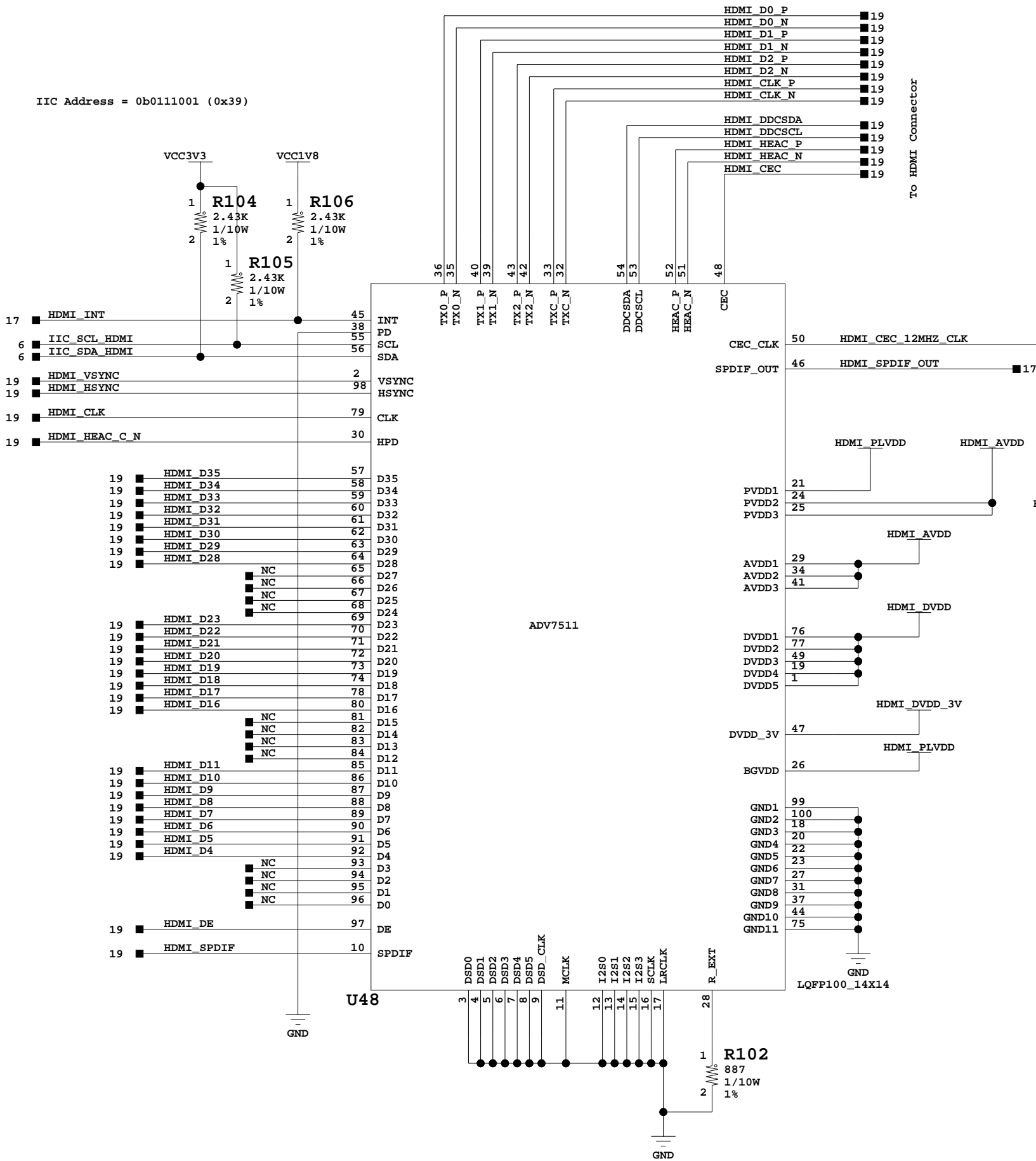
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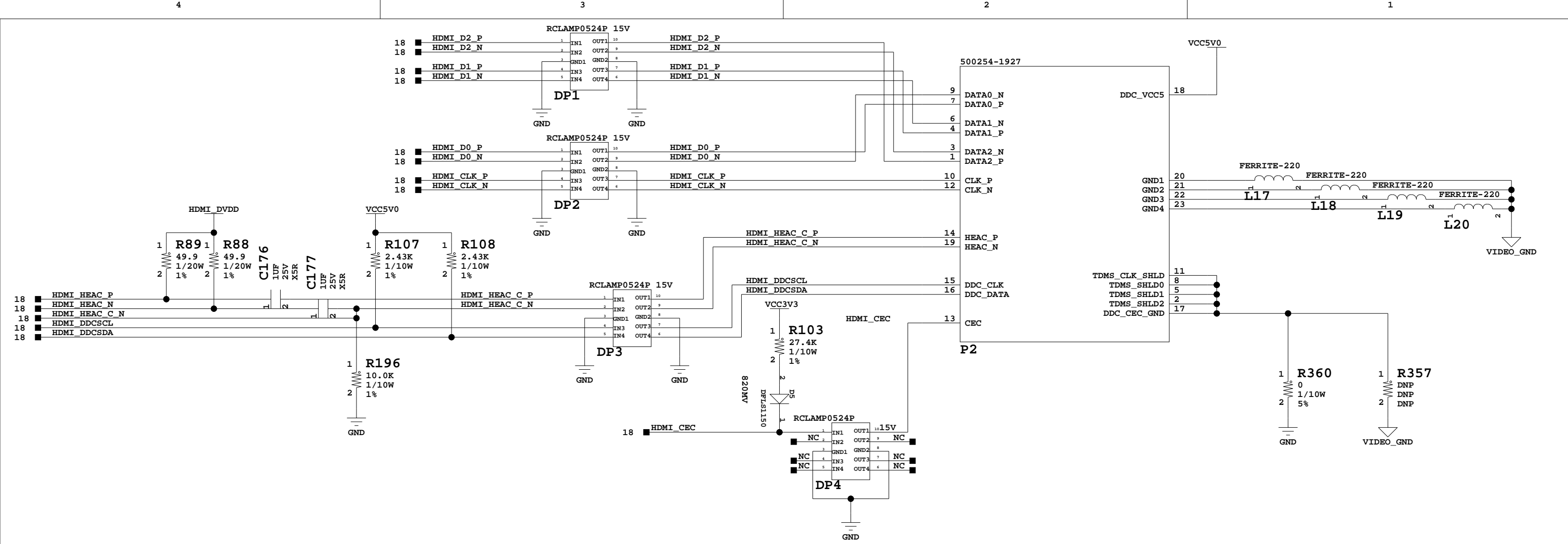
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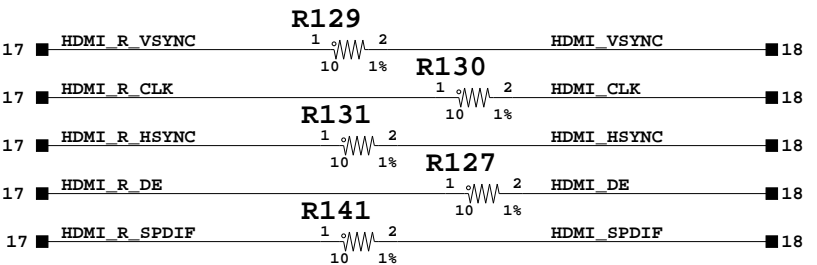
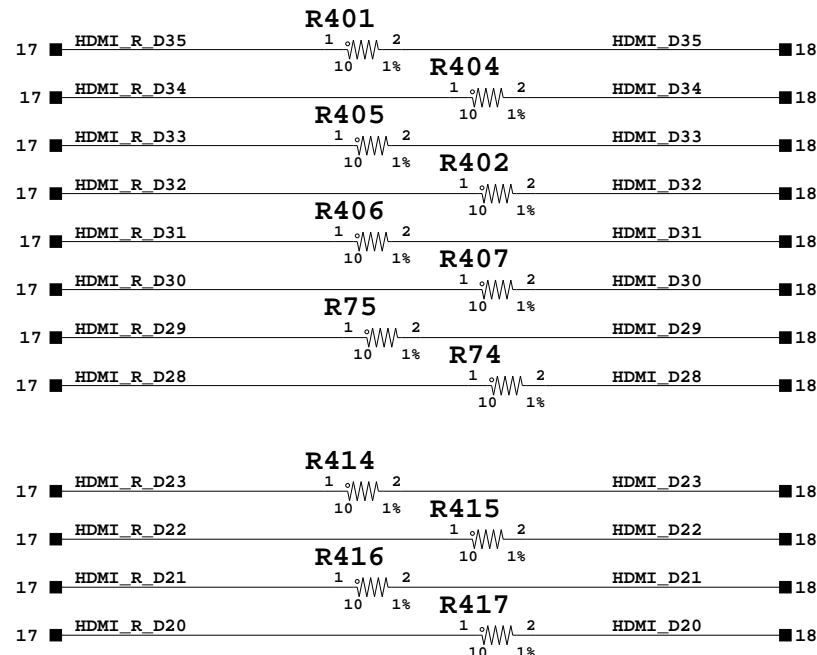
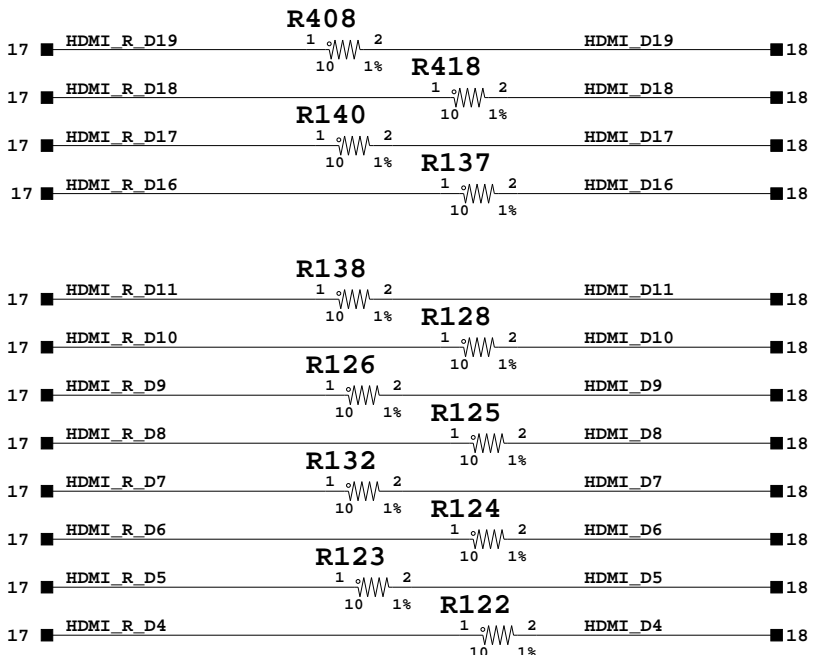
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ADV7511 HDMI CODEC			
			
		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD ADV7511 HDMI CODEC	
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	18 of 51	Drawn By	DN

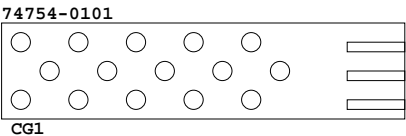
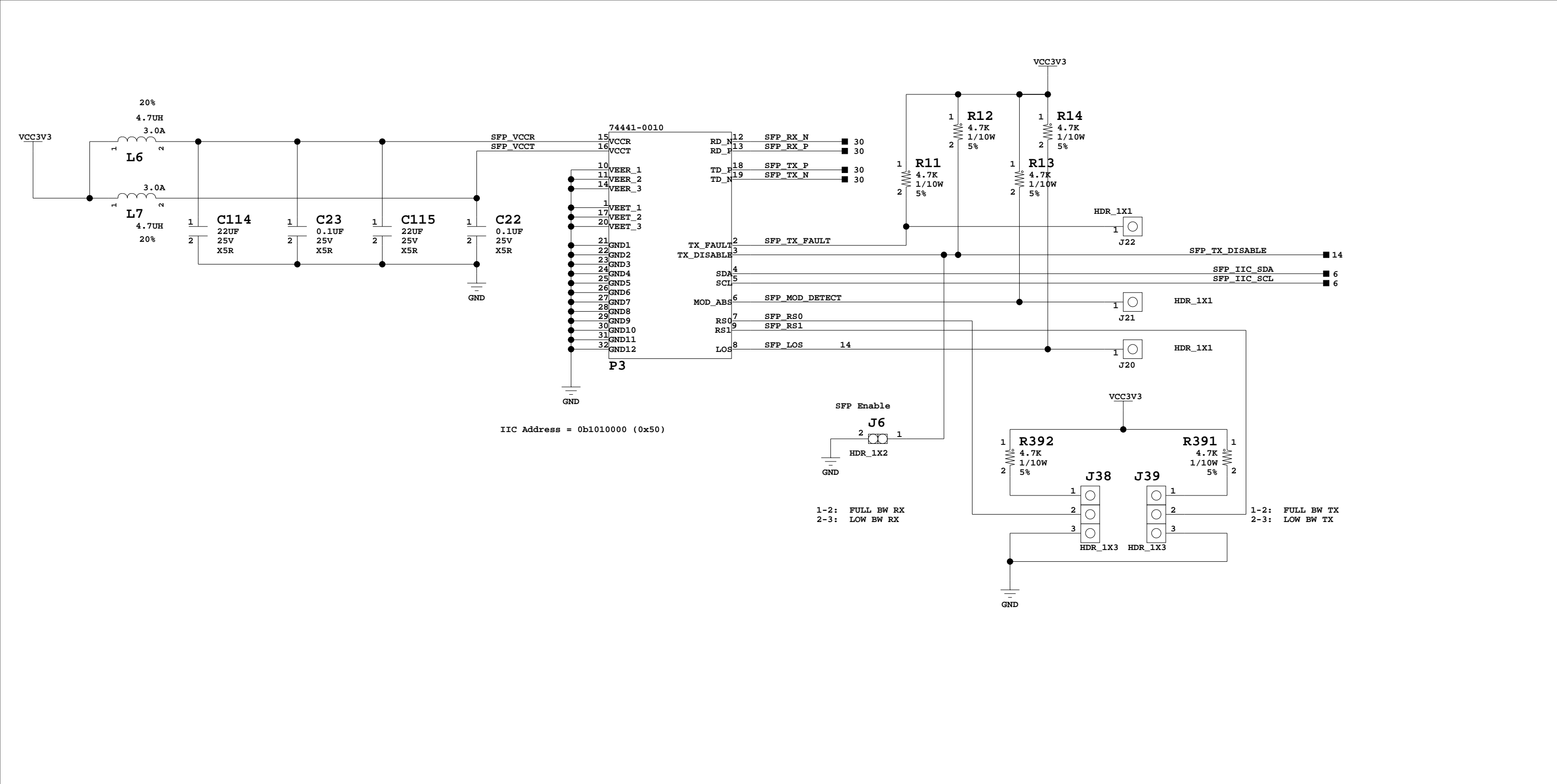


Place series Rs at FPGA




HDMI CONNECTOR

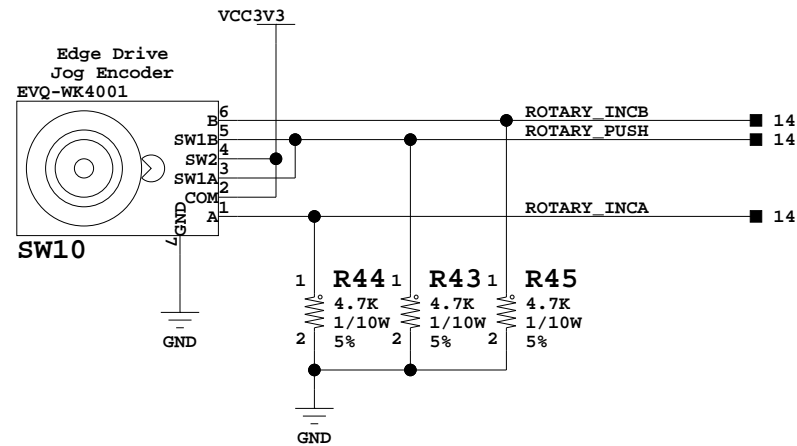
		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD HDMI CONN. P2, HDMI SERIES R's	
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	19 of 51	Drawn By	DN



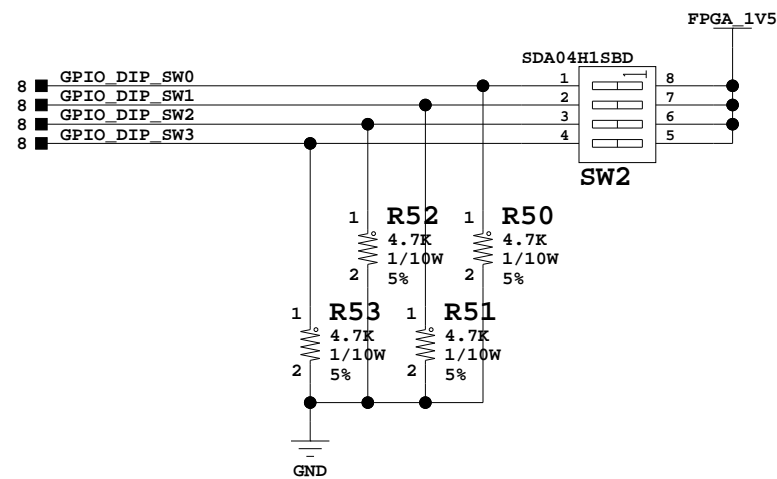
SFP+ Connector and Cage

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD SFP+ CONN. P3			
Date: 9-20-2012_14:39		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 20 of 51		Drawn By DN	

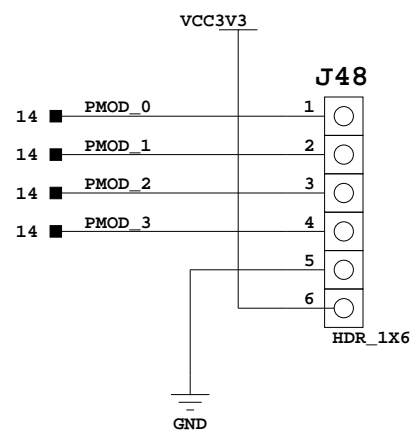
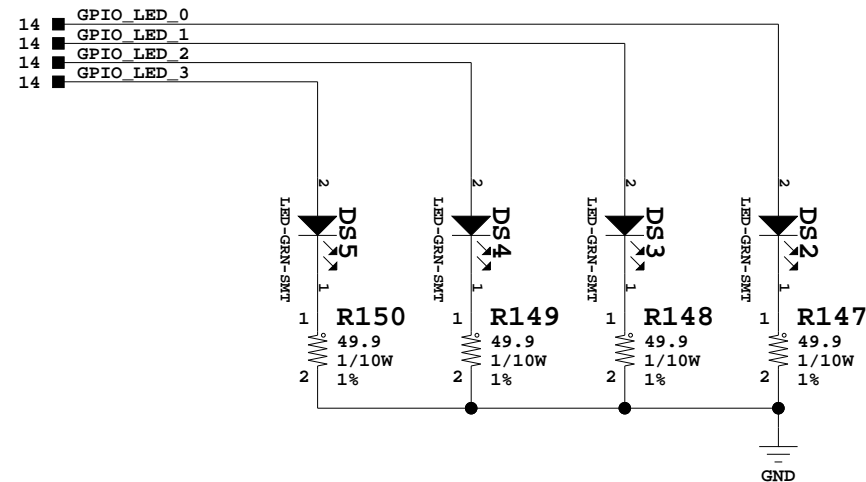
## Rotary Switch



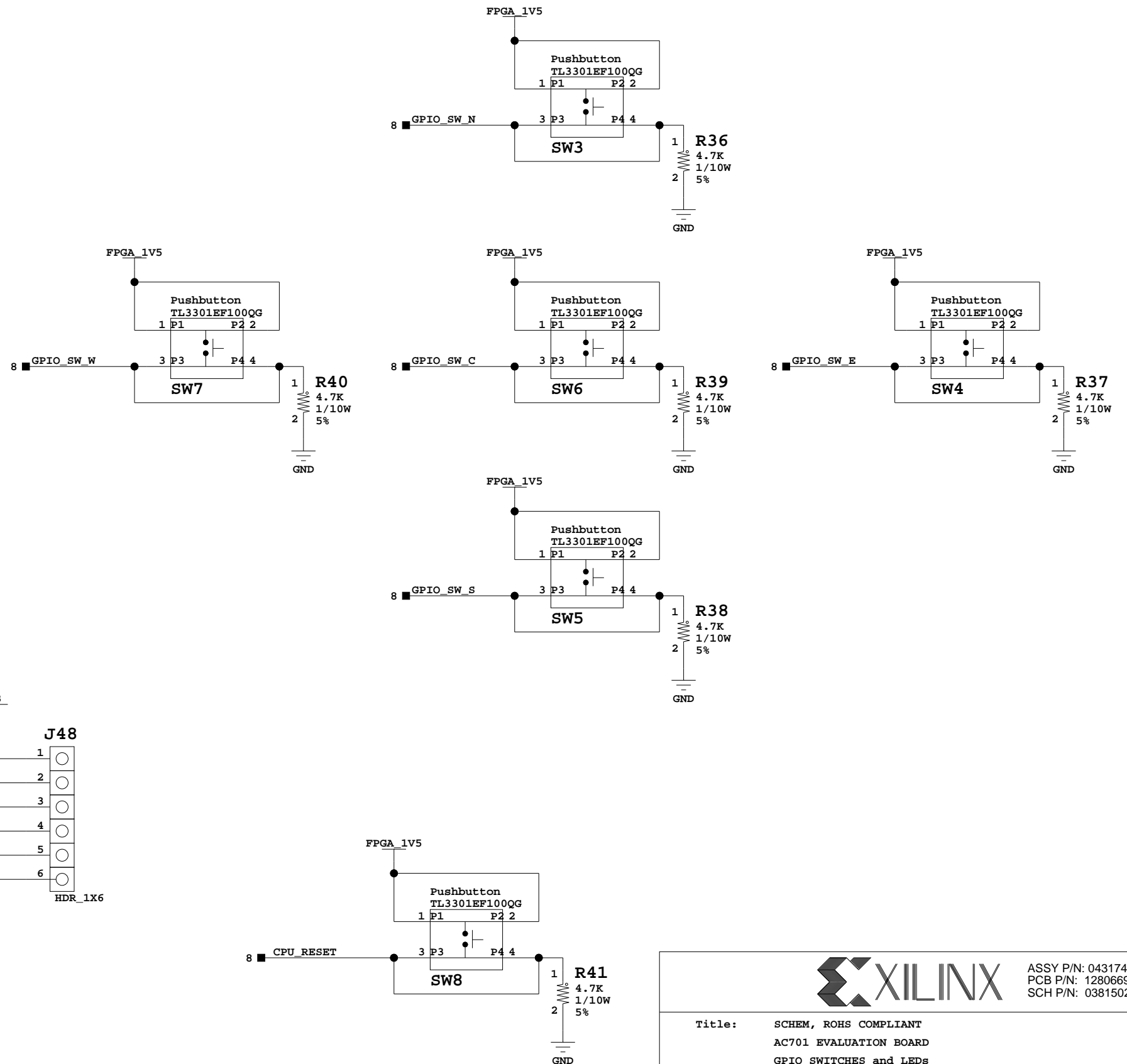
## 4-Pole DIP Switch



## LEDs near top edge



## Directional Push-Buttons



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
GPIO SWITCHES and LEDs

Date: 9-20-2012\_14:39 Ver: 1.0

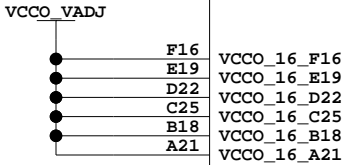
Sheet Size: B Rev: 01

Sheet 21 of 51 Drawn By DN

BANK 16  
XC7A200TFBG676

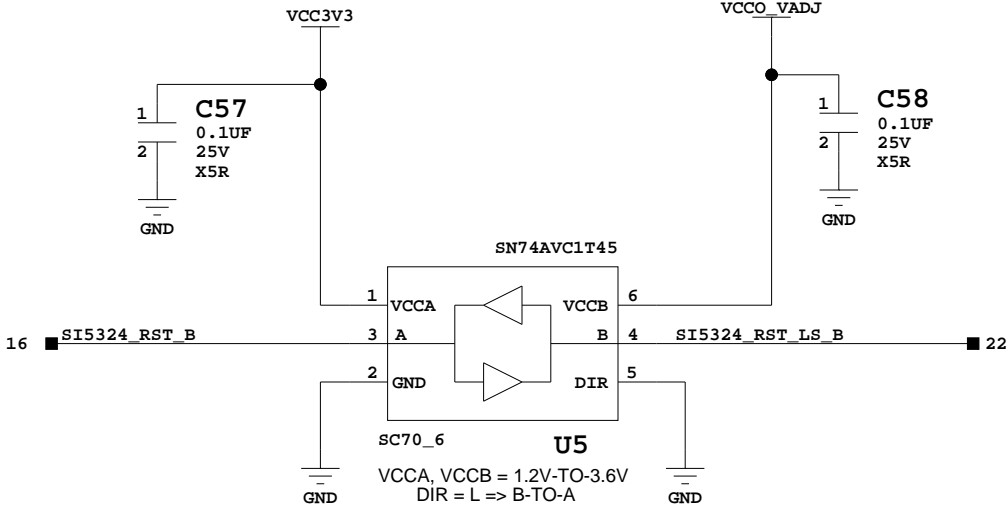
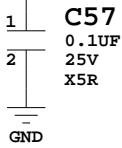
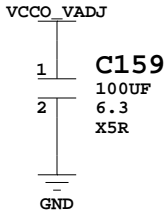
IO_0_16	H17
IO_L1P_T0_16	H14
IO_L1N_T0_16	H15
IO_L2P_T0_16	G17
IO_L2N_T0_16	F17
IO_L3P_T0_DQS_16	F18
IO_L3N_T0_DQS_16	F19
IO_L4P_T0_16	G15
IO_L4N_T0_16	F15
IO_L5P_T0_16	G19
IO_L5N_T0_16	F20
IO_L6P_T0_16	H16
IO_L6N_T0_VREF_16	G16
IO_L7P_T1_16	C17
IO_L7N_T1_16	B17
IO_L8P_T1_16	E16
IO_L8N_T1_16	D16
IO_L9P_T1_DQS_16	A17
IO_L9N_T1_DQS_16	A18
IO_L10P_T1_16	B19
IO_L10N_T1_16	A19
IO_L11P_T1_SRCC_16	E17
IO_L11N_T1_SRCC_16	E18
IO_L12P_T1_MRCC_16	D18
IO_L12N_T1_MRCC_16	C18
IO_L13P_T2_MRCC_16	D19
IO_L13N_T2_MRCC_16	C19
IO_L14P_T2_SRCC_16	E20
IO_L14N_T2_SRCC_16	D20
IO_L15P_T2_DQS_16	B20
IO_L15N_T2_DQS_16	A20
IO_L16P_T2_16	C21
IO_L16N_T2_16	B21
IO_L17P_T2_16	B22
IO_L17N_T2_16	A22
IO_L18P_T2_16	E21
IO_L18N_T2_16	D21
IO_L19P_T3_16	C22
IO_L19N_T3_VREF_16	C23
IO_L20P_T3_16	B25
IO_L20N_T3_16	A25
IO_L21P_T3_DQS_16	A23
IO_L21N_T3_DQS_16	A24
IO_L22P_T3_16	C26
IO_L22N_T3_16	B26
IO_L23P_T3_16	C24
IO_L23N_T3_16	B24
IO_L24P_T3_16	D23
IO_L24N_T3_16	D24
IO_25_16	E22

H17	XADC_GPIO_0	29
H14	FMC1_HPC_LA02_P	26
H15	FMC1_HPC_LA02_N	26
G17	FMC1_HPC_LA03_P	25
F17	FMC1_HPC_LA03_N	25
F18	FMC1_HPC_LA04_P	26
F19	FMC1_HPC_LA04_N	26
G15	FMC1_HPC_LA05_P	24
F15	FMC1_HPC_LA05_N	24
G19	FMC1_HPC_LA06_P	24
F20	FMC1_HPC_LA06_N	24
H16	FMC1_HPC_LA07_P	26
G16	FMC1_HPC_LA07_N	26
C17	FMC1_HPC_LA08_P	25
B17	FMC1_HPC_LA08_N	25
E16	FMC1_HPC_LA09_P	24
D16	FMC1_HPC_LA09_N	24
A17	FMC1_HPC_LA10_P	24
A18	FMC1_HPC_LA10_N	24
B19	FMC1_HPC_LA11_P	26
A19	FMC1_HPC_LA11_N	26
E17	FMC1_HPC_LA01_CC_P	24
E18	FMC1_HPC_LA01_CC_N	24
D18	FMC1_HPC_LA00_CC_P	25
C18	FMC1_HPC_LA00_CC_N	25
D19	FMC1_HPC_CLK0_M2C_P	26
C19	FMC1_HPC_CLK0_M2C_N	26
E20	FMC1_HPC_LA12_P	25
D20	FMC1_HPC_LA12_N	25
B20	FMC1_HPC_LA13_P	24
A20	FMC1_HPC_LA13_N	24
C21	FMC1_HPC_LA14_P	24
B21	FMC1_HPC_LA14_N	24
B22	FMC1_HPC_LA15_P	26
A22	FMC1_HPC_LA15_N	26
E21	FMC1_HPC_LA16_P	25
D21	FMC1_HPC_LA16_N	25
C22	NC	
C23	NC	
B25	XADC_MUX_ADDR0_LS	37
A25	XADC_MUX_ADDR1_LS	37
A23	XADC_MUX_ADDR2_LS	37
A24	PCIE_MGT_CLK_SEL0	30
C26	PCIE_MGT_CLK_SEL1	30
B26	SFP_MGT_CLK_SEL0	30
C24	SFP_MGT_CLK_SEL1	30
B24	SI5324_RST_LS_B	22
D23	REC_CLOCK_C_P	16
D24	REC_CLOCK_C_N	16
E22	XADC_GPIO_1	29



U1

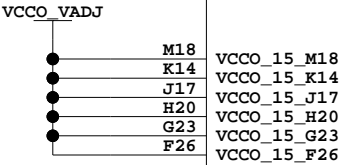
SOC\_IRON\_FG676



BANK 15  
XC7A200TFBG676

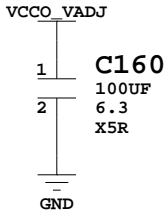
IO_0_15	K18
IO_L1P_T0_AD0P_15	K15
IO_L1N_T0_AD0N_15	J16
IO_L2P_T0_AD8P_15	J14
IO_L2N_T0_AD8N_15	J15
IO_L3P_T0_DQS_AD1P_15	K16
IO_L3N_T0_DQS_AD1N_15	K17
IO_L4P_T0_15	M14
IO_L4N_T0_15	L14
IO_L5P_T0_AD9P_15	M15
IO_L5N_T0_AD9N_15	L15
IO_L6P_T0_15	M16
IO_L6N_T0_VREF_15	M17
IO_L7P_T1_AD2P_15	J19
IO_L7N_T1_AD2N_15	H19
IO_L8P_T1_AD10P_15	L17
IO_L8N_T1_AD10N_15	L18
IO_L9P_T1_DQS_AD3P_15	K20
IO_L9N_T1_DQS_AD3N_15	J20
IO_L10P_T1_AD11P_15	J18
IO_L10N_T1_AD11N_15	H18
IO_L11P_T1_SRCC_15	G20
IO_L11N_T1_SRCC_15	G21
IO_L12P_T1_MRCC_15	K21
IO_L12N_T1_MRCC_15	J21
IO_L13P_T2_MRCC_15	H21
IO_L13N_T2_MRCC_15	H22
IO_L14P_T2_SRCC_15	J23
IO_L14N_T2_SRCC_15	H23
IO_L15P_T2_DQS_ADV_B_15	G22
IO_L15N_T2_DQS_ADV_B_15	F22
IO_L16P_T2_A28_15	J24
IO_L16N_T2_A27_15	H24
IO_L17P_T2_A26_15	F23
IO_L17N_T2_A25_15	E23
IO_L18P_T2_A24_15	K22
IO_L18N_T2_A23_15	K23
IO_L19P_T3_A22_15	G24
IO_L19N_T3_A21_VREF_15	F24
IO_L20P_T3_A20_15	E25
IO_L20N_T3_A19_15	D25
IO_L21P_T3_DQS_15	E26
IO_L21N_T3_DQS_A18_15	D26
IO_L22P_T3_A17_15	H26
IO_L22N_T3_A16_15	G26
IO_L23P_T3_FOE_B_15	G25
IO_L23N_T3_FWE_B_15	F25
IO_L24P_T3_RS1_15	J25
IO_L24N_T3_RS0_15	J26
IO_25_15	L19

K18	XADC_GPIO_2	29
K15	XADC_VAUX0_R_P	29
J16	XADC_VAUX0_R_N	29
J14	XADC_VAUX8_R_P	29
J15	XADC_VAUX8_R_N	29
K16	XADC_AD1_R_P	37
K17	XADC_AD1_R_N	37
M14	FMC1_HPC_LA19_P	26
L14	FMC1_HPC_LA19_N	26
M15	XADC_AD9_R_P	37
L15	XADC_AD9_R_N	37
M16	FMC1_HPC_LA20_P	25
M17	FMC1_HPC_LA20_N	25
J19	FMC1_HPC_LA21_P	26
H19	FMC1_HPC_LA21_N	26
L17	FMC1_HPC_LA22_P	25
L18	FMC1_HPC_LA22_N	25
K20	FMC1_HPC_LA23_P	24
J20	FMC1_HPC_LA23_N	24
J18	FMC1_HPC_LA24_P	26
H18	FMC1_HPC_LA24_N	26
G20	FMC1_HPC_LA18_CC_P	24
G21	FMC1_HPC_LA18_CC_N	24
K21	FMC1_HPC_LA17_CC_P	24
J21	FMC1_HPC_LA17_CC_N	24
H21	FMC1_HPC_CLK1_M2C_P	25
H22	FMC1_HPC_CLK1_M2C_N	25
J23	USER_SMA_CLOCK_P	3
H23	USER_SMA_CLOCK_N	3
G22	FMC1_HPC_LA25_P	25
F22	FMC1_HPC_LA25_N	25
J24	FMC1_HPC_LA26_P	24
H24	FMC1_HPC_LA26_N	24
F23	FMC1_HPC_LA27_P	24
E23	FMC1_HPC_LA27_N	24
K22	FMC1_HPC_LA28_P	26
K23	FMC1_HPC_LA28_N	26
G24	FMC1_HPC_LA29_P	25
F24	FMC1_HPC_LA29_N	25
E25	FMC1_HPC_LA30_P	26
D25	FMC1_HPC_LA30_N	26
E26	FMC1_HPC_LA31_P	25
D26	FMC1_HPC_LA31_N	25
H26	FMC1_HPC_LA32_P	26
G26	FMC1_HPC_LA32_N	26
G25	FMC1_HPC_LA33_P	25
F25	FMC1_HPC_LA33_N	25
J25	SM_FAN_TACH	38
J26	SM_FAN_PWM	38
L19	XADC_GPIO_3	29



U1

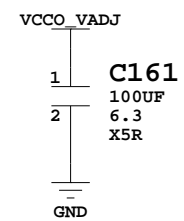
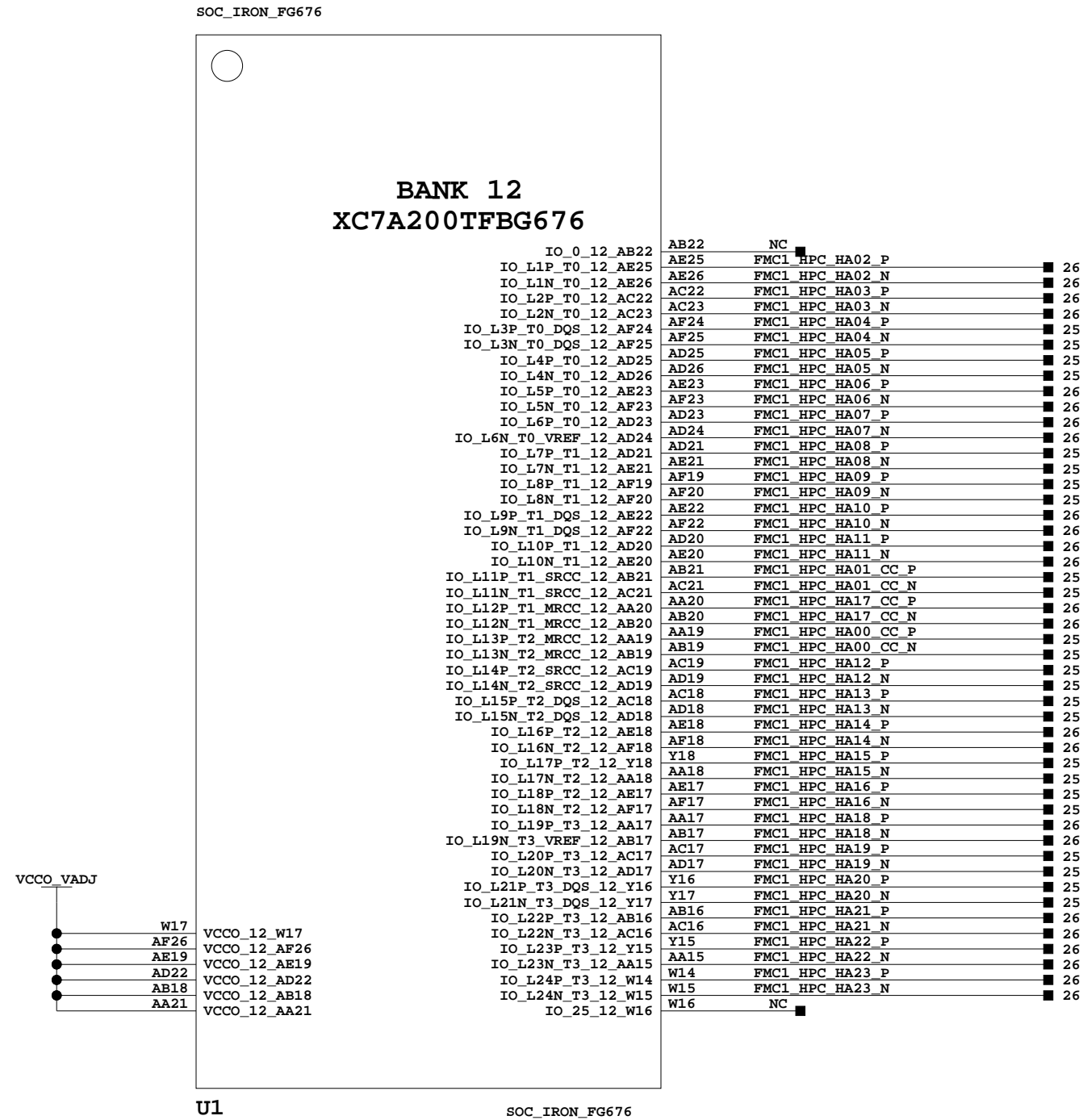
SOC\_IRON\_FG676



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANKS15,16 HPC FMC and XADC IF	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 22 of 51	Drawn By DN

**XC7A200T-FBG676 ONLY**



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
BANK12 HPC FMC IF

Date:	9-20-2012_14:39	Ver:	1.0
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Sheet Size: B	Rev: 01
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Sheet	<b>23</b> of <b>51</b>	Drawn By	DN
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D

C

B

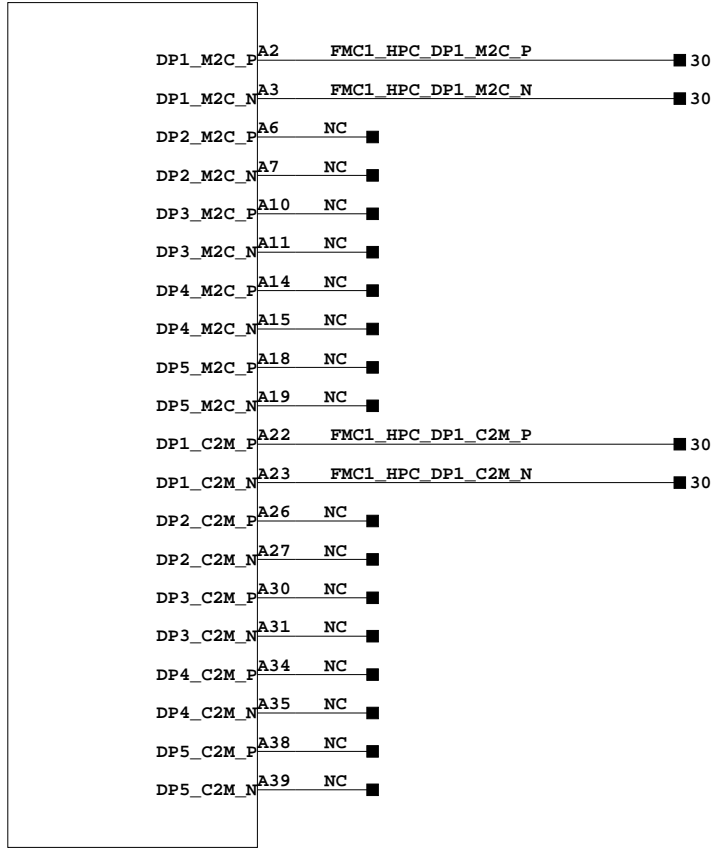
A

D

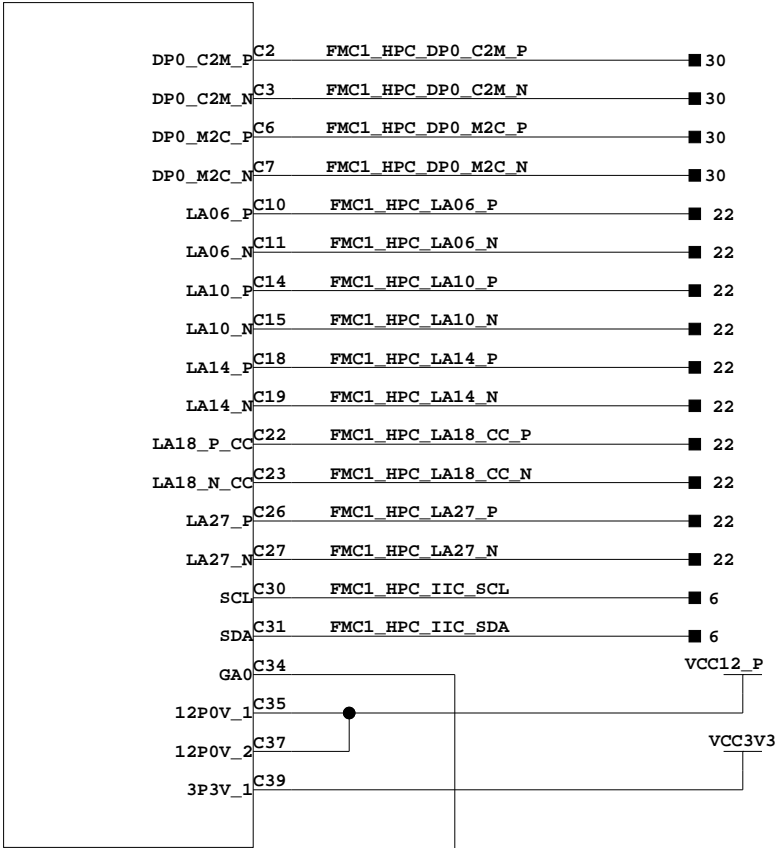
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B

A

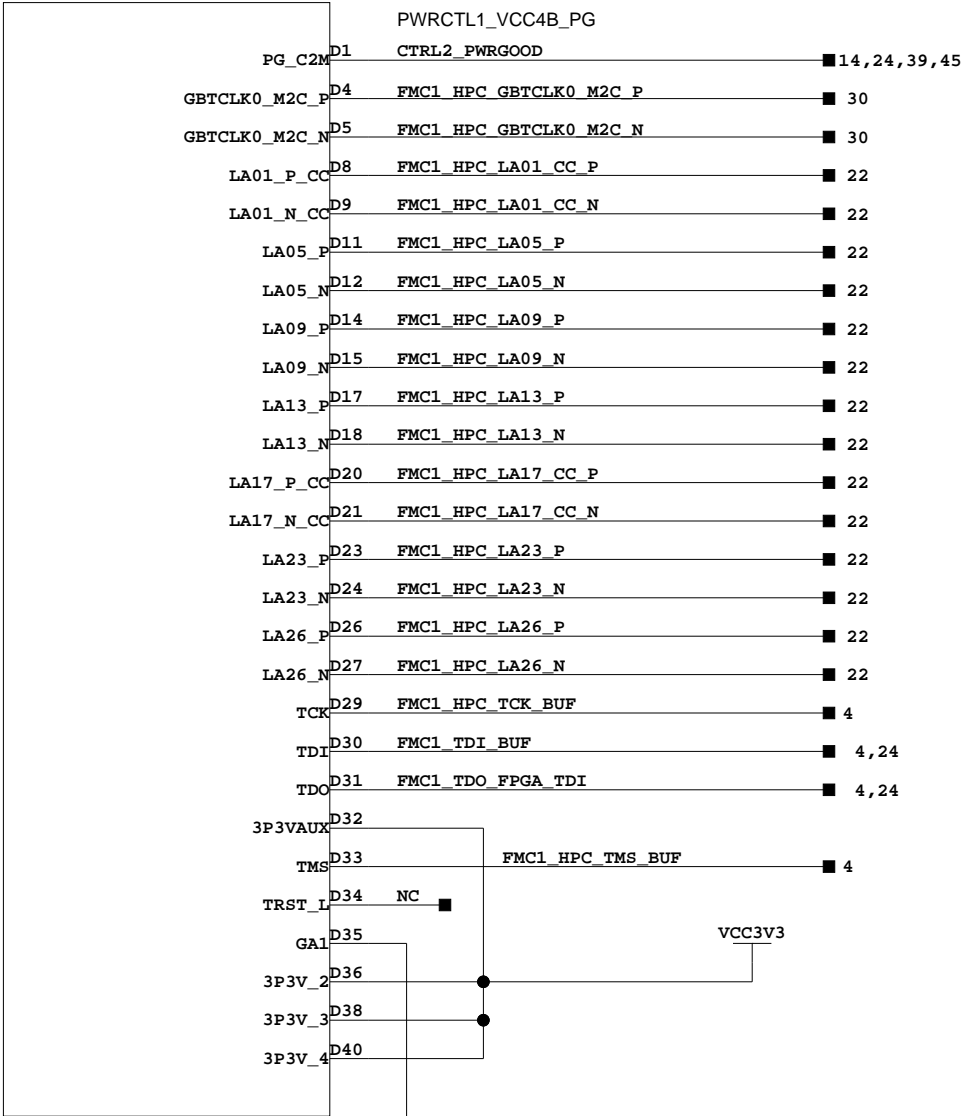


J30  
ASP\_134486\_01

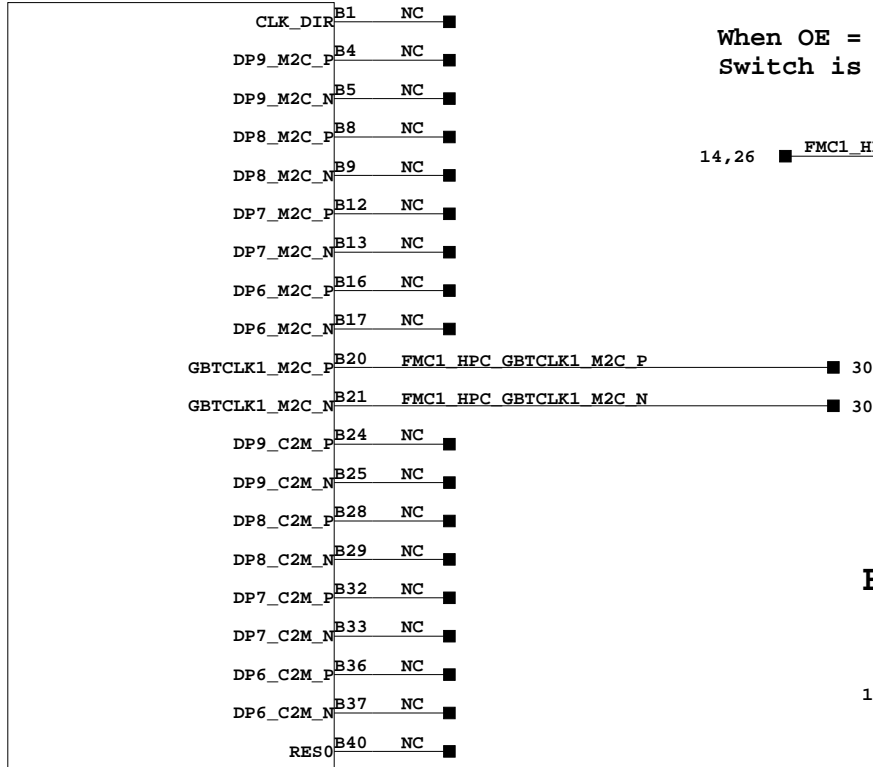


J30  
ASP\_134486\_01

IIC Address = 0bxxxxxx00

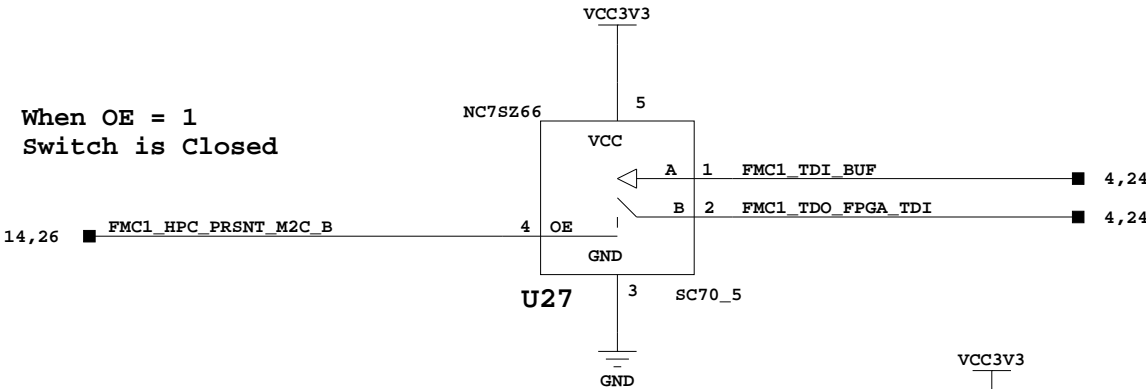


J30  
ASP\_134486\_01



J30  
ASP\_134486\_01

When OE = 1  
Switch is Closed



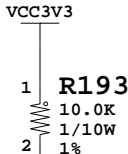
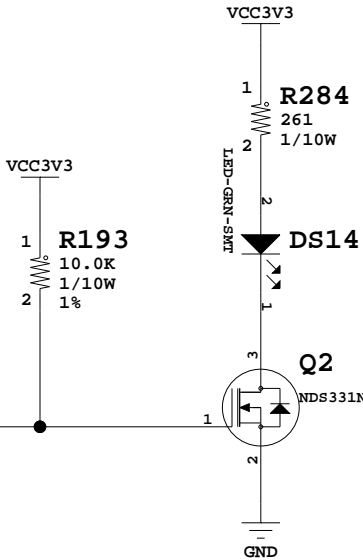
FMC Power Good

14,24,39,45


CTRL2\_PWRGOOD

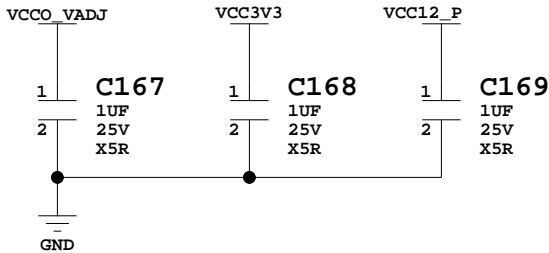
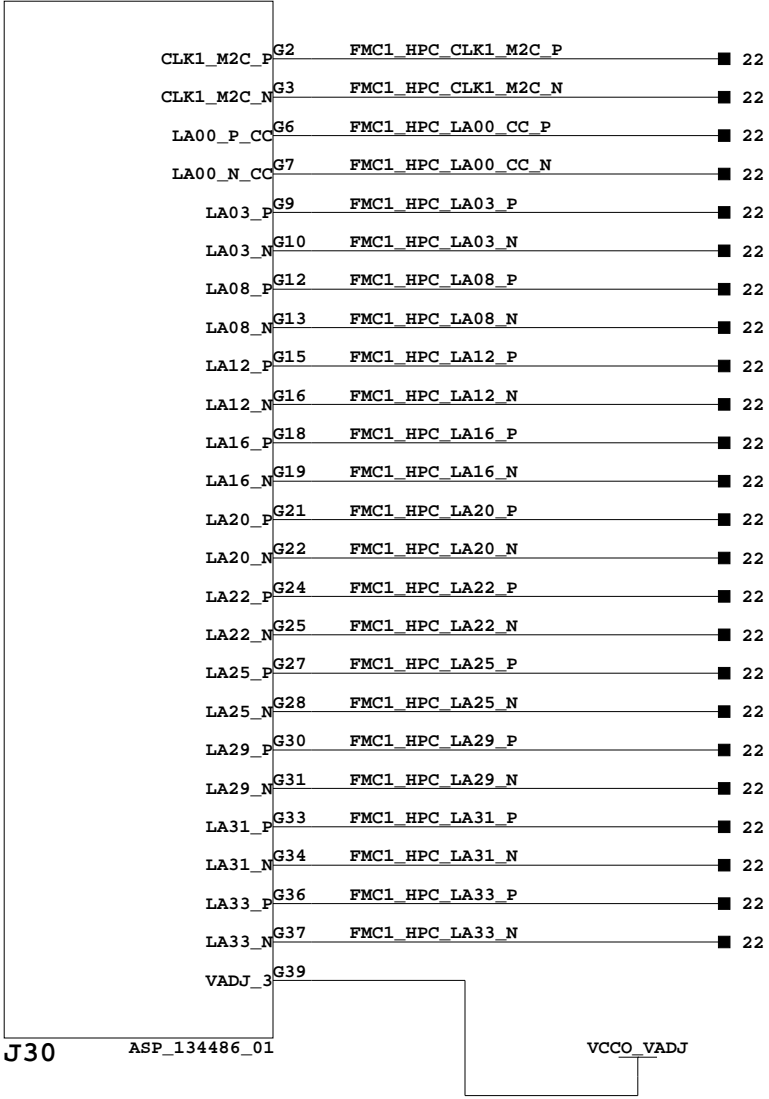
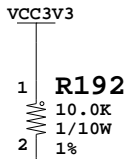
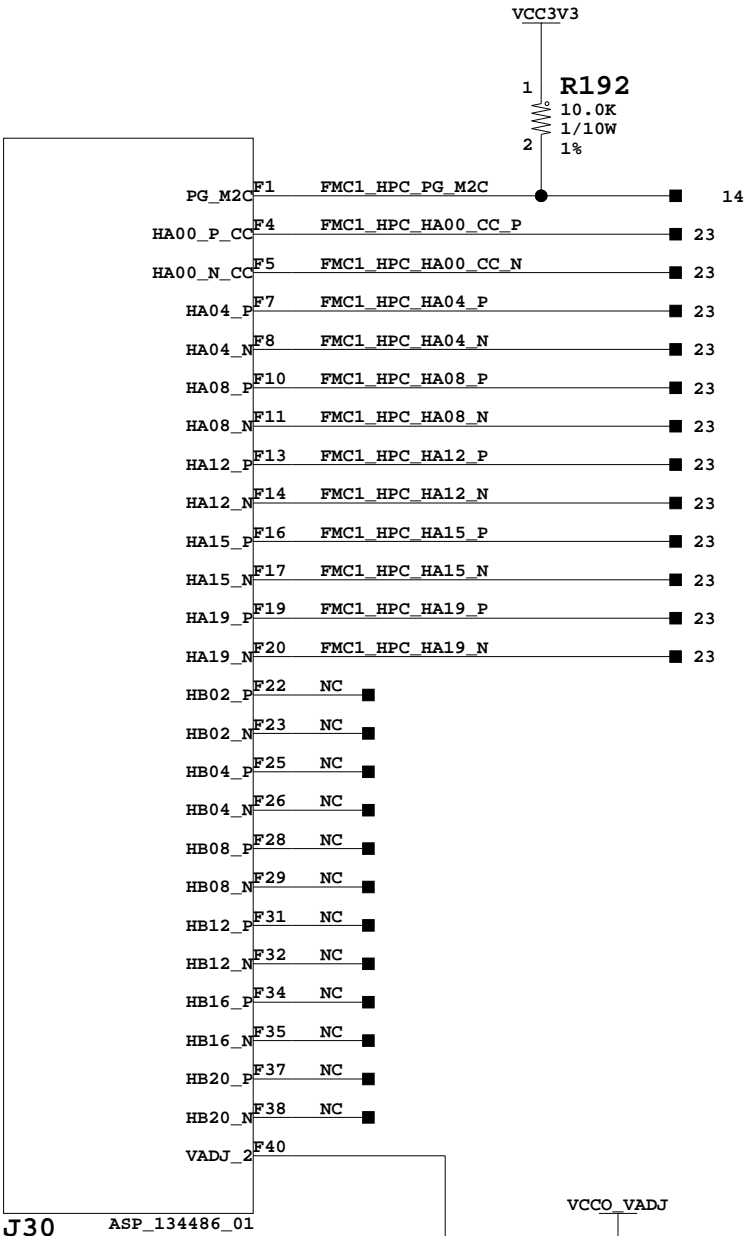
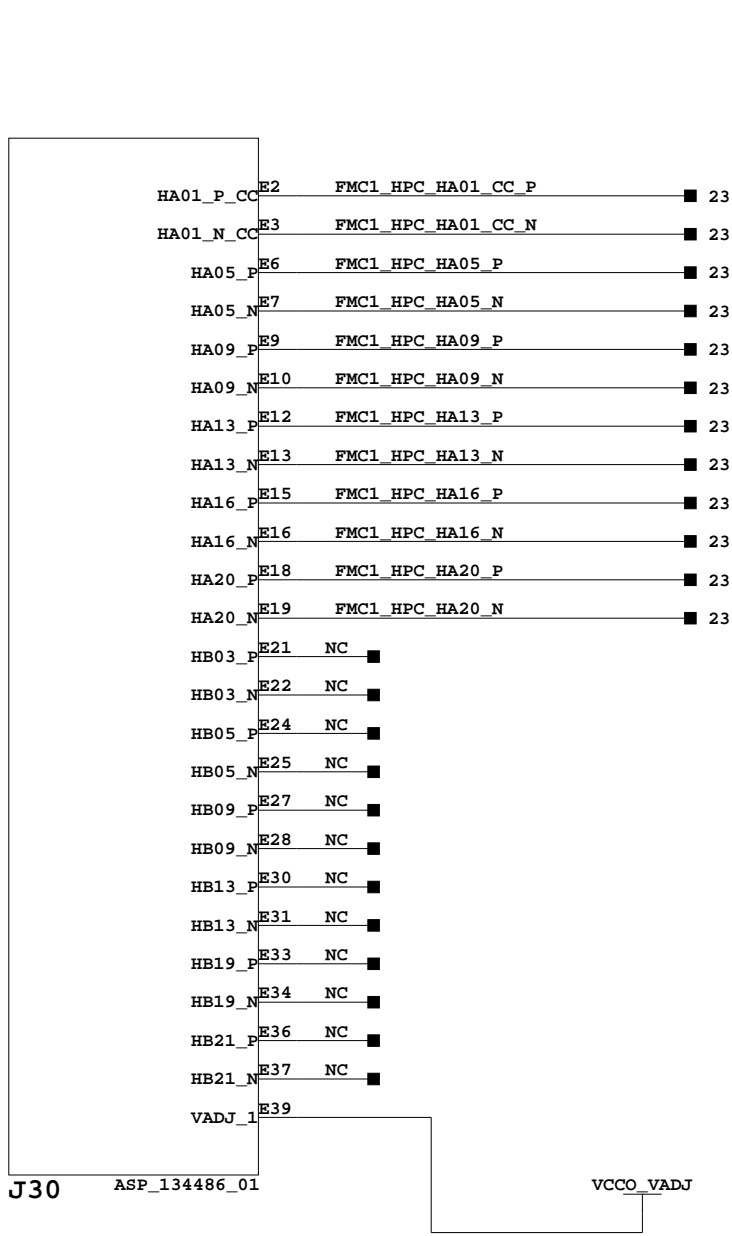
PWRCTL1\_VCC4B\_PG

CTRL2\_PWRGOOD from TI controller U9  
indicates both VCC3V3 and VCCO\_VADJ  
FMC power rails are OK



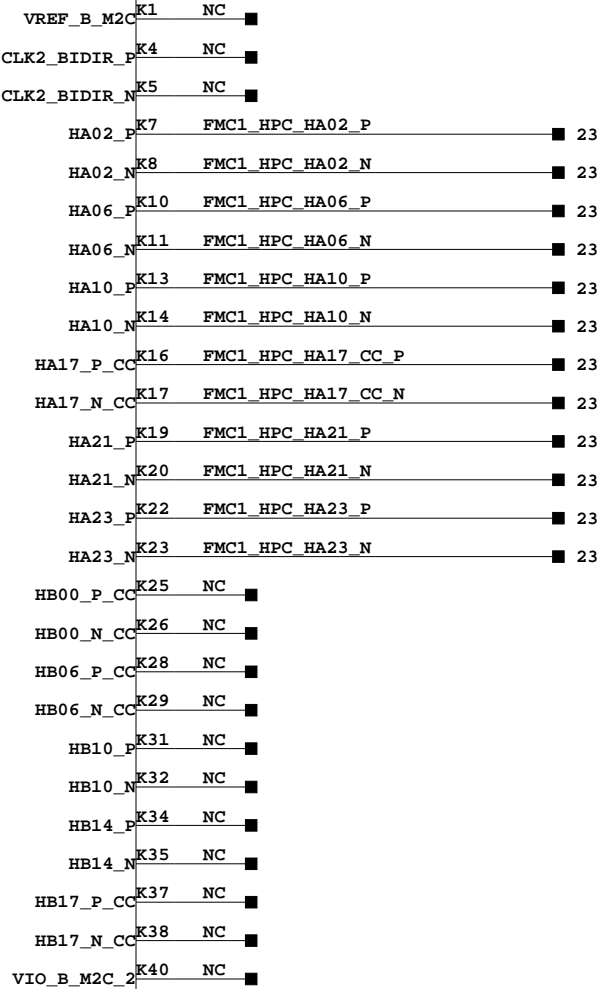
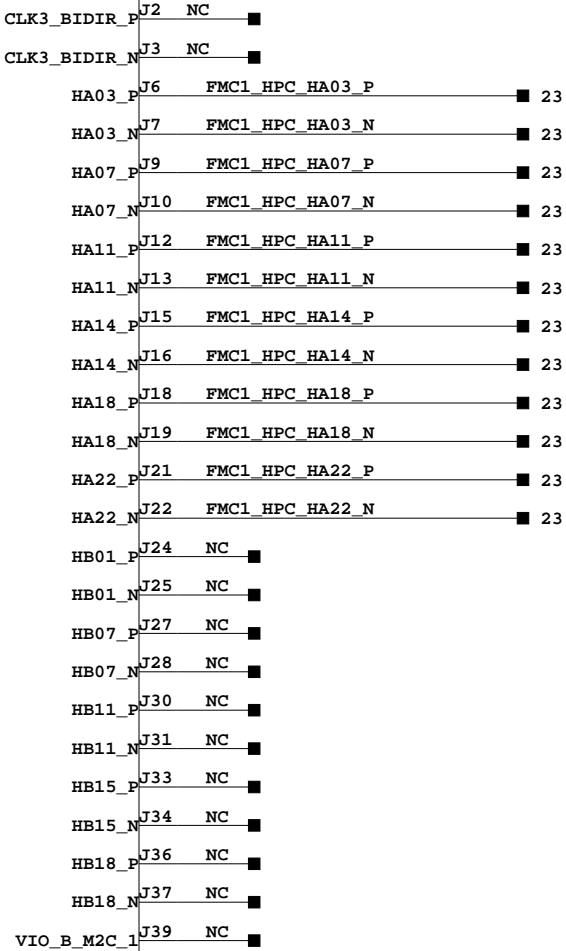
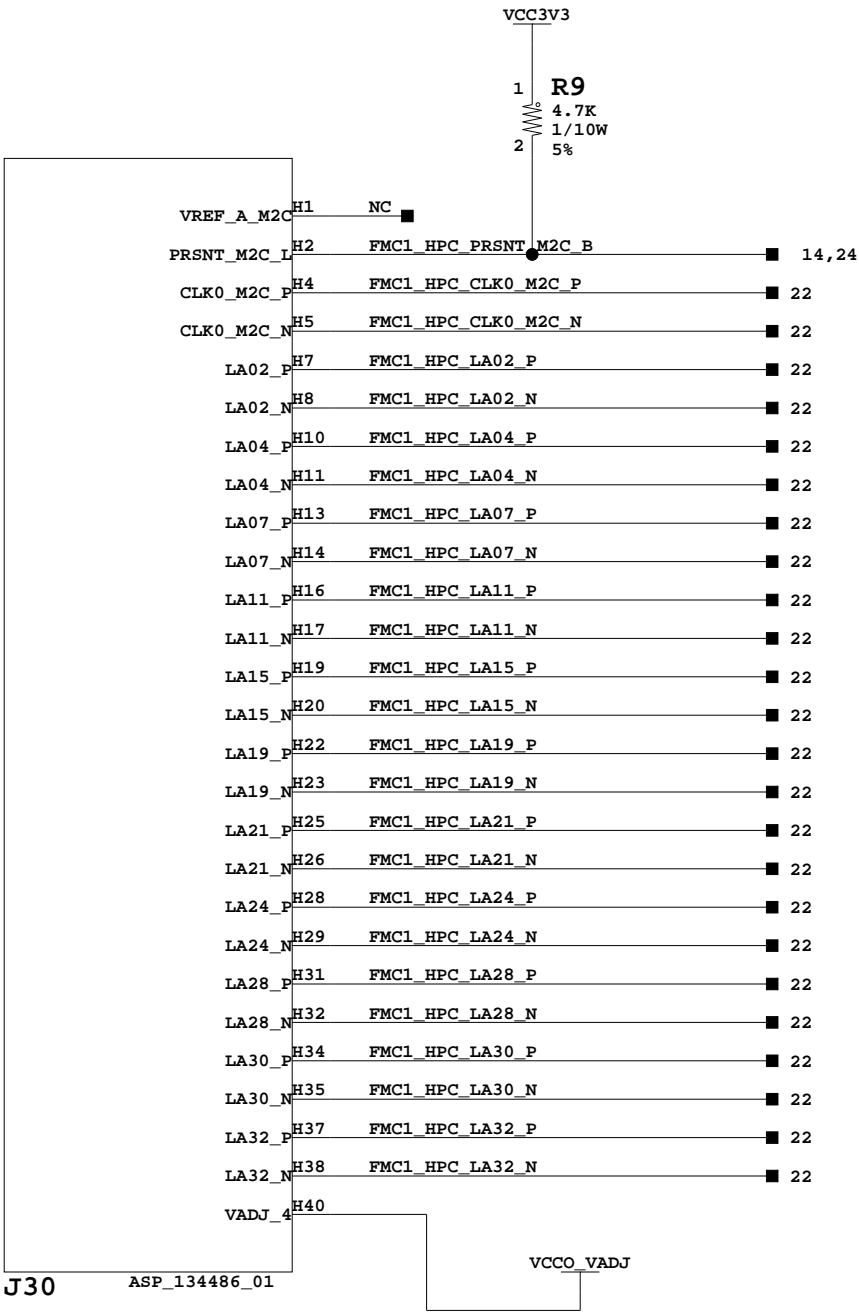
ANSI/VITA 57.1 - Revised 2010  
FMC 1 HPC Header, Rows A, B, C, D

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS A, B, C, D	
Date:	9-20-2012_14:57	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	24 of 51	Drawn By	DN




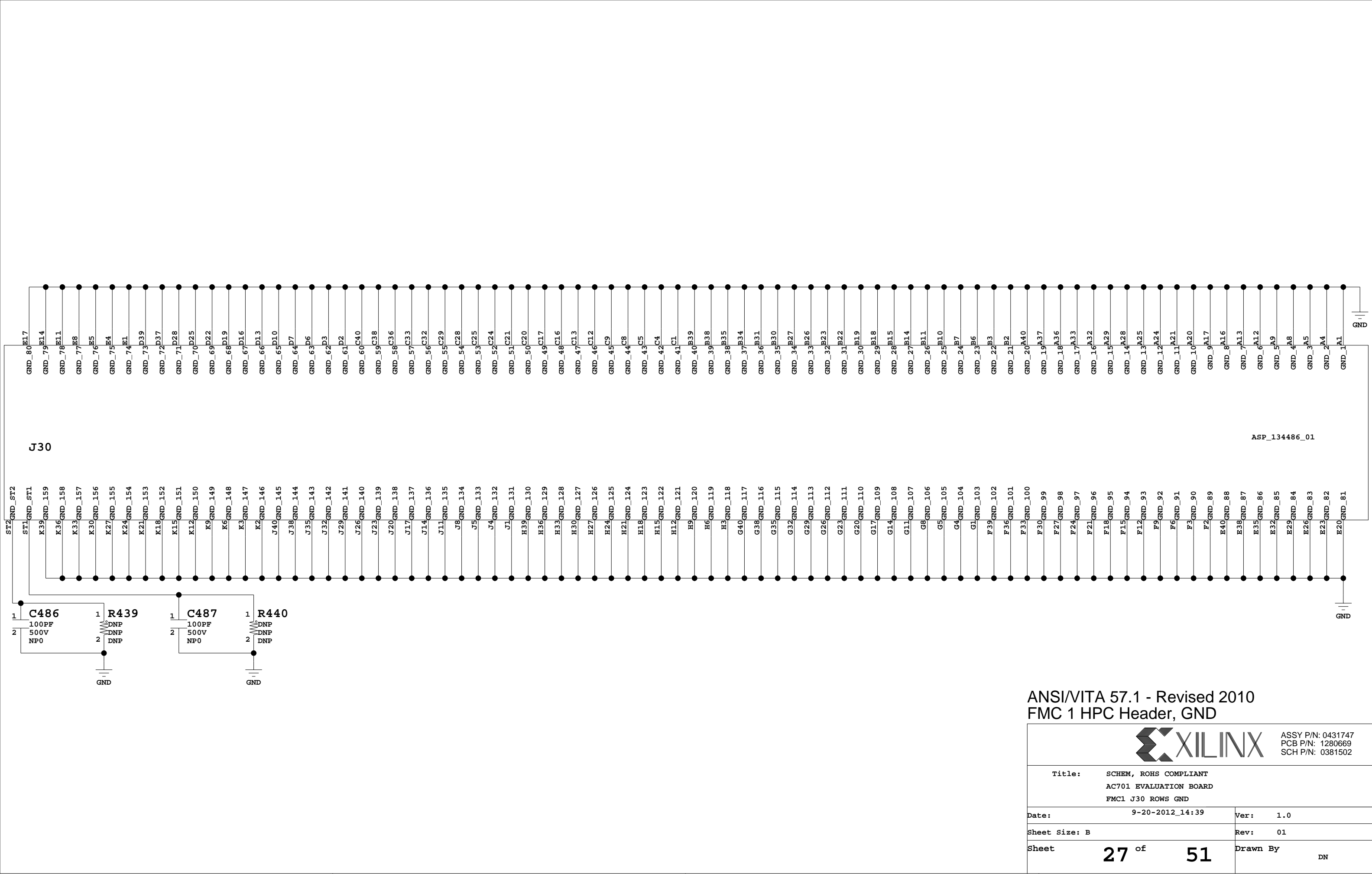
ANSI/VITA 57.1 - Revised 2010  
FMC 1 HPC Header, Rows E, F, G

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS E, F, G	
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	25 of 51	Drawn By	DN




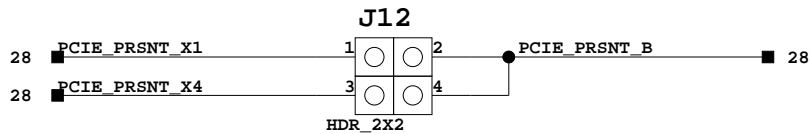
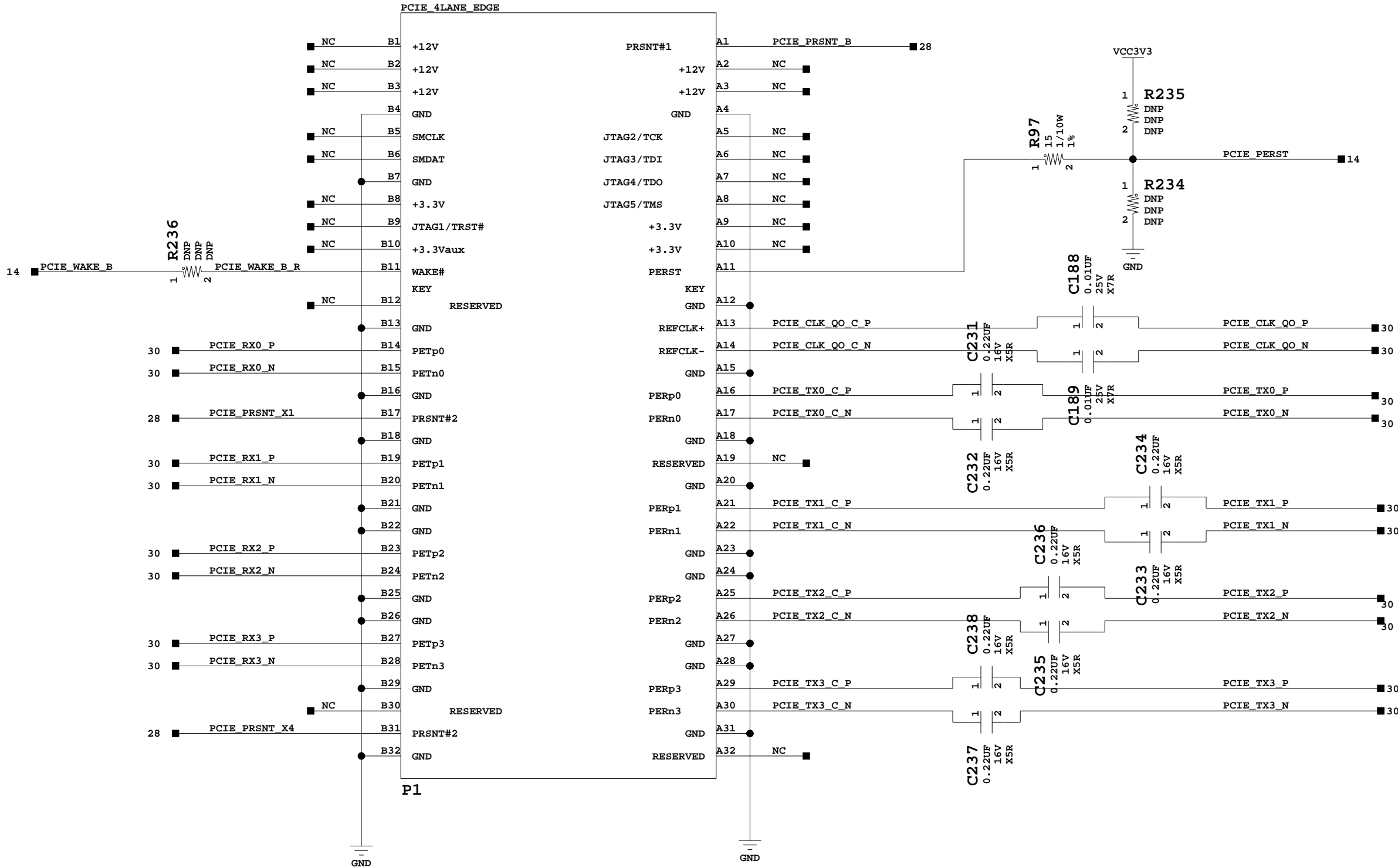
ANSI/VITA 57.1 - Revised 2010  
FMC 1 HPC Header, Rows H, J, K

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS H, J, K	
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	26 of 51	Drawn By	DN



ANSI/VITA 57.1 - Revised 2010  
FMC 1 HPC Header, GND

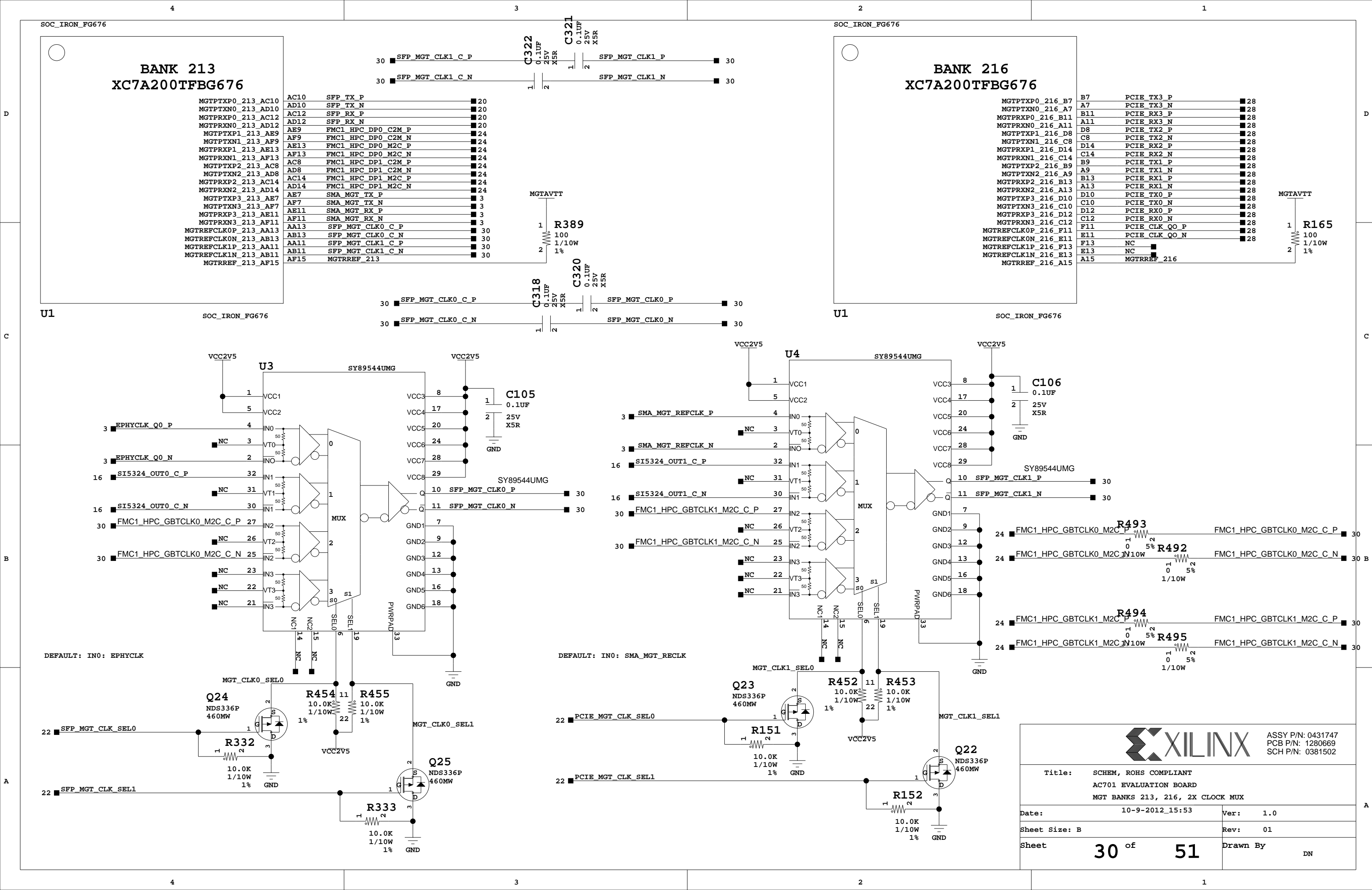
		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS GND	
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	27 of 51	Drawn By	DN



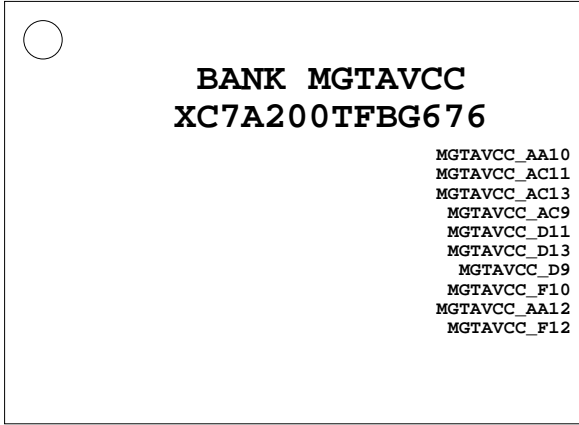
PCIe 4X Card Edge

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD PCIe 4X CARD EDGE CONN. P1	
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	28 of 51	Drawn By	DN



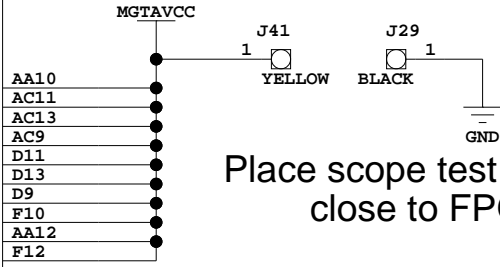


SOC\_IRON\_FG676



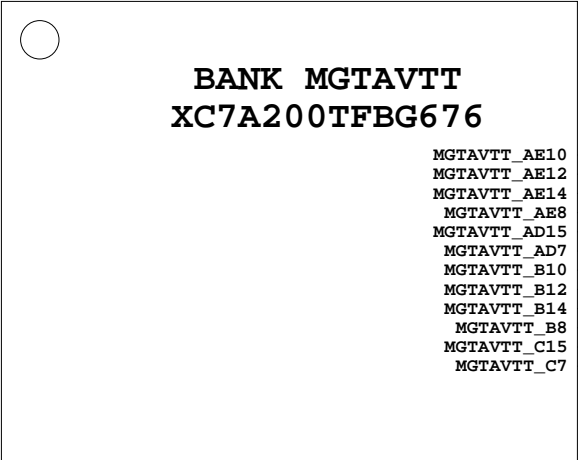
U1

SOC\_IRON\_FG676



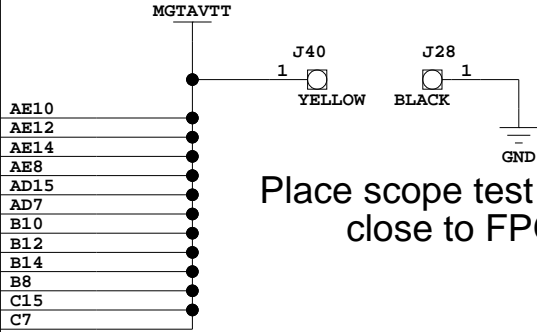
Place scope test points  
close to FPGA

SOC\_IRON\_FG676

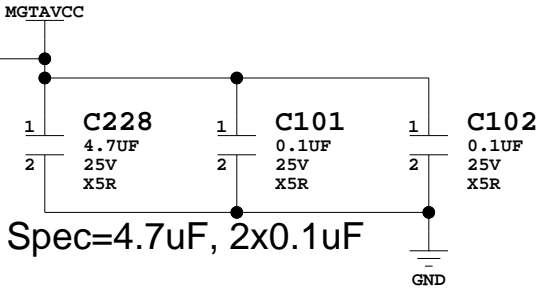


U1

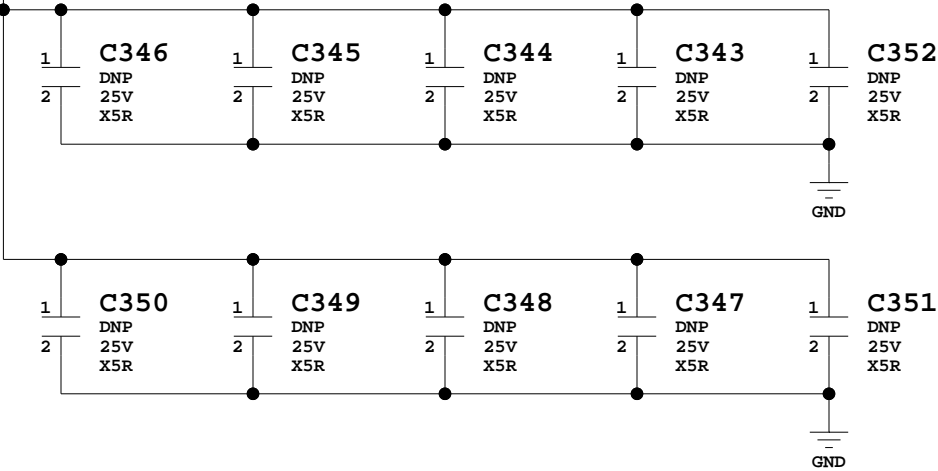
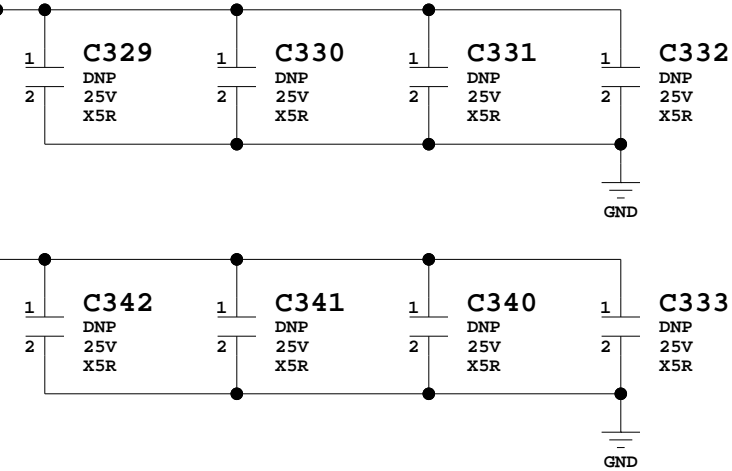
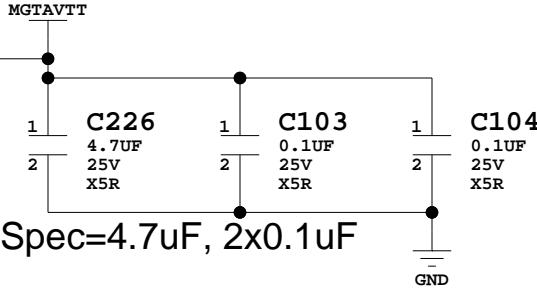
SOC\_IRON\_FG676



Place scope test points  
close to FPGA



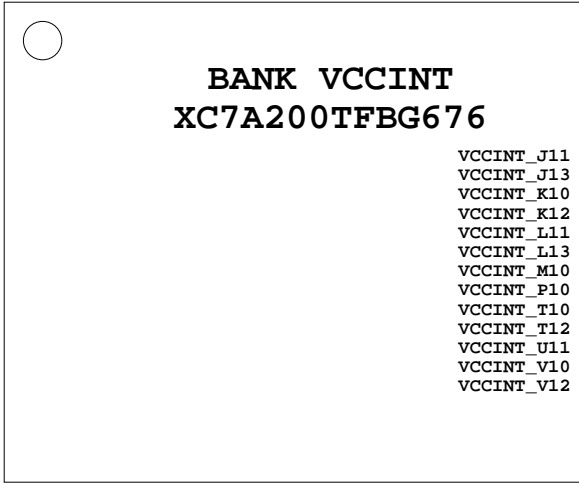
Place MGT 0.1uF caps within  
the FPGA via field on the bottom  
of the board, one for each  
MGT power pin/GND pin pair



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD MGT PWR. BANKS AVCC and AVTT	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 31 of 51	Drawn By DN

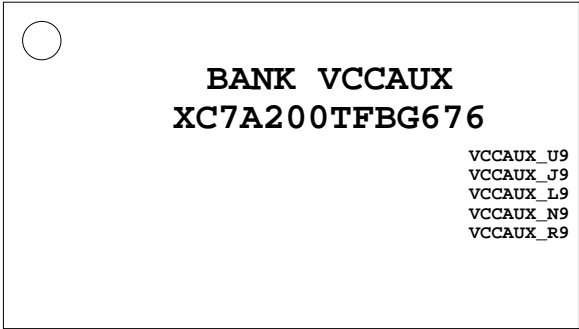
SOC\_IRON\_FG676



U1

SOC\_IRON\_FG676

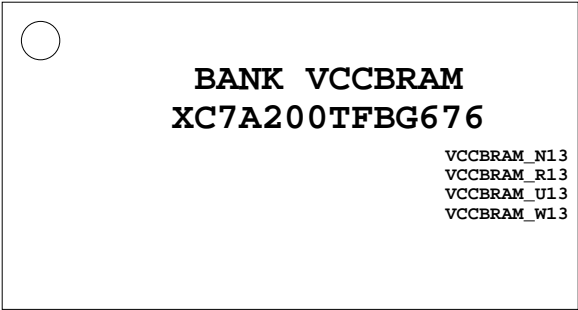
SOC\_IRON\_FG676



U1

SOC\_IRON\_FG676

SOC\_IRON\_FG676

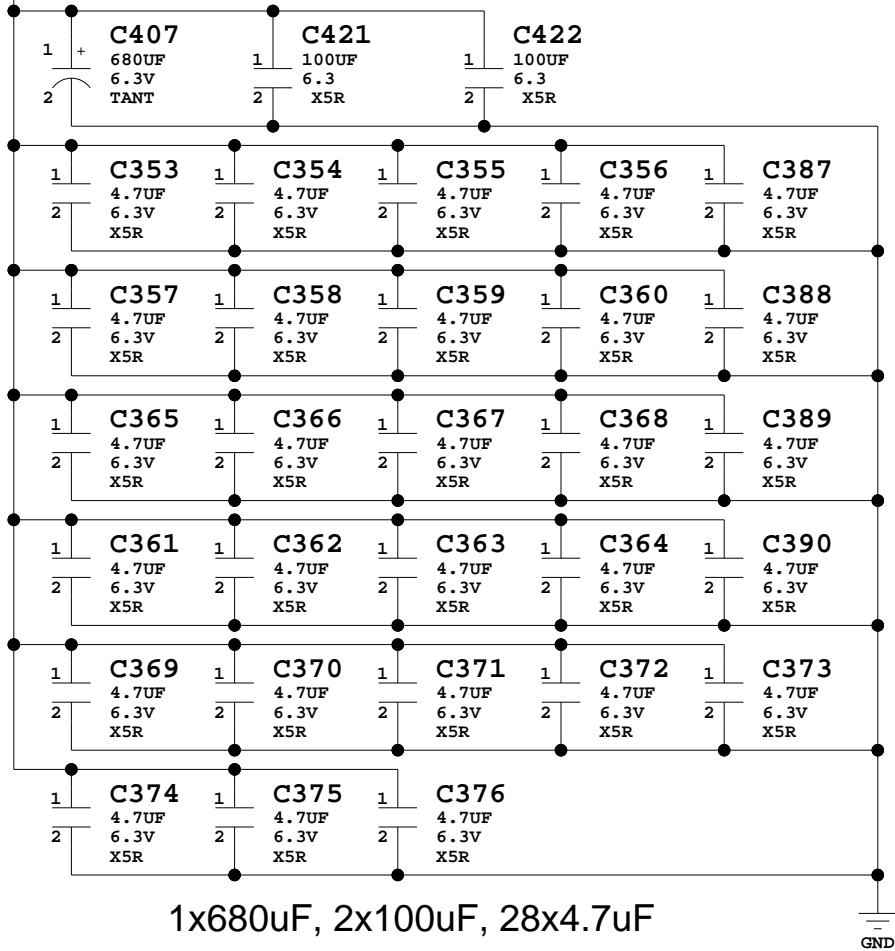


U1

SOC\_IRON\_FG676

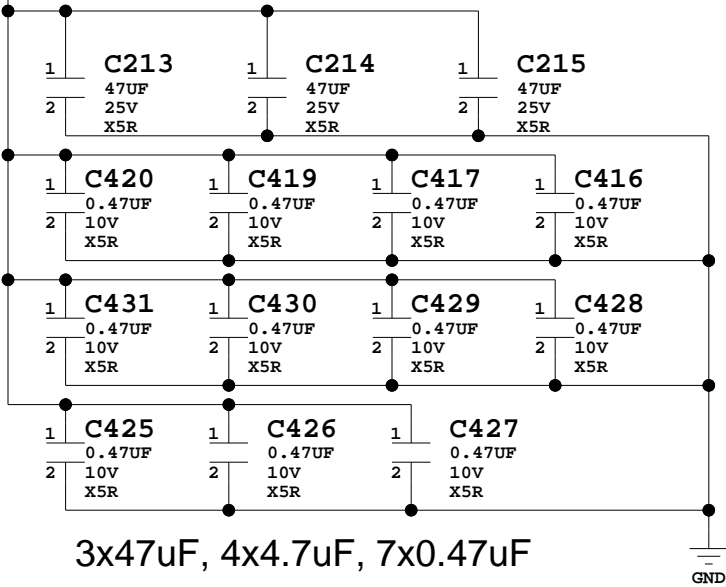
VCCINT

## VCCINT



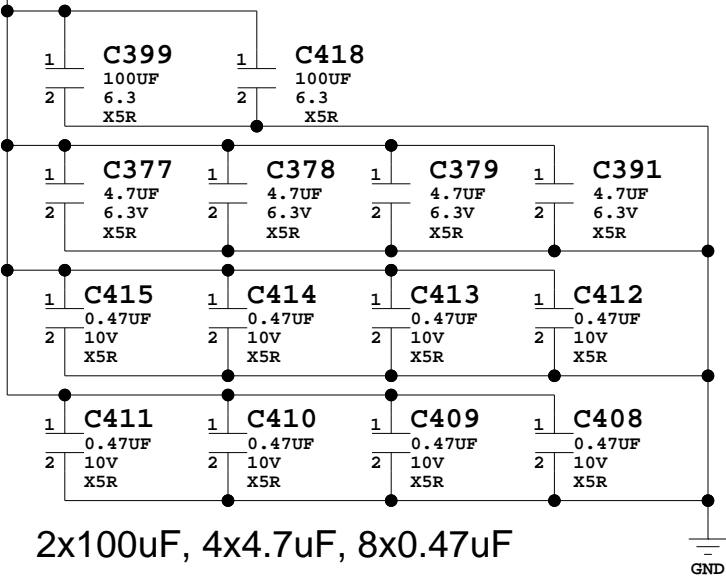
VCCAUX

## VCCAUX



VCCBRAM

## VCCBRAM



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
FPGA CORE PWR. BANKS

Date: 9-20-2012\_14:39

Ver: 1.0

Sheet Size: B

Rev: 01

Sheet

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51

Drawn By

DN

SOC\_IRON\_FG676

BANK GND  
XC7A200TFBG676

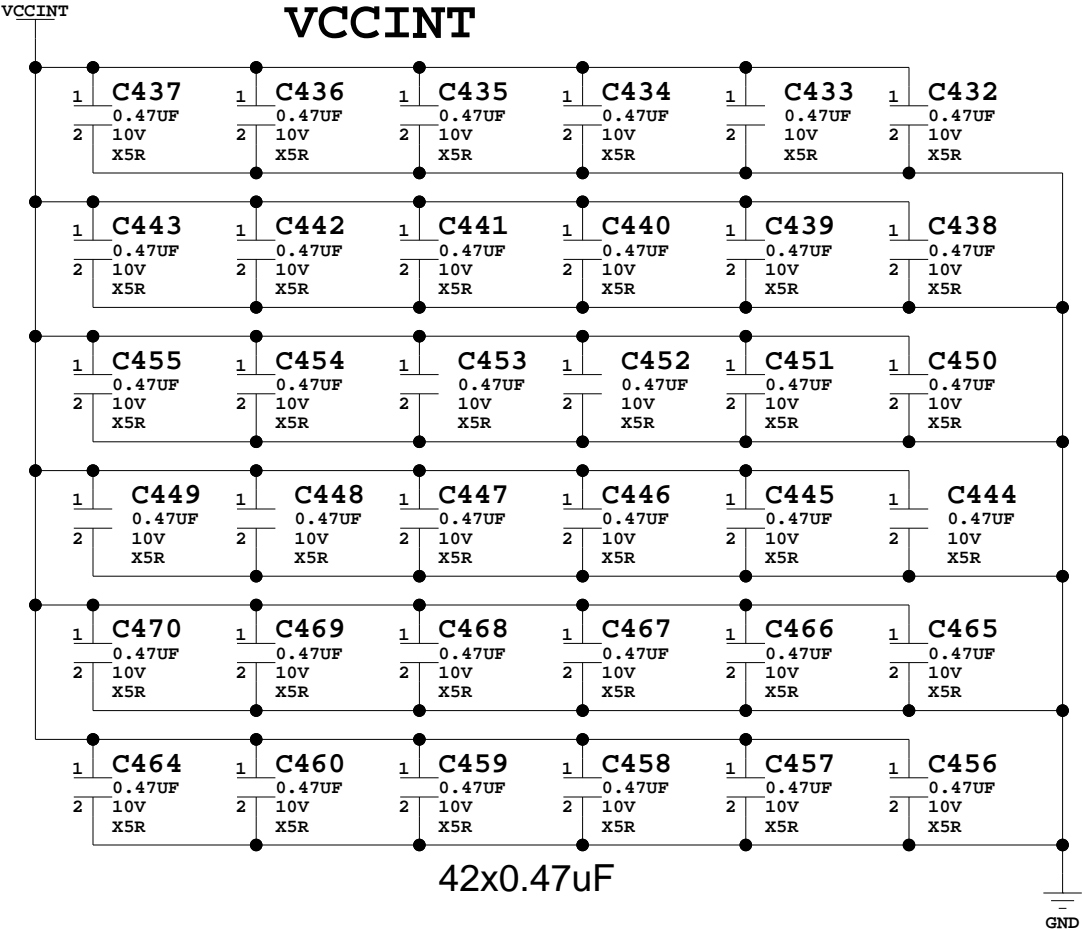
K19  
P7  
AA26  
A6  
A8  
A10  
A12  
A16  
AA6  
A26  
AA14  
AA16  
A14  
AA9  
AB8  
AB9  
AB10  
AB3  
AB14  
AB23  
AC7  
AB12  
AC15  
AD6  
AD9  
AC20  
AD16  
AE4  
AD11  
AD13  
AE6  
AE15  
AF6  
AF8  
AE24  
AF1  
AF12  
AF14  
AF16  
AF21  
AF10  
B6  
B15  
B16  
B3  
B23  
C9  
C6  
C13  
C11  
C16  
T11  
C20  
D7  
D15  
D17  
V5  
E7  
E8

GND\_K19  
GND\_P7  
GND\_AA26  
GND\_A6  
GND\_A8  
GND\_A10  
GND\_A12  
GND\_A16  
GND\_AA6  
GND\_A26  
GND\_AA14  
GND\_AA16  
GND\_A14  
GND\_AA9  
GND\_AB8  
GND\_AB9  
GND\_AB10  
GND\_AB3  
GND\_AB14  
GND\_AB23  
GND\_AC7  
GND\_AB12  
GND\_AC15  
GND\_AD6  
GND\_AD9  
GND\_AC20  
GND\_AD16  
GND\_AE4  
GND\_AD11  
GND\_AD13  
GND\_AE6  
GND\_AE15  
GND\_AF6  
GND\_AF8  
GND\_AE24  
GND\_AF1  
GND\_AF12  
GND\_AF14  
GND\_AF16  
GND\_AF21  
GND\_AF10  
GND\_B6  
GND\_B15  
GND\_B16  
GND\_B3  
GND\_B23  
GND\_C9  
GND\_C6  
GND\_C13  
GND\_C11  
GND\_C16  
GND\_T11  
GND\_C20  
GND\_D7  
GND\_D15  
GND\_D17  
GND\_V5  
GND\_E7  
GND\_E8

E4  
E9  
E24  
F9  
F14  
F21  
E10  
E12  
E14  
E15  
G11  
G12  
G10  
H5  
H25  
J2  
J12  
G13  
G18  
K11  
K13  
J22  
K9  
L12  
L16  
L26  
M3  
M9  
L6  
L10  
M13  
N20  
F1  
M23  
N10  
R4  
R10  
P9  
P13  
T1  
T9  
R24  
U8  
U10  
U12  
U18  
T13  
P17  
T21  
V15  
V25  
W2  
V13  
Y10  
Y11  
Y12  
Y13  
Y19  
W12  
W22

GND\_E4  
GND\_E9  
GND\_E24  
GND\_F9  
GND\_F14  
GND\_F21  
GND\_E10  
GND\_E12  
GND\_E14  
GND\_E15  
GND\_G11  
GND\_G12  
GND\_G10  
GND\_H5  
GND\_H25  
GND\_J2  
GND\_J12  
GND\_G13  
GND\_G18  
GND\_K11  
GND\_K13  
GND\_J22  
GND\_K9  
GND\_L12  
GND\_L16  
GND\_L26  
GND\_M3  
GND\_M9  
GND\_L6  
GND\_L10  
GND\_M13  
GND\_N20  
GND\_F1  
GND\_M23  
GND\_N10  
GND\_R4  
GND\_R10  
GND\_P9  
GND\_P13  
GND\_T1  
GND\_T9  
GND\_R24  
GND\_U8  
GND\_U10  
GND\_U12  
GND\_U18  
GND\_T13  
GND\_P17  
GND\_T21  
GND\_V15  
GND\_V25  
GND\_W2  
GND\_V13  
GND\_Y10  
GND\_Y11  
GND\_Y12  
GND\_Y13  
GND\_Y19  
GND\_W12  
GND\_W22

VCCINT



42x0.47uF

U1

SOC\_IRON\_FG676



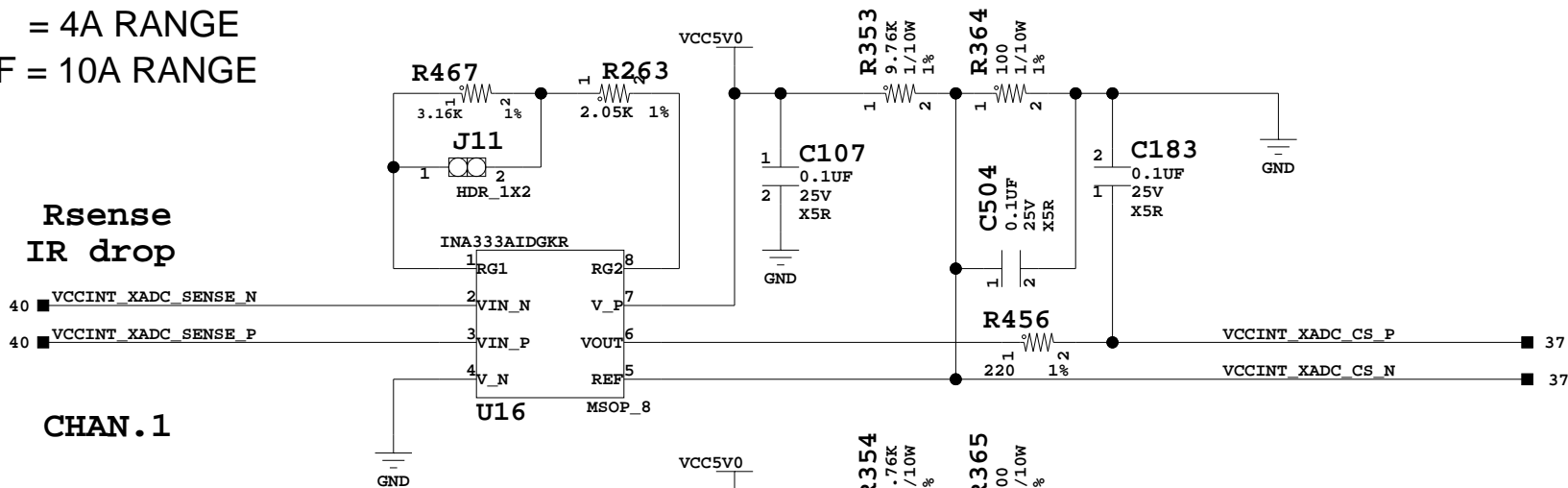
ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FPGA PWR. BANK GND	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 33 of 51	Drawn By DN

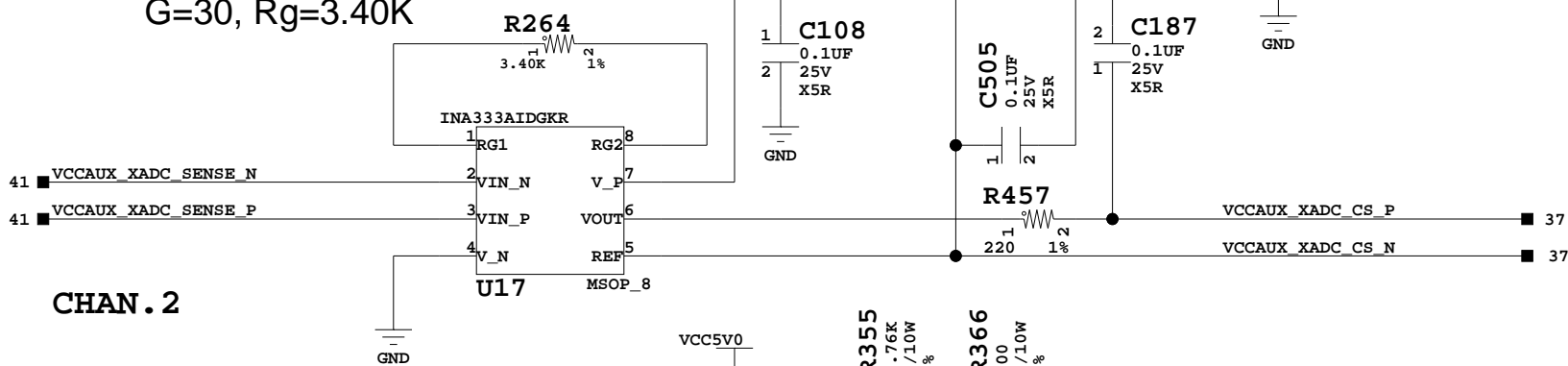
XADC I/F MONITORING CIRCUIT PAGE 1

VCCINT 0A-10A => CS = 0V - 1.009V    G=20, Rg=5.21K  
VCCINT 0A-4A    => CS = 0V - 0.996V    G=50, Rg=2.05K  
J11 ON    = 4A RANGE  
J11 OFF = 10A RANGE

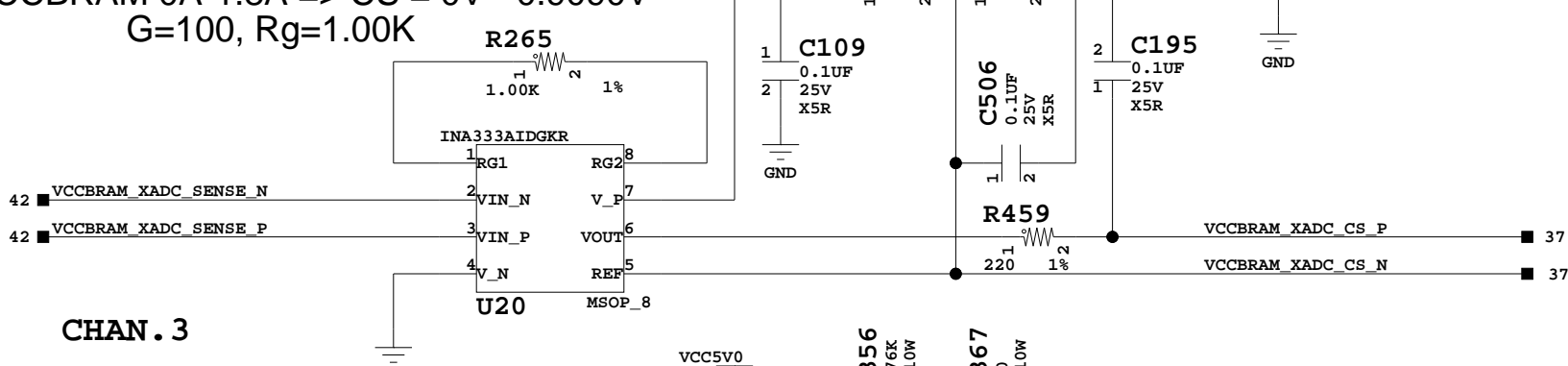
Rsense  
IR drop



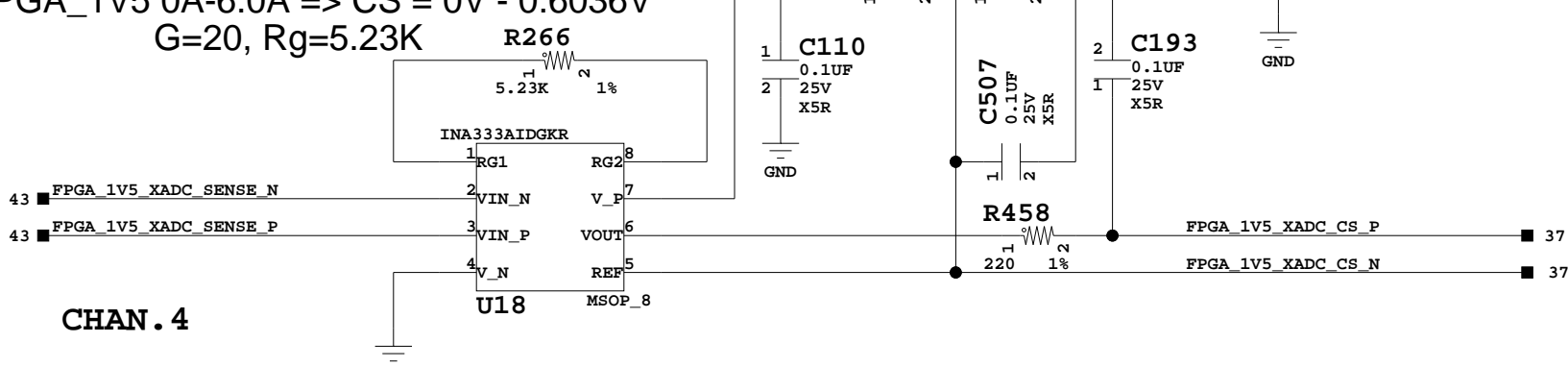
VCCAUX 0A-6.0A => CS = 0V - 0.9124V  
G=30, Rg=3.40K



VCCBRAM 0A-1.8A => CS = 0V - 0.9090V  
G=100, Rg=1.00K

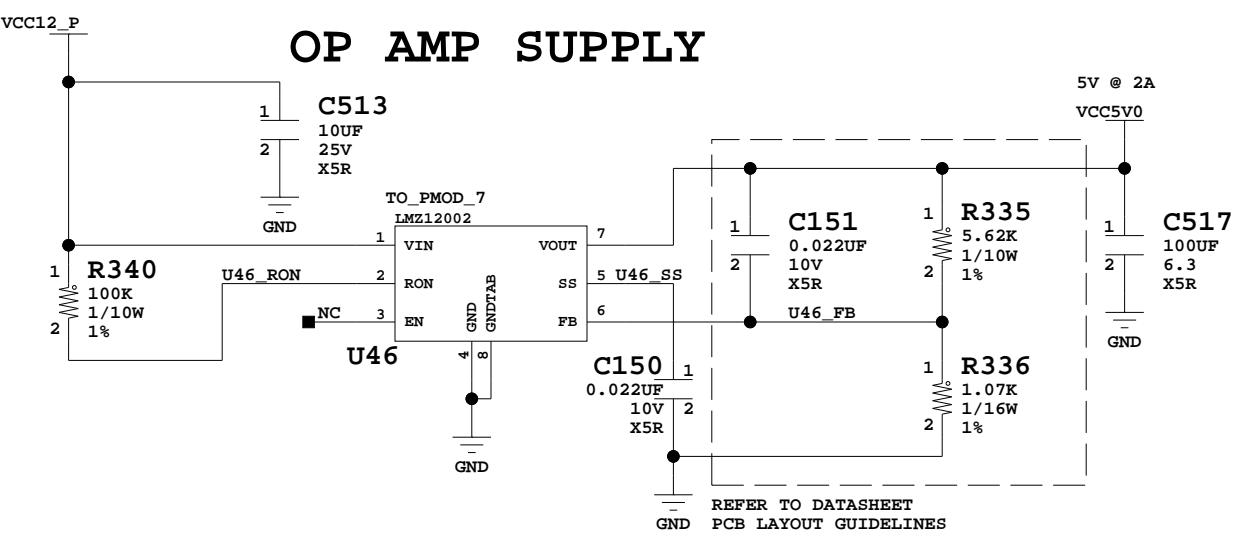


FPGA\_1V5 0A-6.0A => CS = 0V - 0.6036V  
G=20, Rg=5.23K

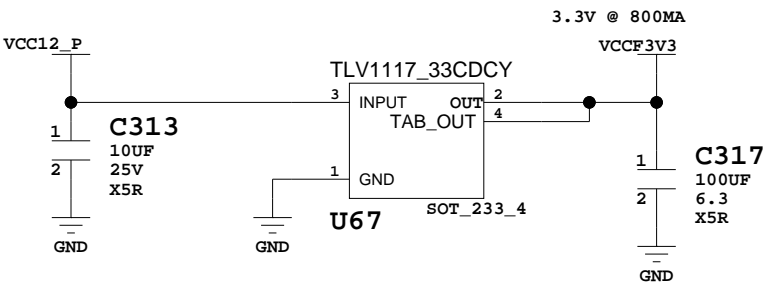


CONTROLLER #1

OP AMP SUPPLY

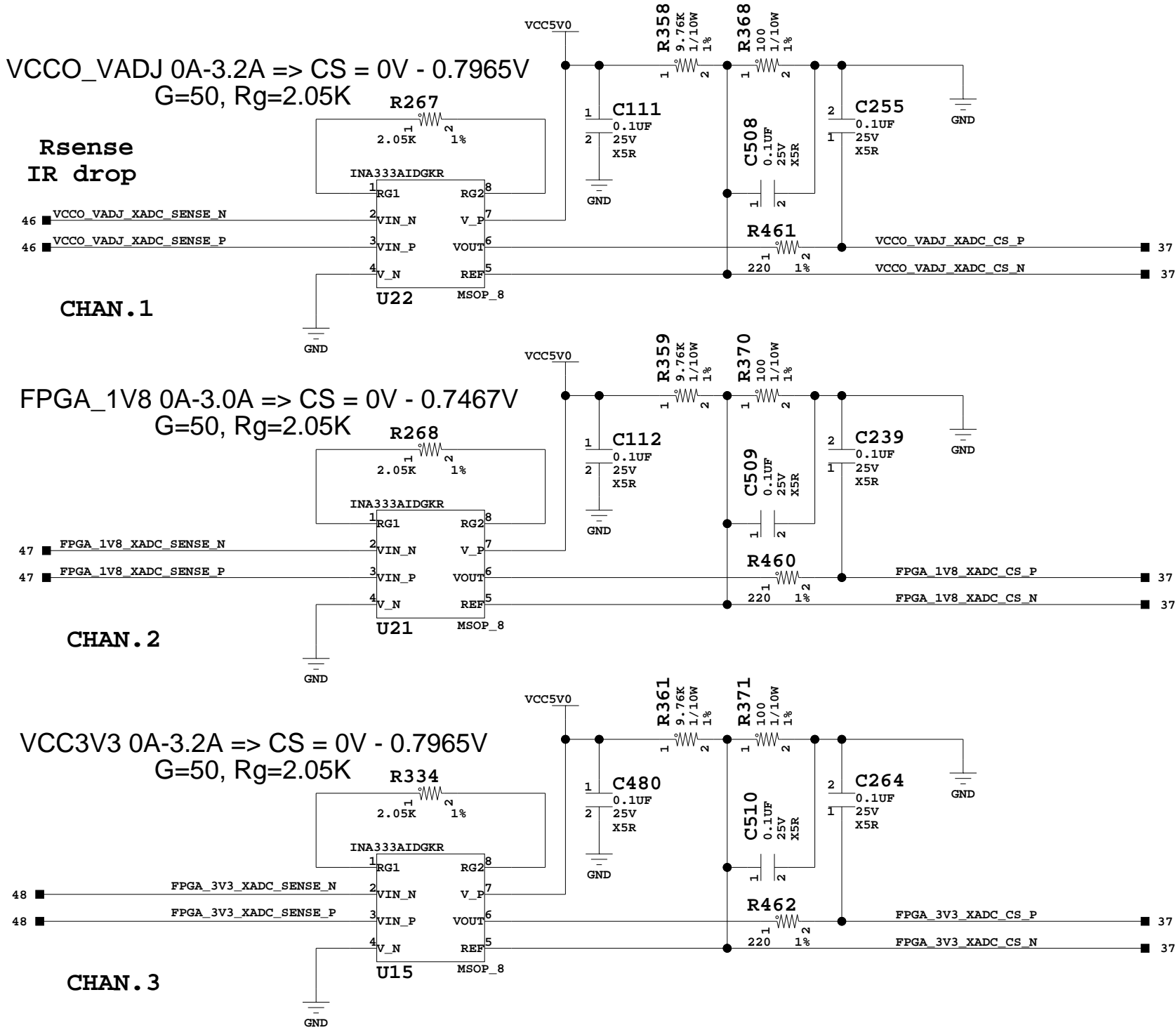


3.3V IMMEDIATE ON FIXED SUPPLY



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. OP AMPS	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 34 of 51	Drawn By DN



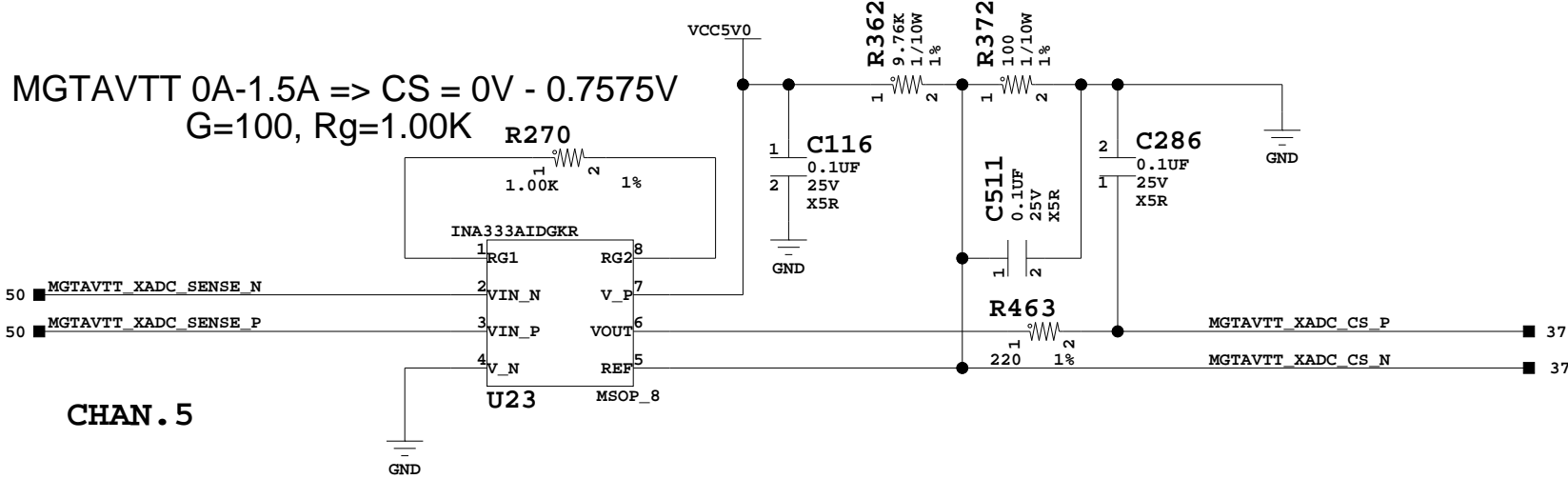
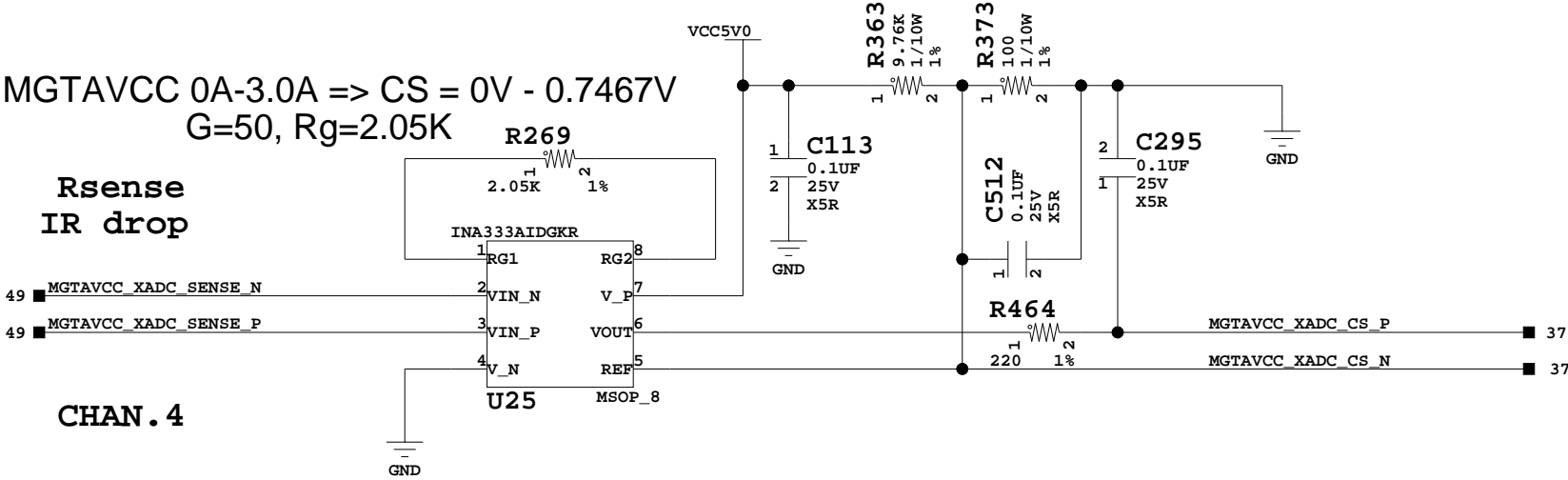
ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
XADC MON. OP AMPS

Date: 9-20-2012\_14:39 Ver: 1.0

Sheet Size: B Rev: 01

Sheet 35 of 51 Drawn By DN



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

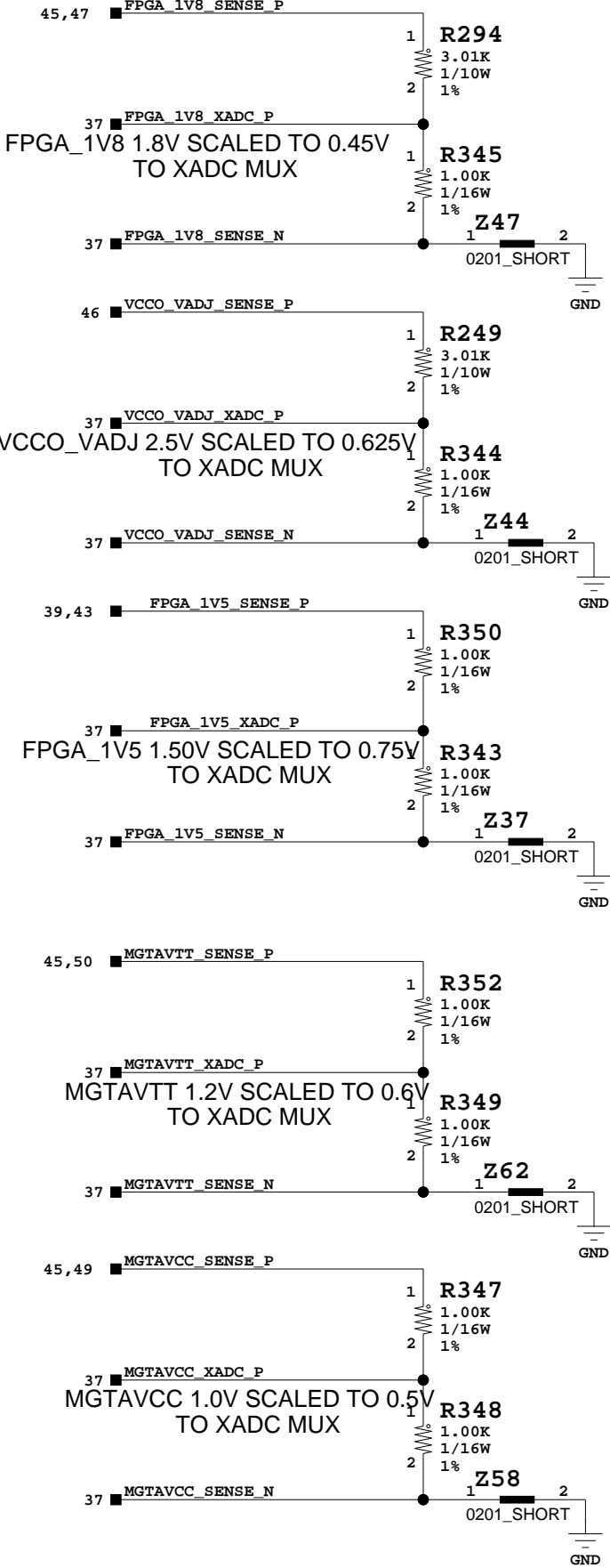
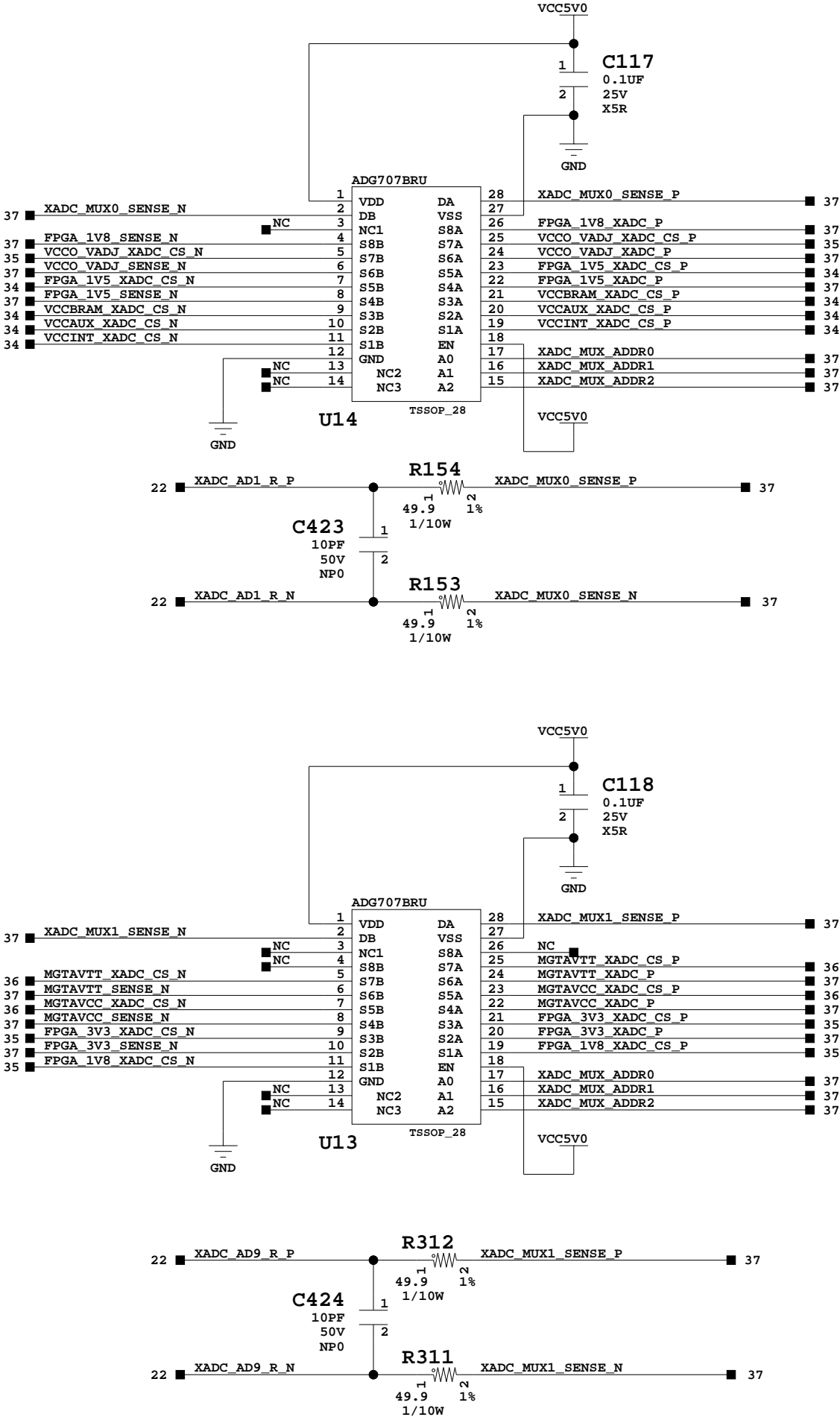
Title: SCHEM, ROHS COMPLIANT  
AC701 EVALUATION BOARD  
XADC MON. OP AMPS


Date: 9-20-2012\_14:39 Ver: 1.0

Sheet Size: B Rev: 01

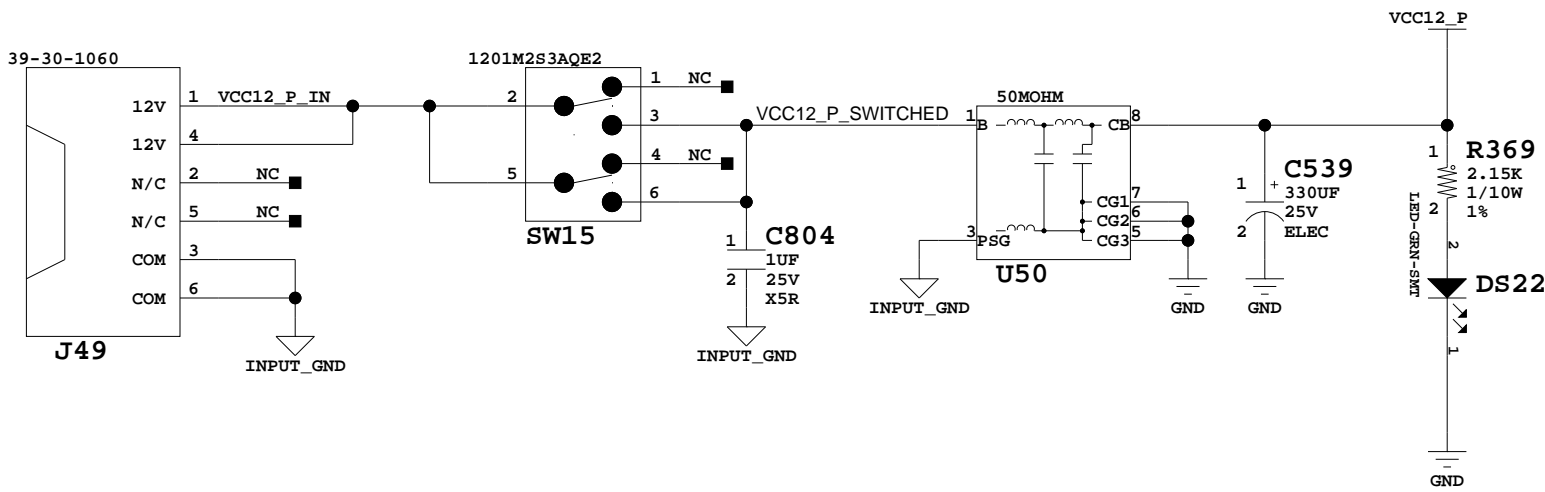
Sheet 36 of 51 Drawn By DN

XADC I/F MONITORING CIRCUIT PAGE 4



		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. 2X MUX	
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	37 of 51	Drawn By	DN

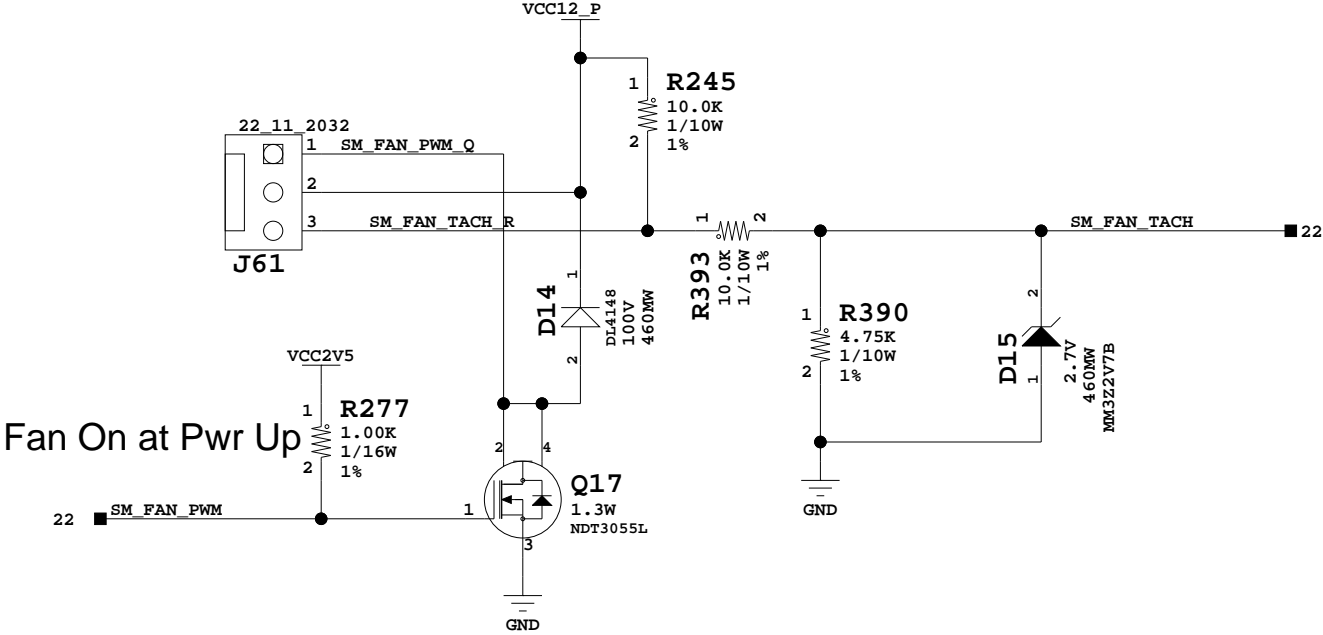
POWER SYSTEM SCHEMATIC STARTS HERE



AC701 POWER SYSTEM CONFIGURATION

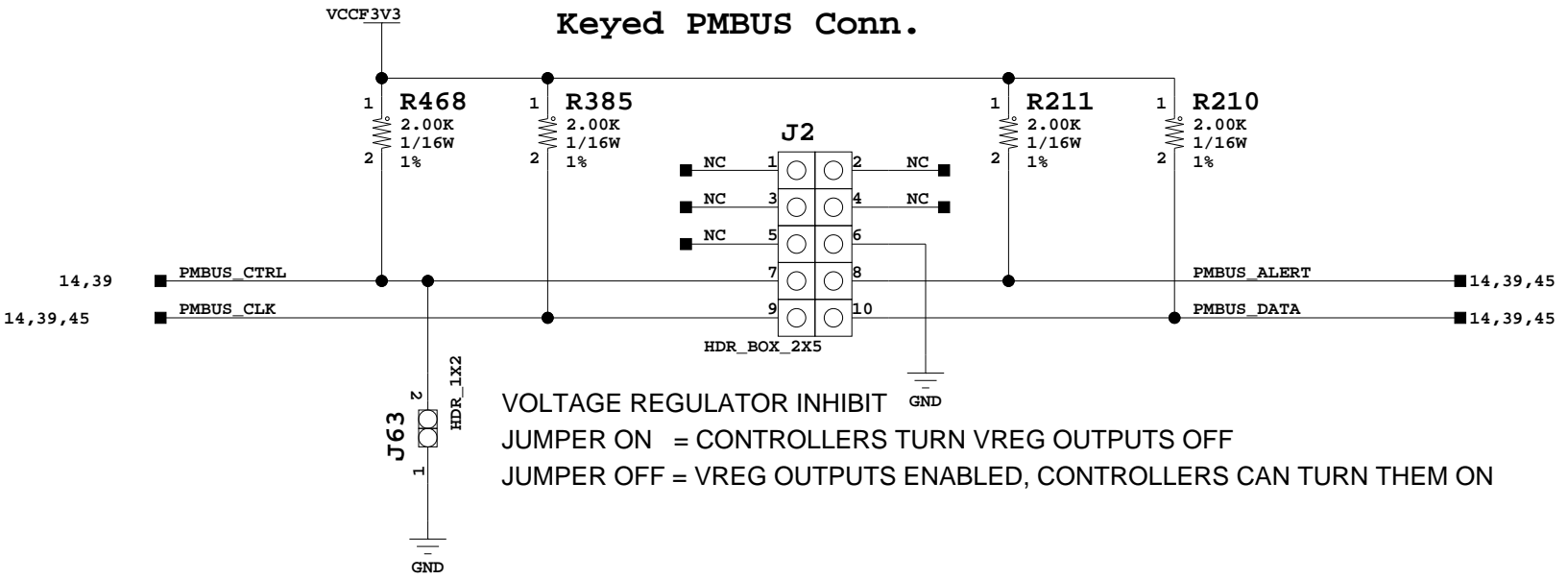
CTLR REF	PAGE	PMBUS ADDR/RAIL	NET NAME	VOLTAGE	VREG-TYPE	MAX I
#1 U8	PG 39 101	UCD90120A	4 RAILS:			
	PG 40 101	1	VCCINT	1.0V	LMZ12010 U49	10A
	PG 41 101	2	VCCAUX	1.8V	TPS84621 U53	6A
	PG 42 101	3	VCCBRAM	1.0V	TPS84320 U54	3A
	PG 43 101	4	FPGA_1V5	1.5V	TPS84621 U55	6A
#2 U9	PG 45 102	UCD90120A	5 RAILS:			
	PG 46 102	1	VCCO_VADJ	2.5V	TPS84621 U56	6A
	PG 47 102	2	FPGA_1V8	1.8V	TPS84320 U57	3A
	PG 48 102	3	FPGA_3V3	3.3V	TPS84621 U58	6A
	PG 49 102	4	MGTAVCC	1.0V	TPS84320 U59	3A
	PG 49 102	5	MGTAVTT	1.2V	TPS84320 U60	3A

Keyed Fan Header



Fan On at Pwr Up

Keyed PMBUS Conn.

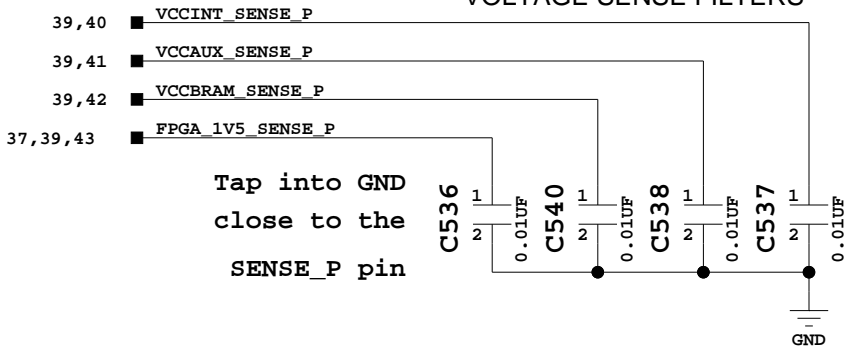


VOLTAGE REGULATOR INHIBIT  
JUMPER ON = CONTROLLERS TURN VREG OUTPUTS OFF  
JUMPER OFF = VREG OUTPUTS ENABLED, CONTROLLERS CAN TURN THEM ON

Power Connector and switch, PMBus Header

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD POWER CONN.,SWITCH,PMBUS HEADER,FAN CONTROL	
Date:	12-3-2012_12:58	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	38 of 51	Drawn By	DN

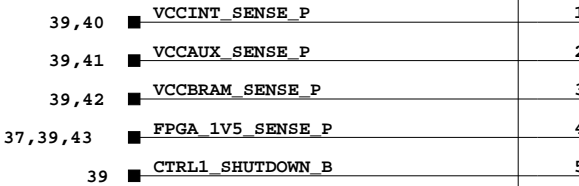
VOLTAGE SENSE FILTERS



R375  
10.0K  
1/10W  
1%

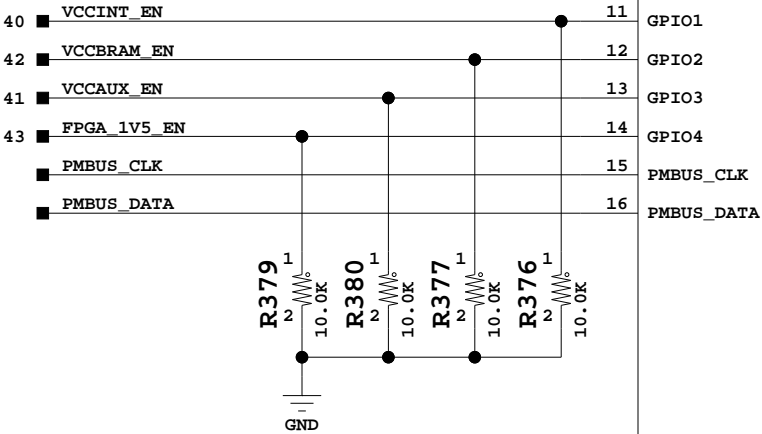
C553  
1000PF  
50V  
X7R

VOLTAGE SENSE

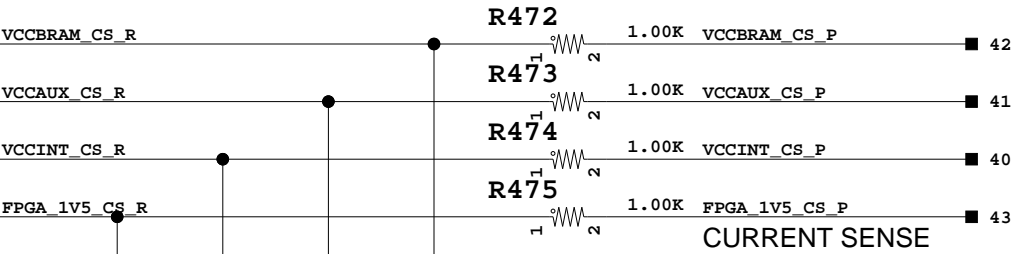
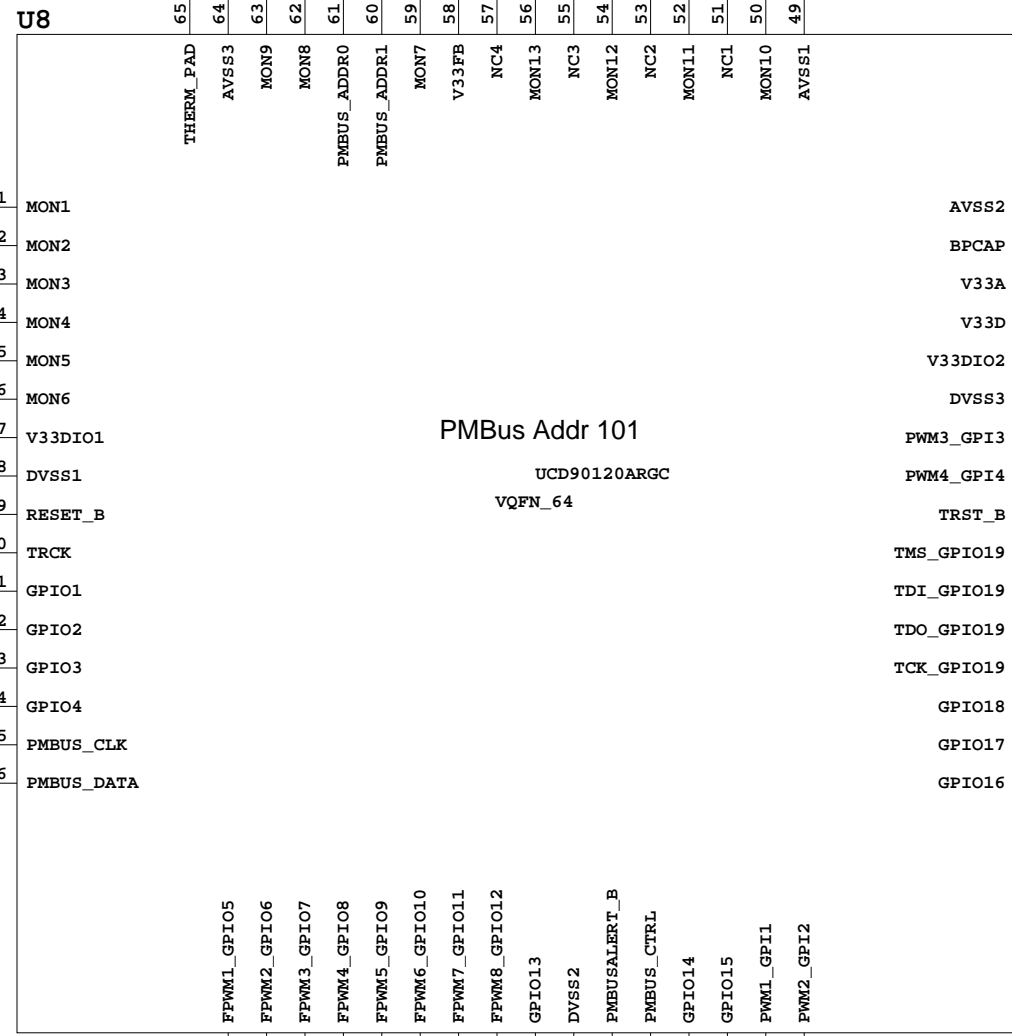
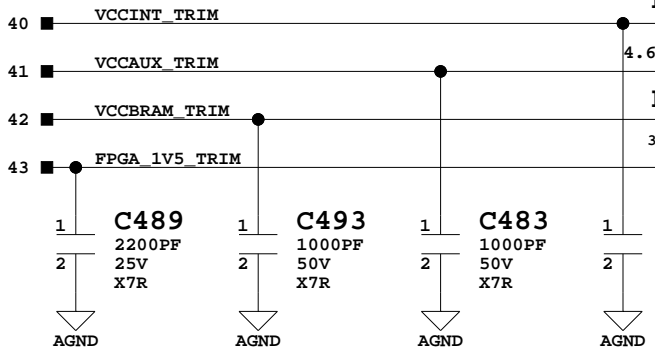


C516  
0.1uF  
25V  
X5R

RAIL ENABLES

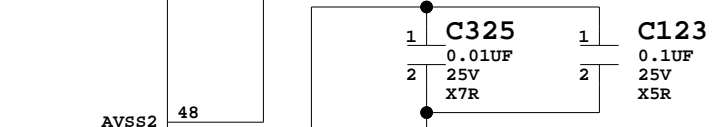


MARGIN TRIM

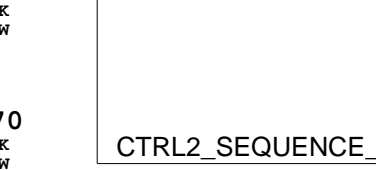
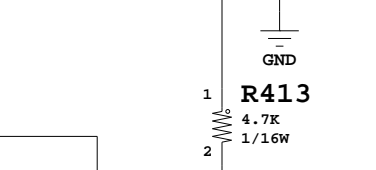
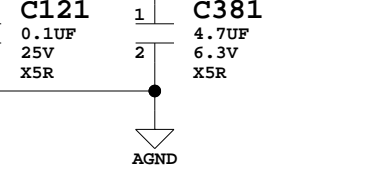
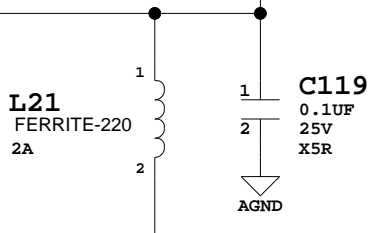
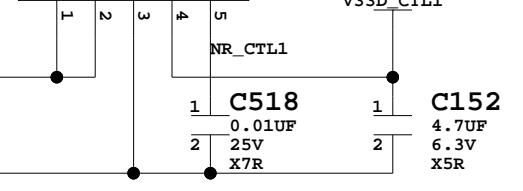
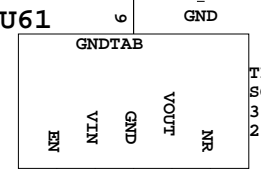
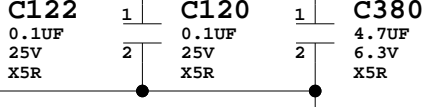


CURRENT SENSE FILTERS

Tap into GND  
close to the  
SENSE\_P pin



PLACE CLOSE TO Ux PINS44,45



CORE,VCCO/DDR3 DIMM POWER



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

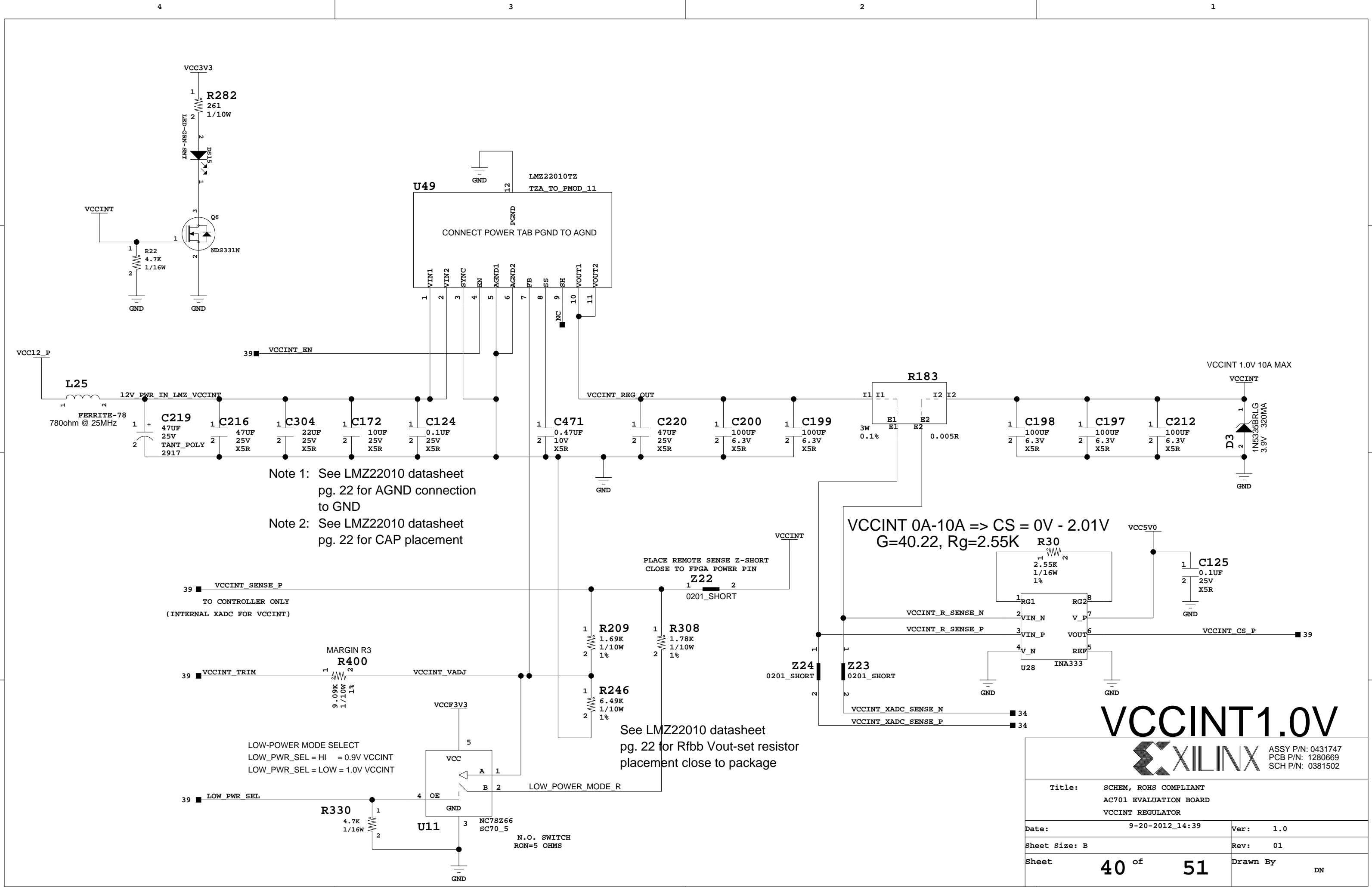
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Date: 10-24-2012_11:45	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 39 of 51	Drawn By DN

CTRL1 SHUTDOWN ENABLE  
HI = CLOSE SWITCH, ENABLE S/D  
LO = OPEN SWITCH, INHIBIT S/D

N.O. SWITCH  
RON=5 OHMS

NC7SZ66  
SC70\_5

R483  
4.7K  
1/16W



Note 1: See LMZ22010 datasheet  
pg. 22 for AGND connection  
to GND

Note 2: See LMZ22010 datasheet  
pg. 22 for CAP placement

VCCINT 0A-10A => CS = 0V - 2.01V  
G=40.22, Rg=2.55K

See LMZ22010 datasheet  
pg. 22 for Rfbb Vout-set resistor  
placement close to package

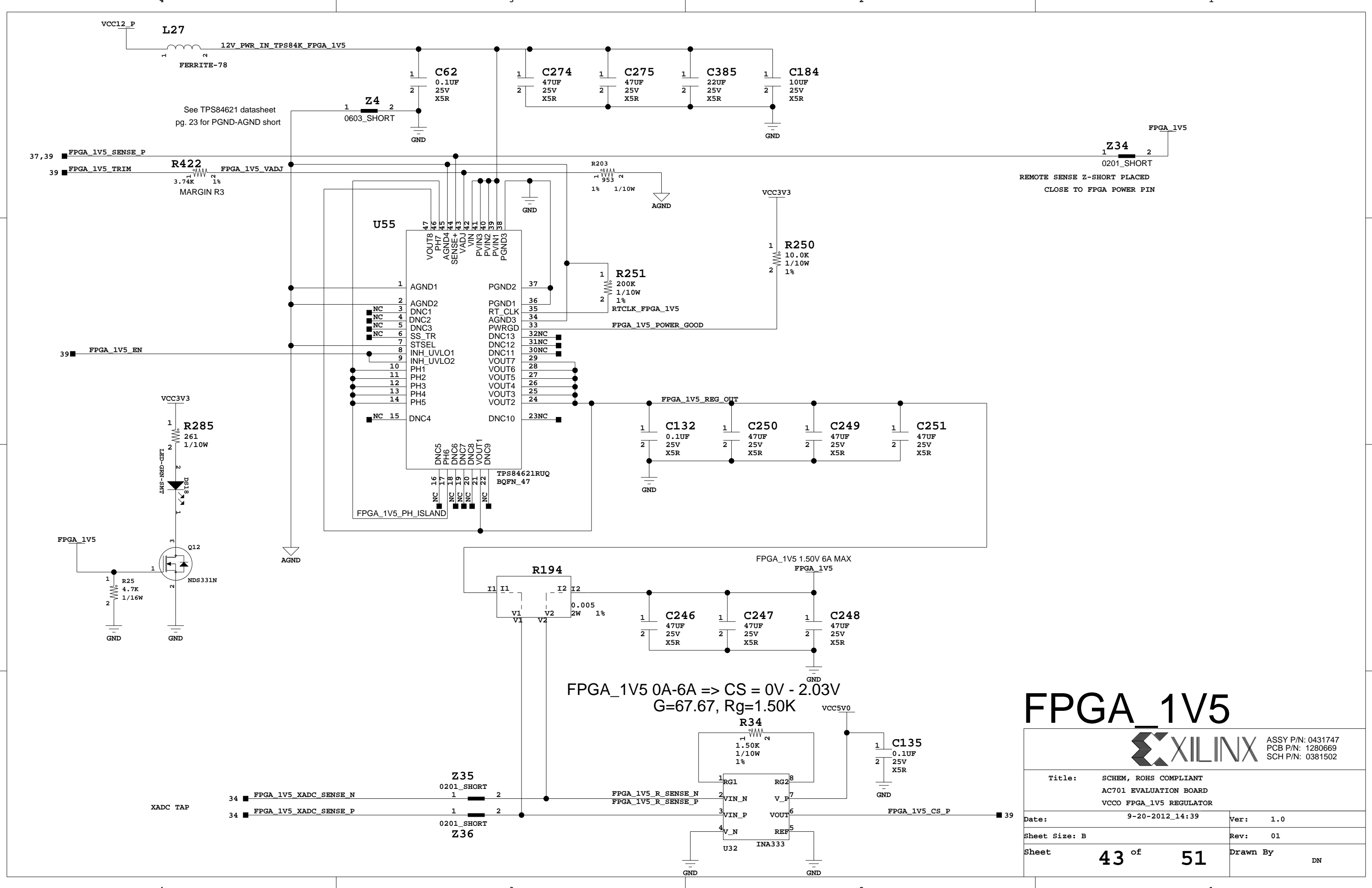
# VCCINT1.0V

**XILINX**  
ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCINT REGULATOR		
Date: 9-20-2012_14:39	Ver: 1.0	
Sheet Size: B	Rev: 01	
Sheet 40 of 51	Drawn By DN	





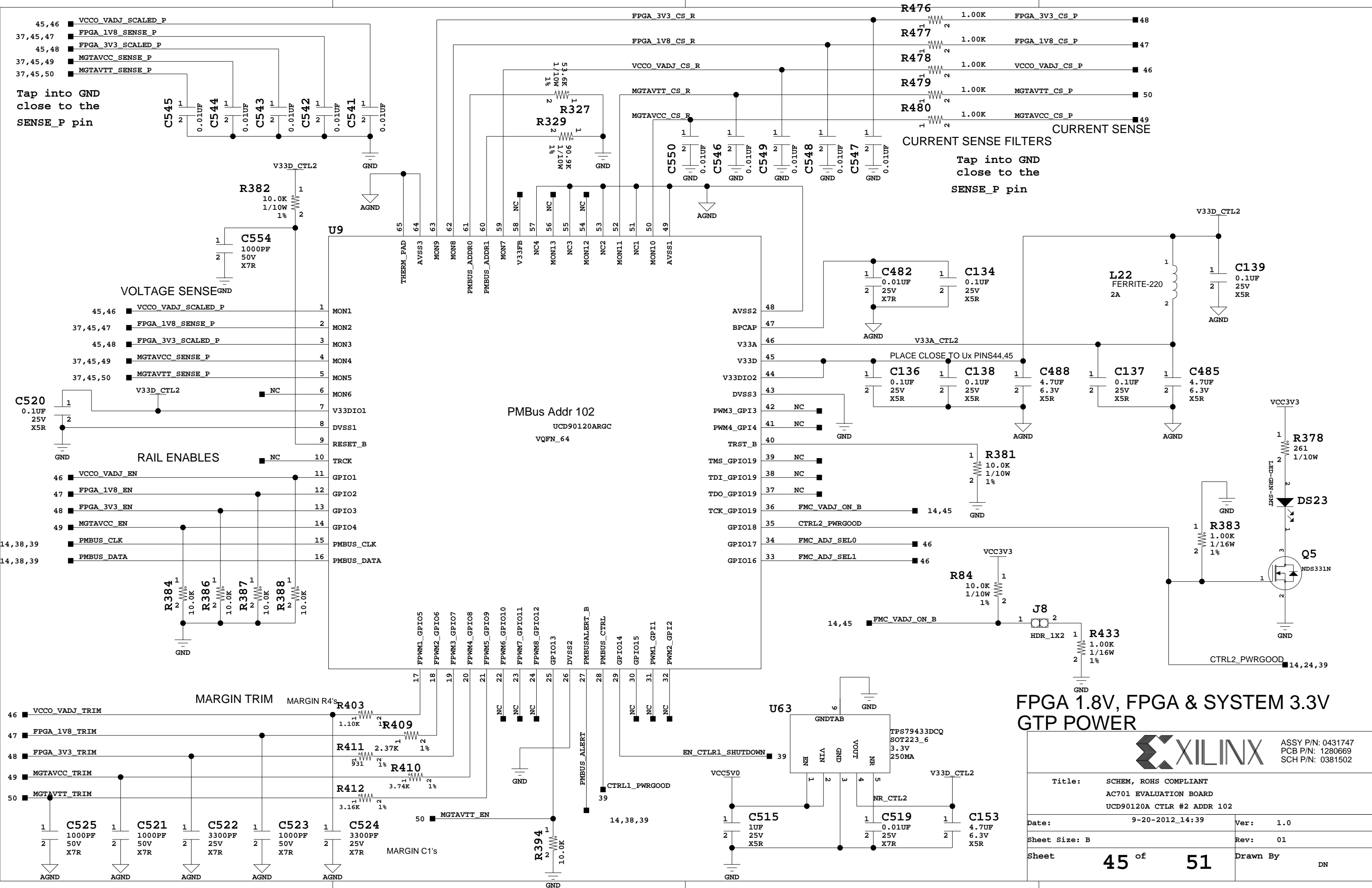


# FPGA\_1V5

ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCO FPGA_1V5 REGULATOR	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 43 of 51	Drawn By DN



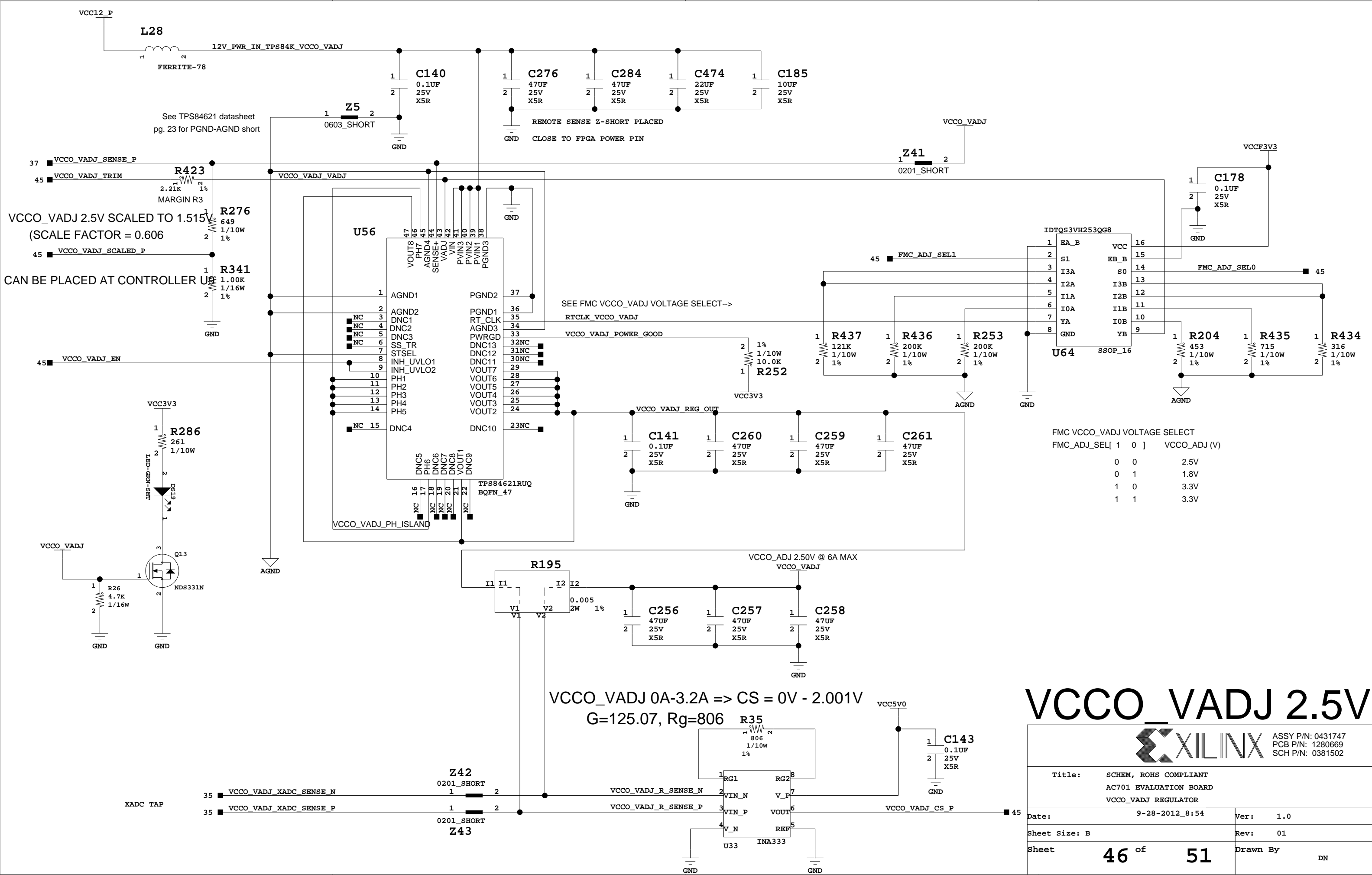


# FPGA 1.8V, FPGA & SYSTEM 3.3V GTP POWER



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD UCD90120A CTRLR #2 ADDR 102	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 45 of 51	Drawn By DN

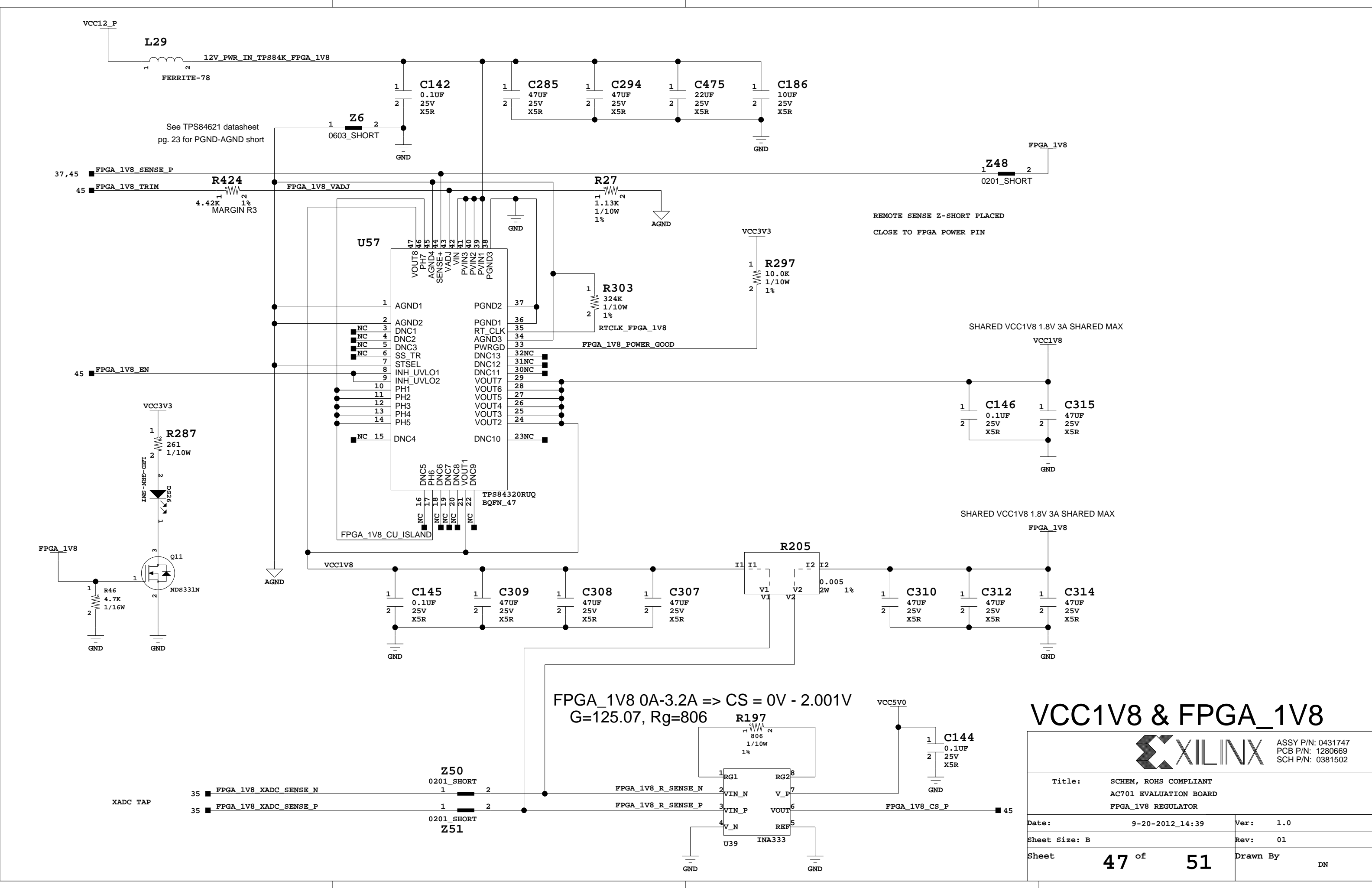


# VCCO\_VADJ 2.5V



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCO_VADJ REGULATOR	
Date: 9-28-2012_8:54	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 46 of 51	Drawn By DN

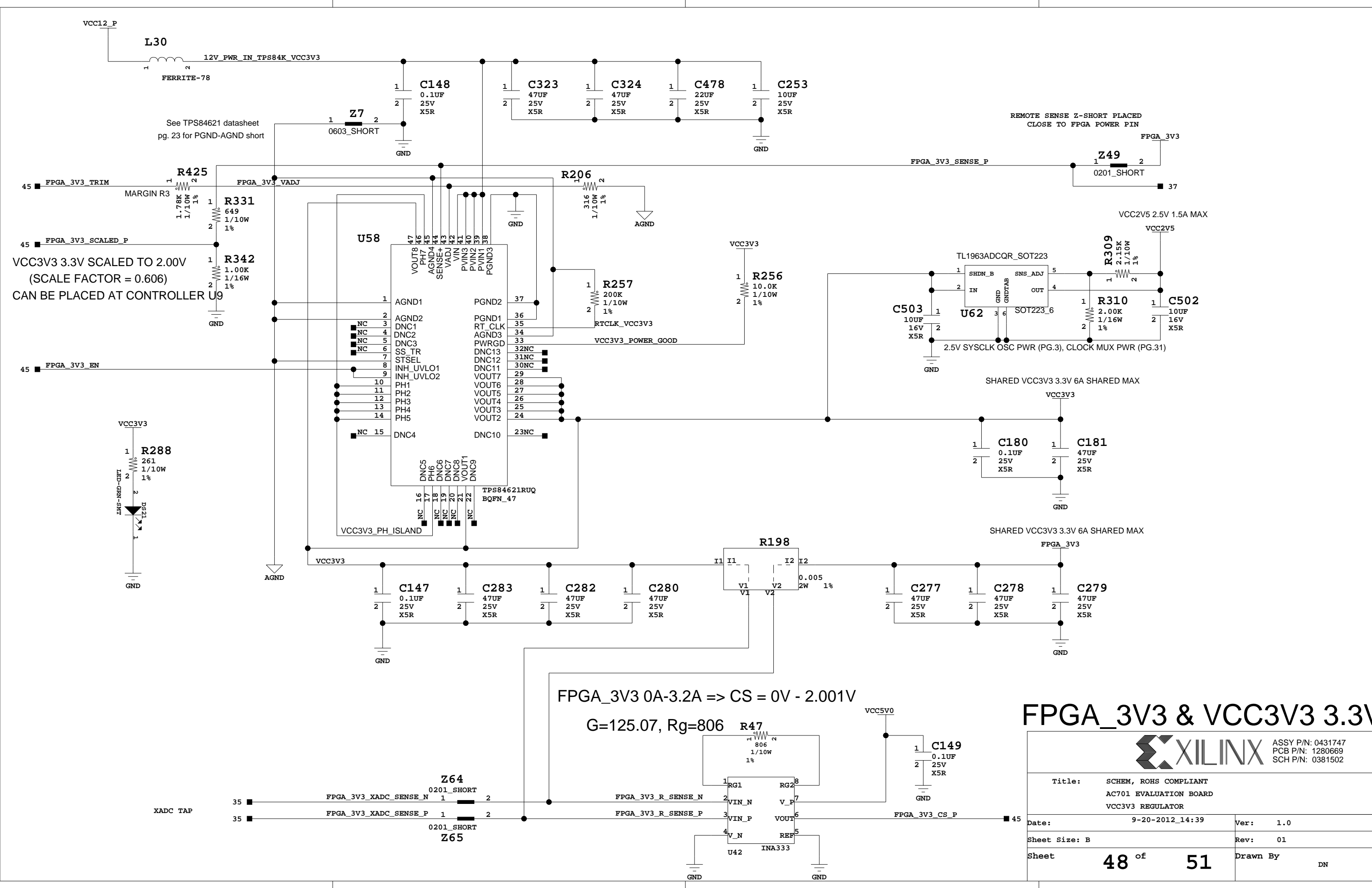


# VCC1V8 & FPGA\_1V8




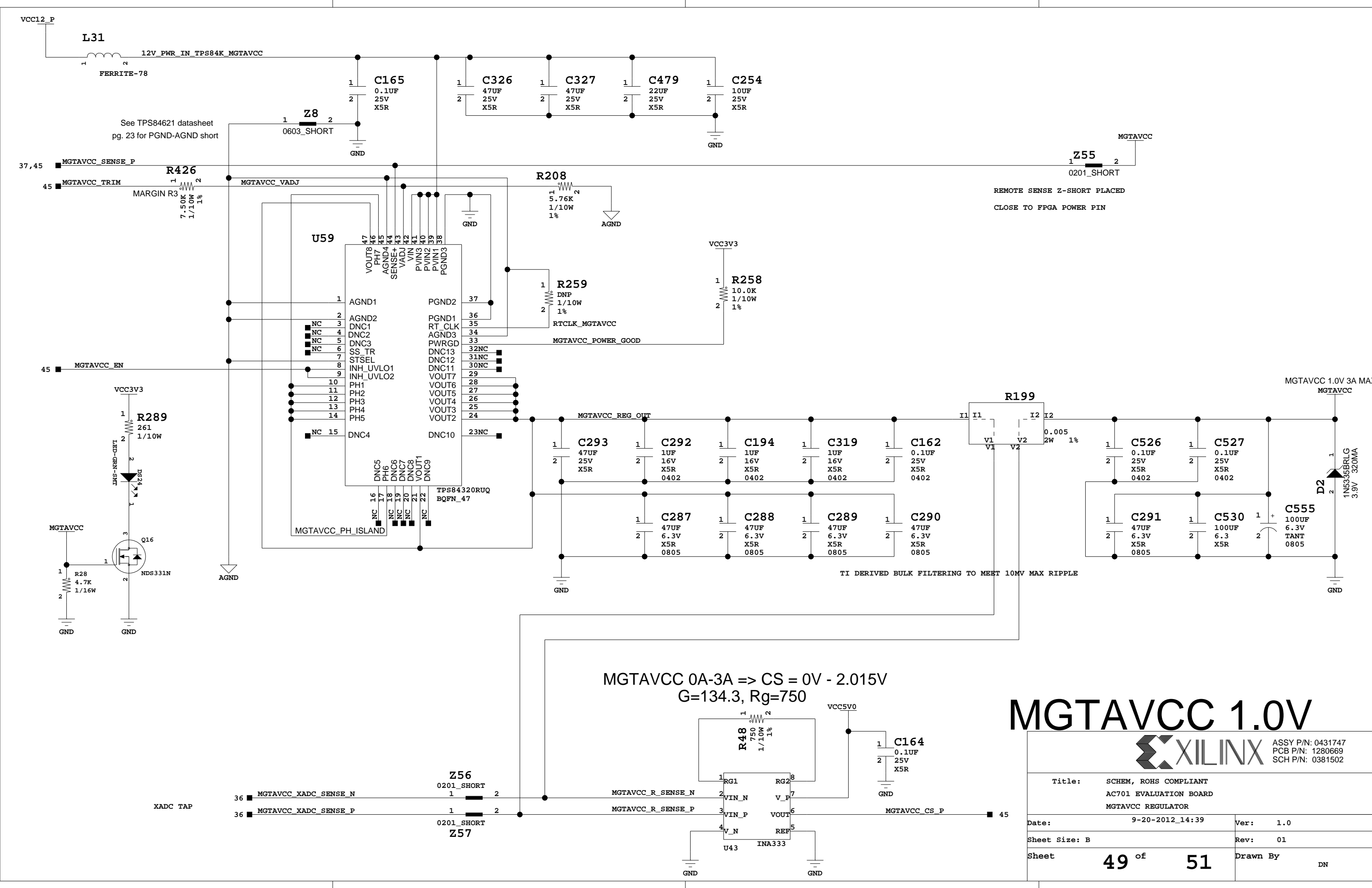
ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FPGA_1V8 REGULATOR	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
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# FPGA\_3V3 & VCC3V3 3.3V

		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCC3V3 REGULATOR	
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	48 of 51	Drawn By	DN



MGTAVCC 0A-3A => CS = 0V - 2.015V  
G=134.3, Rg=750

# MGTAVCC 1.0V



ASSY P/N: 0431747  
PCB P/N: 1280669  
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD MGTAVCC REGULATOR	
Date: 9-20-2012_14:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 49 of 51	Drawn By DN

