

AC701 EVALUATION BOARD HW-A7-AC701
(XC7A200T-FBG676)

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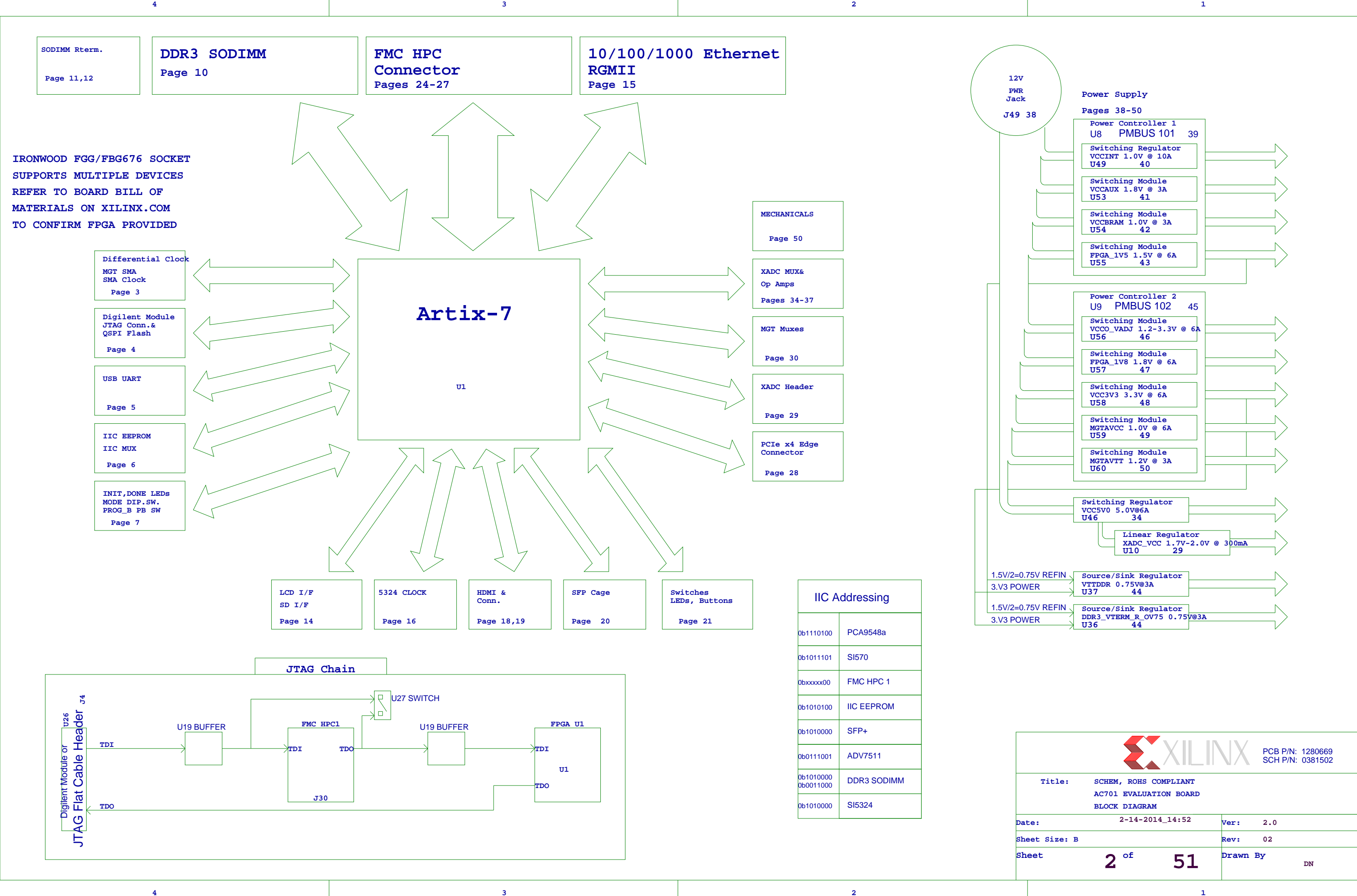
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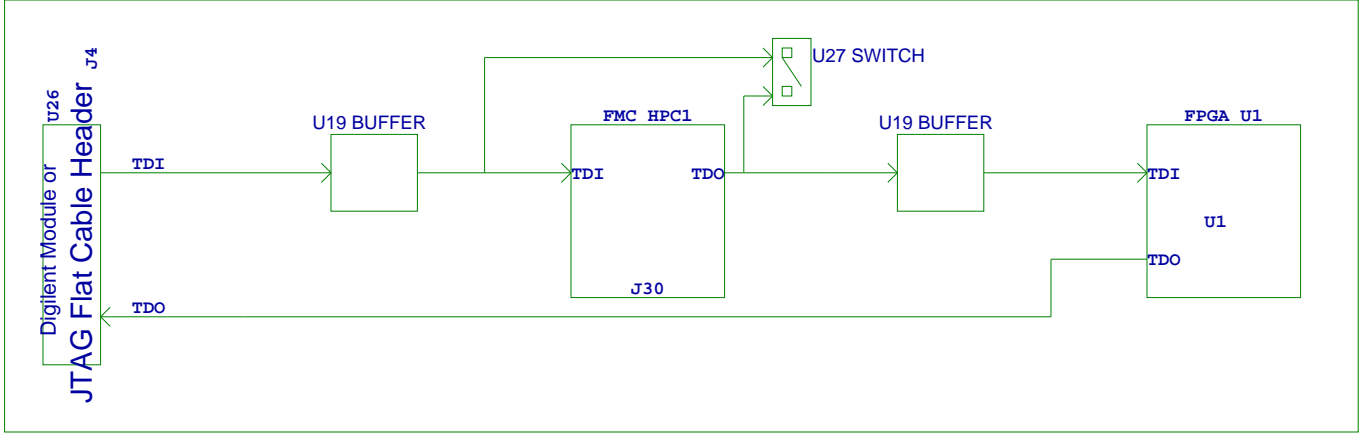
REV. 2.0

		PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DISCLAIMER	
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	1 of 51	Drawn By	DN



IRONWOOD FGG/FBG676 SOCKET
SUPPORTS MULTIPLE DEVICES
REFER TO BOARD BILL OF
MATERIALS ON XILINX.COM
TO CONFIRM FPGA PROVIDED

JTAG Chain



IIC Addressing

0b1110100	PCA9548a
0b1011101	SI570
0bxxxxx00	FMC HPC 1
0b1010100	IIC EEPROM
0b1010000	SFP+
0b0111001	ADV7511
0b1010000 0b0011000	DDR3 SODIMM
0b1010000	SI5324

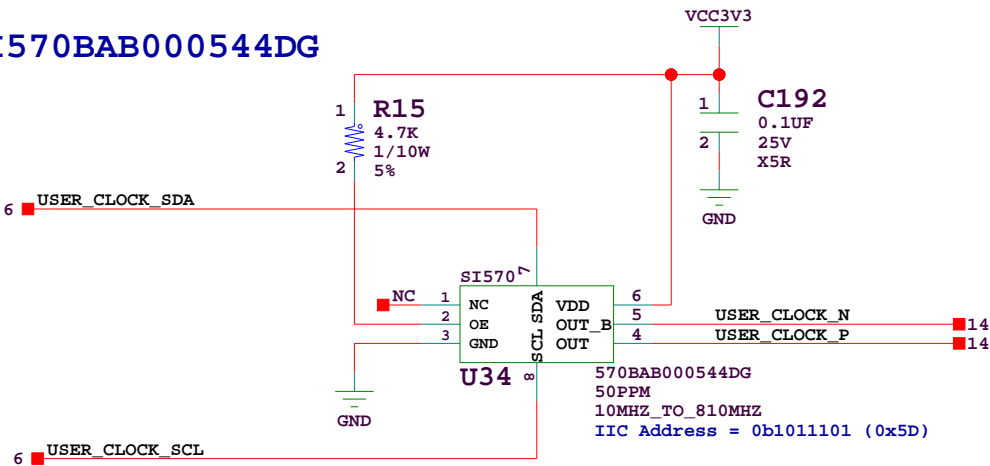


PCB P/N: 1280669
SCH P/N: 0381502

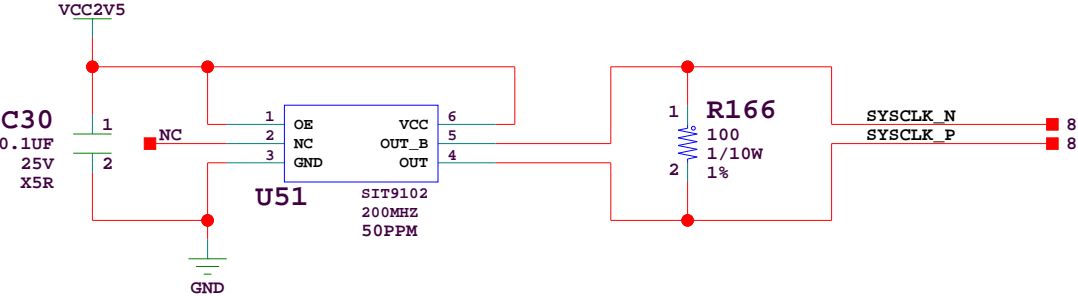
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
BLOCK DIAGRAM

Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	2 of 51	Drawn By	DN

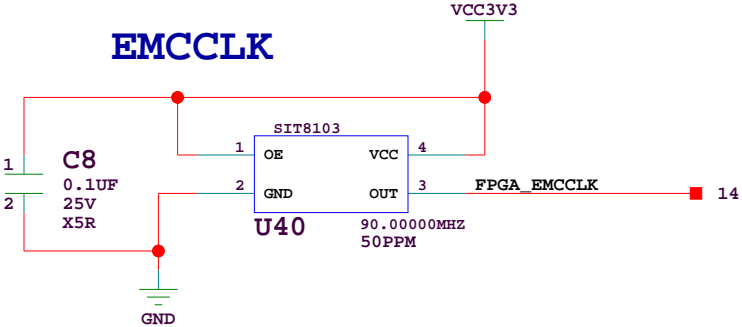
SI570BAB000544DG



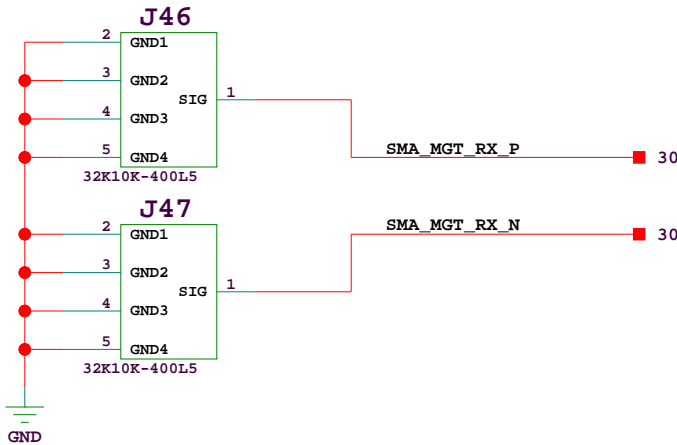
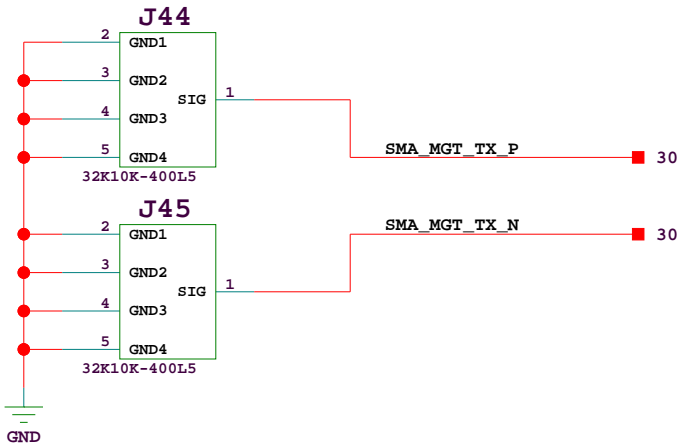
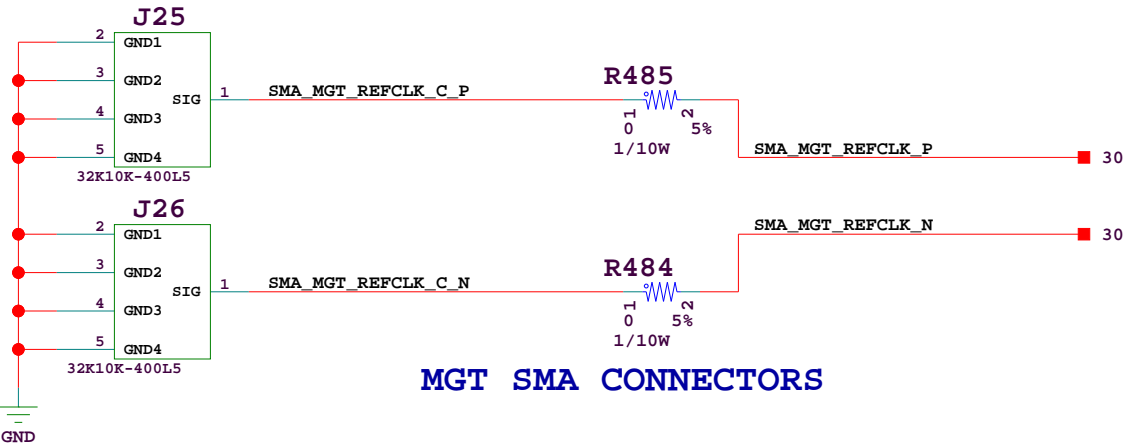
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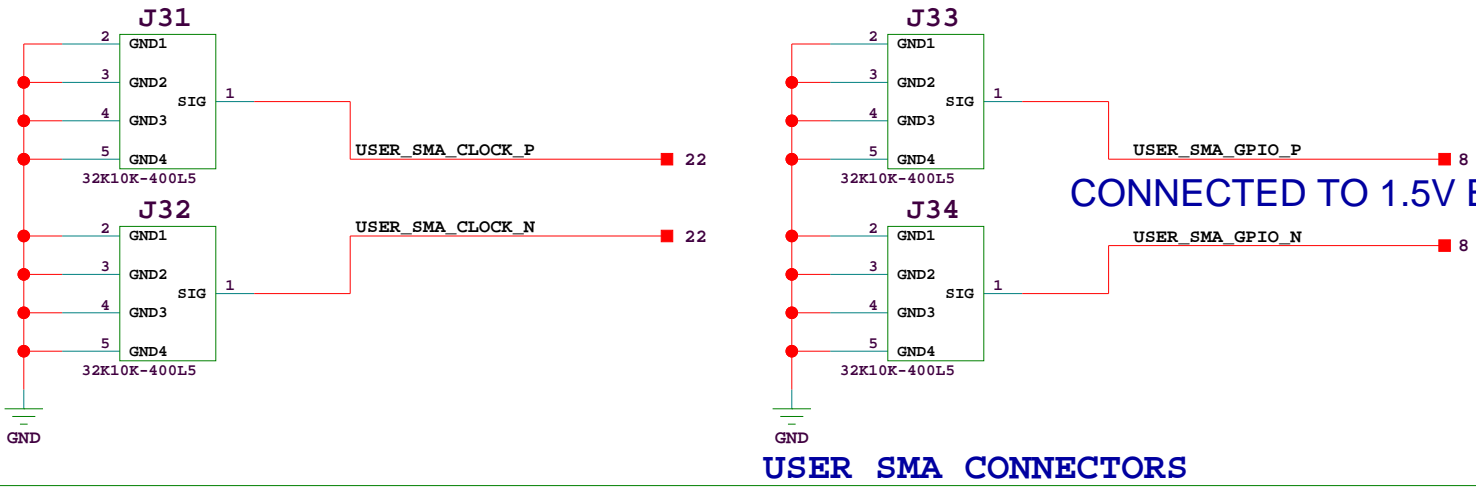
EMCCLK



MGT SMA CONNECTORS



CONNECTED TO 1.5V BANK

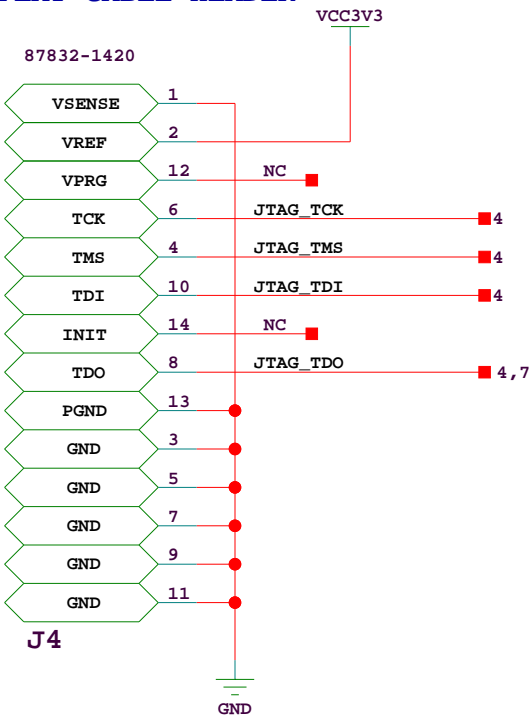


Clocks

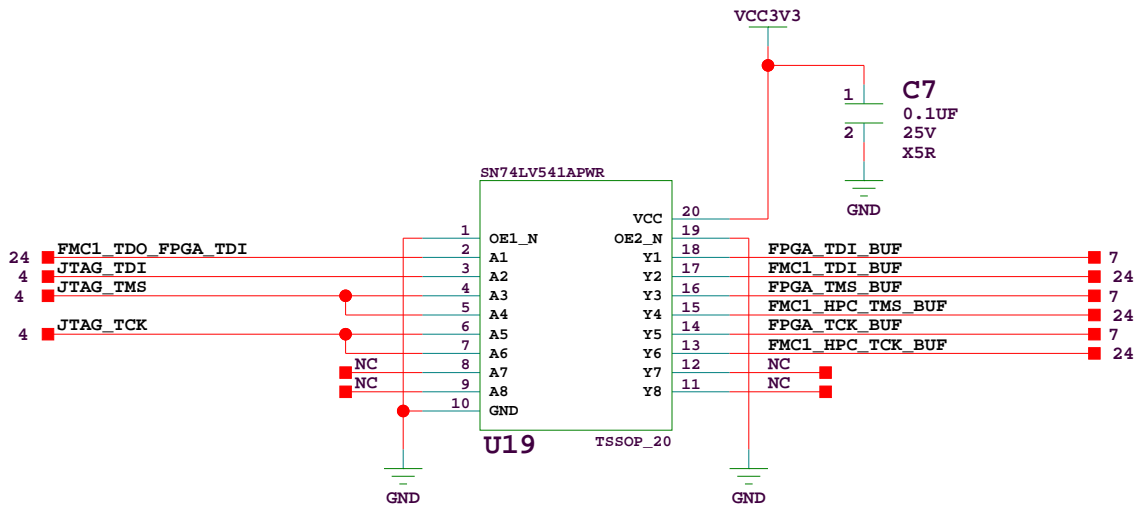
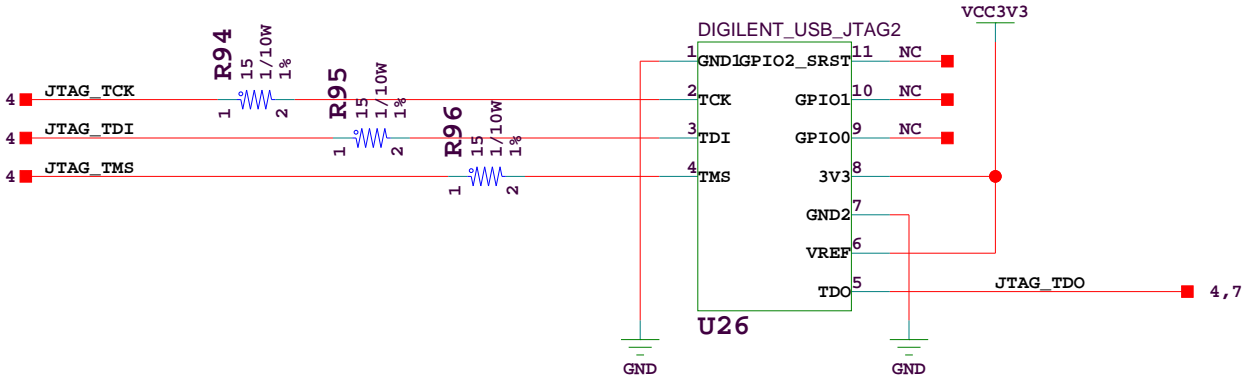


Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD CLOCKS	
Date: 2-14-2014_14:52	Ver: 2.0
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Sheet 3 of 51	Drawn By DN

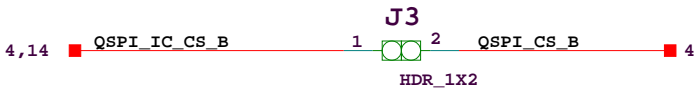
JTAG FLAT-CABLE HEADER



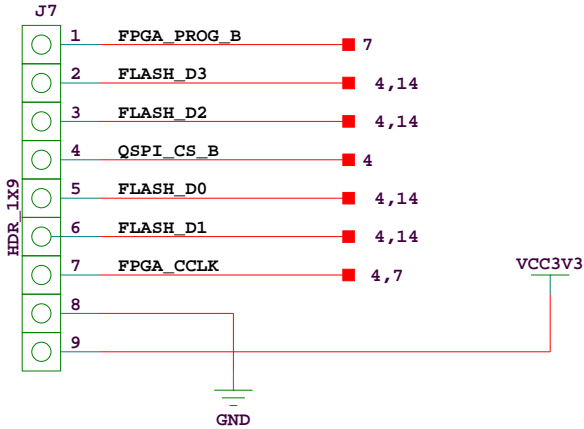
USB JTAG DIGILENT MODULE



ON = SPI DEVICE
OFF = SPI EXTERNAL



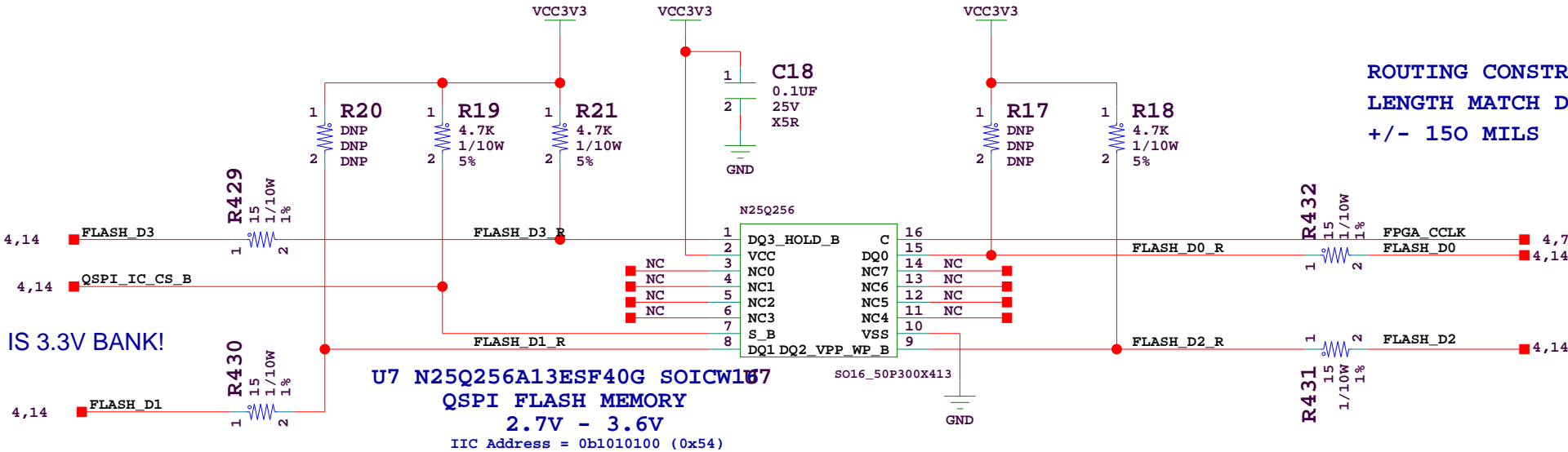
SPI SELECT JUMPER




SPI EXTERNAL
PROGRAMMING HEADER

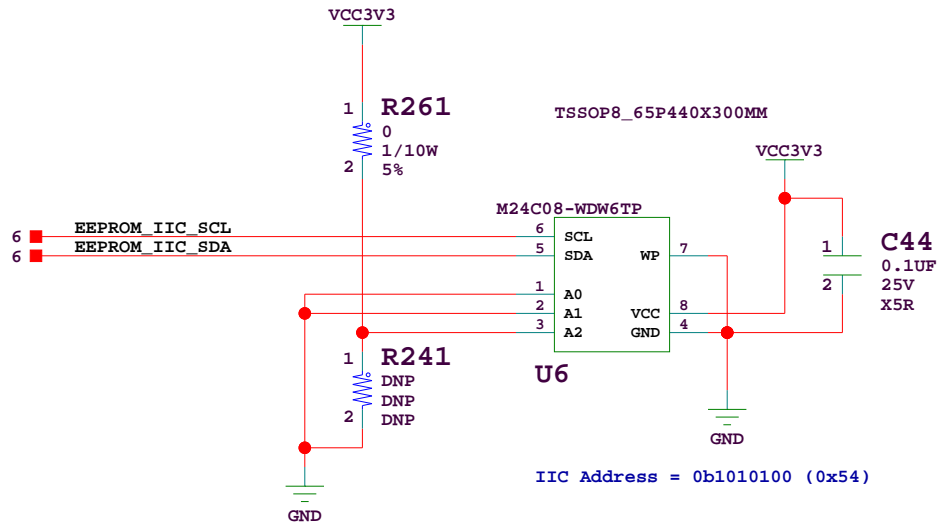
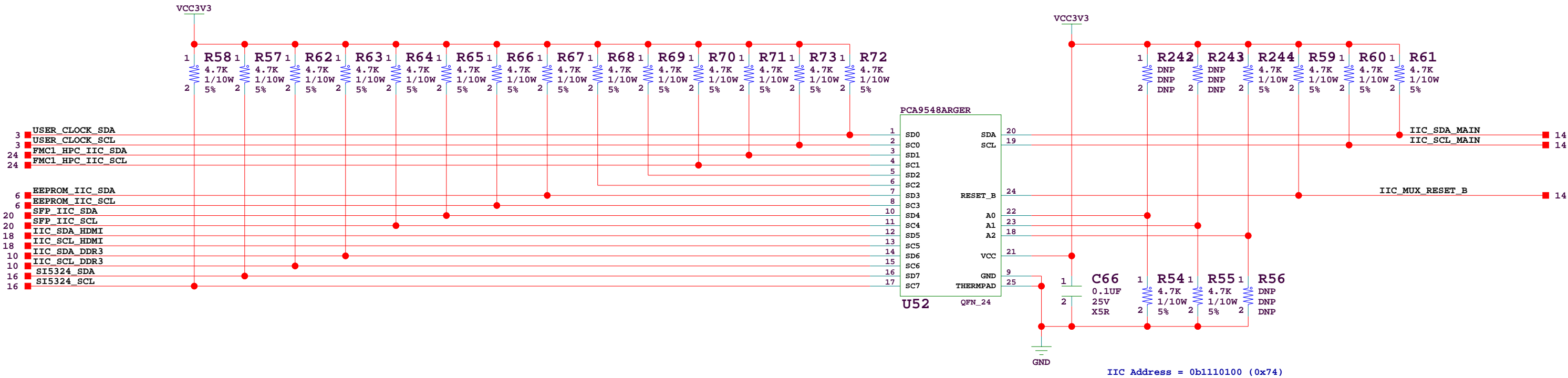
ROUTING CONSTRAINT:
LENGTH MATCH DATA AND CLOCK
+/- 150 MILS

PG.14 IS 3.3V BANK!




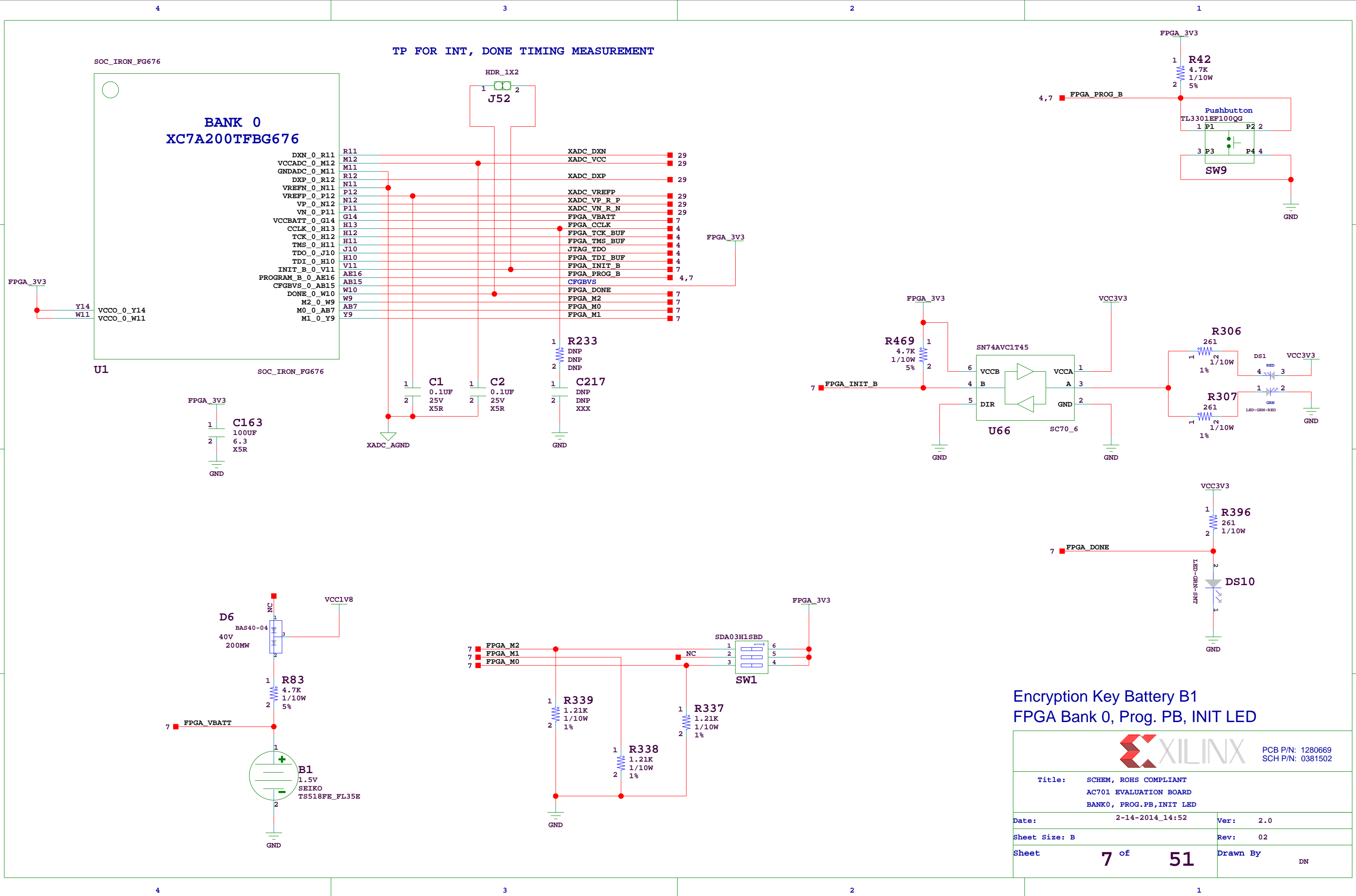
FPGA Configuration Options

		PCB P/N: 1280669 SCH P/N: 0381502	
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Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	4 of 51	Drawn By	DN



IIC MUX, EEPROM

		PCB P/N: 1280669 SCH P/N: 0381502	
Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD IIC MUX and EEPROM			
Date: 2-14-2014_14:52		Ver: 2.0	
Sheet Size: B		Rev: 02	
Sheet 6 of 51		Drawn By DN	

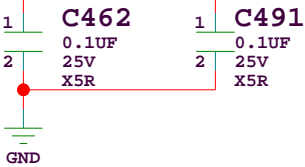


SOC_IRON_FG676

BANK 34
XC7A200TFBG676

IO_0_34_N8	N8	DDR3_RESET_B	10
IO_L1P_T0_34_K3	K3	DDR3_A9	10
IO_L1N_T0_34_J3	J3	DDR3_A1	10
IO_L2P_T0_34_M7	M7	DDR3_A5	10
IO_L2N_T0_34_L7	L7	DDR3_A12	10
IO_L3P_T0_DQS_34_M4	M4	DDR3_A0	10
IO_L3N_T0_DQS_34_L4	L4	DDR3_A3	10
IO_L4P_T0_34_L5	L5	DDR3_A11	10
IO_L4N_T0_34_K5	K5	DDR3_A4	10
IO_L5P_T0_34_N7	N7	DDR3_A10	10
IO_L5N_T0_34_N6	N6	DDR3_A13	10
IO_L6P_T0_34_M6	M6	DDR3_A7	10
IO_L6N_T0_VREF_34_M5	M5		
IO_L7P_T1_34_K1	K1	DDR3_A6	10
IO_L7N_T1_34_J1	J1	DDR3_A2	10
IO_L8P_T1_34_L3	L3	DDR3_A14	10
IO_L8N_T1_34_K2	K2	DDR3_A15	10
IO_L9P_T1_DQS_34_N1	N1	DDR3_BA0	10
IO_L9N_T1_DQS_34_M1	M1	DDR3_BA1	10
IO_L10P_T1_34_H2	H2	DDR3_BA2	10
IO_L10N_T1_34_H1	H1	DDR3_A8	10
IO_L11P_T1_SRCC_34_M2	M2	DDR3_CLK0_P	10
IO_L11N_T1_SRCC_34_L2	L2	DDR3_CLK0_N	10
IO_L12P_T1_MRCC_34_N3	N3	DDR3_CLK1_P	10
IO_L12N_T1_MRCC_34_N2	N2	DDR3_CLK1_N	10
IO_L13P_T2_MRCC_34_R3	R3	SYSCLK_P	3
IO_L13N_T2_MRCC_34_P3	P3	SYSCLK_N	3
IO_L14P_T2_SRCC_34_P4	P4	DDR3_CKE0	10
IO_L14N_T2_SRCC_34_N4	N4	DDR3_CKE1	10
IO_L15P_T2_DQS_34_R1	R1	DDR3_WE_B	10
IO_L15N_T2_DQS_34_P1	P1	DDR3_RAS_B	10
IO_L16P_T2_34_T4	T4	DDR3_CAS_B	10
IO_L16N_T2_34_T3	T3	DDR3_S0_B	10
IO_L17P_T2_34_T2	T2	DDR3_S1_B	10
IO_L17N_T2_34_R2	R2	DDR3_ODT0	10
IO_L18P_T2_34_U2	U2	DDR3_ODT1	10
IO_L18N_T2_34_U1	U1	DDR3_TEMP_EVENT	10
IO_L19P_T3_34_P6	P6	GPIO_SW_N	21
IO_L19N_T3_VREF_34_P5	P5		
IO_L20P_T3_34_T5	T5	GPIO_SW_S	21
IO_L20N_T3_34_R5	R5	GPIO_SW_W	21
IO_L21P_T3_DQS_34_U6	U6	GPIO_SW_C	21
IO_L21N_T3_DQS_34_U5	U5	GPIO_SW_E	21
IO_L22P_T3_34_R8	R8	GPIO_DIP_SW0	21
IO_L22N_T3_34_P8	P8	GPIO_DIP_SW1	21
IO_L23P_T3_34_R7	R7	GPIO_DIP_SW2	21
IO_L23N_T3_34_R6	R6	GPIO_DIP_SW3	21
IO_L24P_T3_34_T8	T8	USER_SMA_GPIO_P	3
IO_L24N_T3_34_T7	T7	USER_SMA_GPIO_N	3
IO_25_34_U4	U4	CPU_RESET	21

VTTVREF



FPGA_1V5

T6	VCCO_34_T6
P2	VCCO_34_P2
N5	VCCO_34_N5
M8	VCCO_34_M8
L1	VCCO_34_L1
K4	VCCO_34_K4

U1

SOC_IRON_FG676

FPGA_1V5

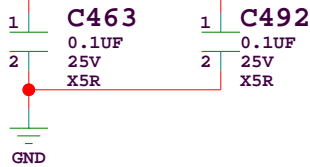


SOC_IRON_FG676

BANK 35
XC7A200TFBG676

IO_0_35_J8	J8	NC	
IO_L1P_T0_AD4P_35_E6	E6	DDR3_D63	10,12
IO_L1N_T0_AD4N_35_D6	D6	DDR3_D62	10,12
IO_L2P_T0_AD12P_35_H8	H8	DDR3_D61	10,12
IO_L2N_T0_AD12N_35_G8	G8	DDR3_D60	10,12
IO_L3P_T0_DQS_AD5P_35_H7	H7	DDR3_DQS7_P	10,12
IO_L3N_T0_DQS_AD5N_35_G7	G7	DDR3_DQS7_N	10,12
IO_L4P_T0_35_F8	F8	DDR3_D59	10,12
IO_L4N_T0_35_F7	F7	DDR3_D58	10,12
IO_L5P_T0_AD13P_35_H6	H6	DDR3_D57	10,12
IO_L5N_T0_AD13N_35_G6	G6	DDR3_D56	10,12
IO_L6P_T0_35_H9	H9	DDR3_DM7	10
IO_L6N_T0_VREF_35_G9	G9		
IO_L7P_T1_AD6P_35_J6	J6	DDR3_D55	10,12
IO_L7N_T1_AD6N_35_J5	J5	DDR3_D54	10,12
IO_L8P_T1_AD14P_35_L8	L8	DDR3_D53	10,12
IO_L8N_T1_AD14N_35_K8	K8	DDR3_D52	10,12
IO_L9P_T1_DQS_AD7P_35_J4	J4	DDR3_DQS6_P	10,12
IO_L9N_T1_DQS_AD7N_35_H4	H4	DDR3_DQS6_N	10,12
IO_L10P_T1_AD15P_35_K7	K7	DDR3_D51	10,12
IO_L10N_T1_AD15N_35_K6	K6	DDR3_D50	10,12
IO_L11P_T1_SRCC_35_G4	G4	DDR3_D49	10,12
IO_L11N_T1_SRCC_35_F4	F4	DDR3_D48	10,12
IO_L12P_T1_MRCC_35_G5	G5	DDR3_DM6	10
IO_L12N_T1_MRCC_35_F5	F5	NC	
IO_L13P_T2_MRCC_35_E5	E5	DDR3_D47	10,12
IO_L13N_T2_MRCC_35_D5	D5	DDR3_D46	10,12
IO_L14P_T2_SRCC_35_D4	D4	DDR3_D45	10,12
IO_L14N_T2_SRCC_35_C4	C4	DDR3_D44	10,12
IO_L15P_T2_DQS_35_B5	B5	DDR3_DQS5_P	10,12
IO_L15N_T2_DQS_35_A5	A5	DDR3_DQS5_N	10,12
IO_L16P_T2_35_B4	B4	DDR3_D43	10,12
IO_L16N_T2_35_A4	A4	DDR3_D42	10,12
IO_L17P_T2_35_D3	D3	DDR3_D41	10,12
IO_L17N_T2_35_C3	C3	DDR3_D40	10,12
IO_L18P_T2_35_F3	F3	DDR3_DM5	10
IO_L18N_T2_35_E3	E3	NC	
IO_L19P_T3_35_C2	C2	DDR3_D39	10,12
IO_L19N_T3_VREF_35_B2	B2		
IO_L20P_T3_35_A3	A3	DDR3_D38	10,12
IO_L20N_T3_35_A2	A2	DDR3_D37	10,12
IO_L21P_T3_DQS_35_C1	C1	DDR3_DQS4_P	10,12
IO_L21N_T3_DQS_35_B1	B1	DDR3_DQS4_N	10,12
IO_L22P_T3_35_F2	F2	DDR3_D36	10,12
IO_L22N_T3_35_E2	E2	DDR3_D35	10,12
IO_L23P_T3_35_E1	E1	DDR3_D34	10,12
IO_L23N_T3_35_D1	D1	DDR3_D33	10,12
IO_L24P_T3_35_G2	G2	DDR3_D32	10,12
IO_L24N_T3_35_G1	G1	DDR3_DM4	10
IO_25_35_H3	H3	NC	

VTTVREF



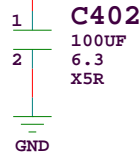
FPGA_1V5

J7	VCCO_35_J7
G3	VCCO_35_G3
F6	VCCO_35_F6
D2	VCCO_35_D2
C5	VCCO_35_C5
A1	VCCO_35_A1

U1

SOC_IRON_FG676

FPGA_1V5



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
BANKS34,35 DDR3 SODIMM IF

Date: 2-14-2014_14:52 Ver: 2.0

Sheet Size: B Rev: 02

Sheet 8 of 51 Drawn By DN

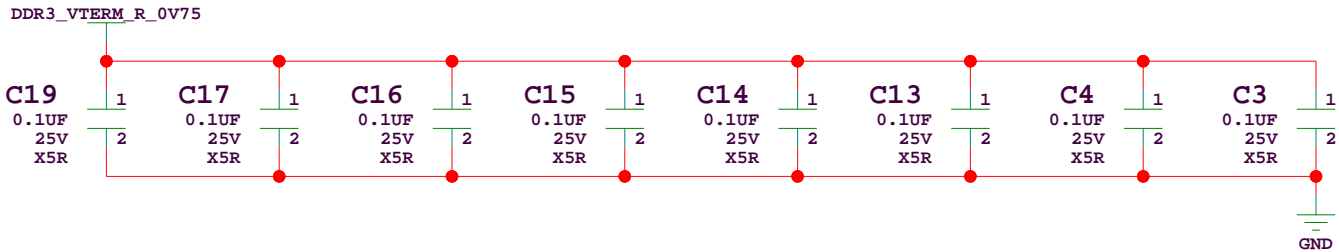
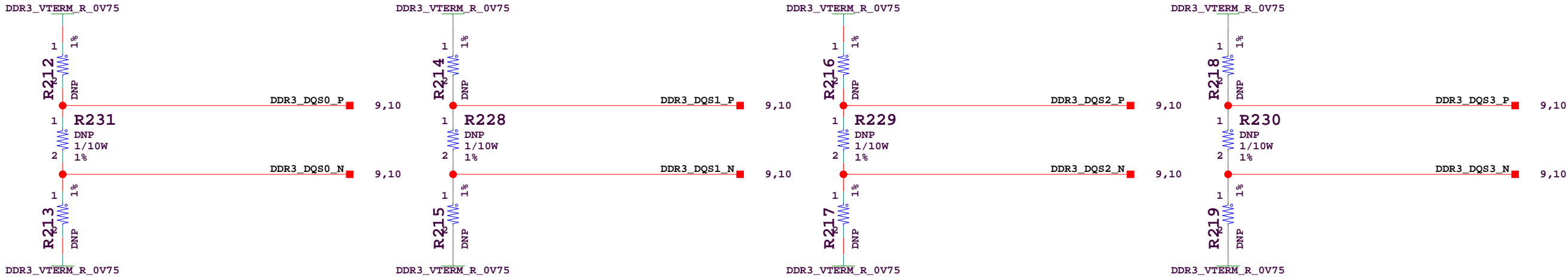
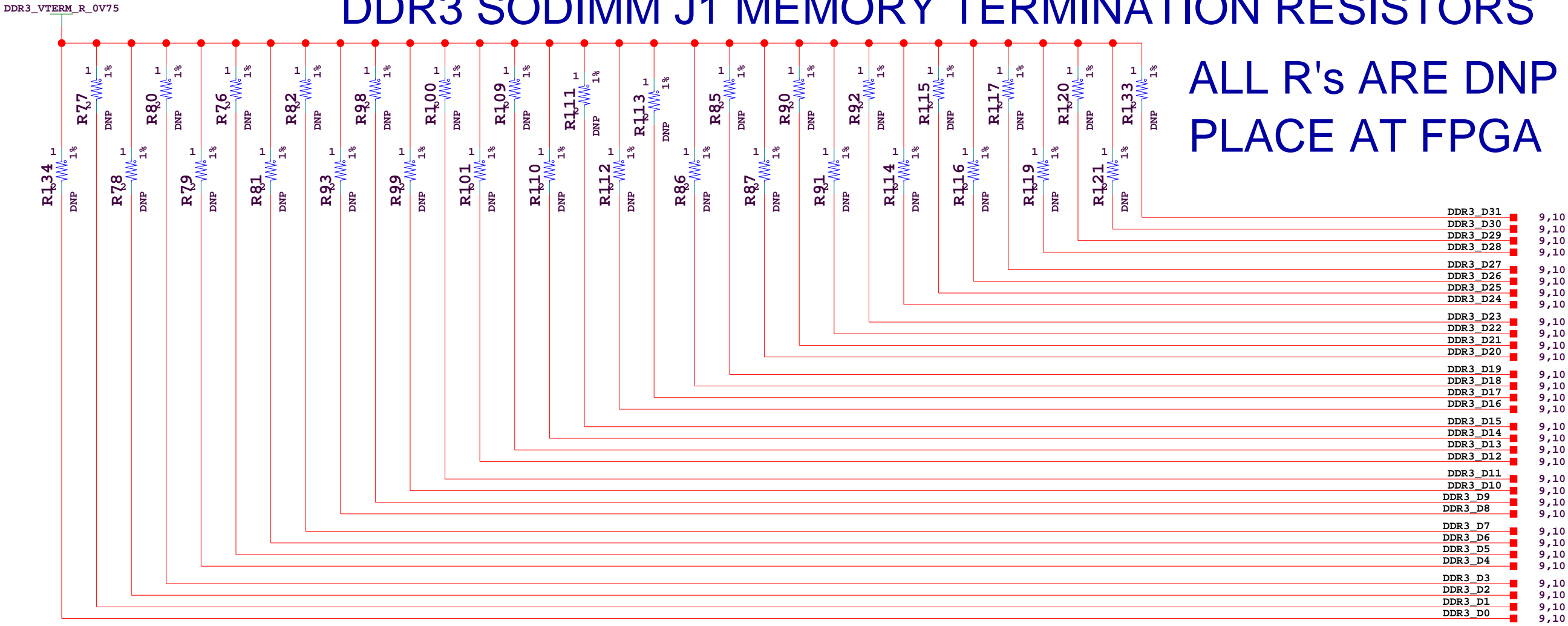
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Sheet **9** of **51** Drawn By **DN**

DDR3 SODIMM J1 MEMORY TERMINATION RESISTORS

ALL R's ARE DNP
PLACE AT FPGA

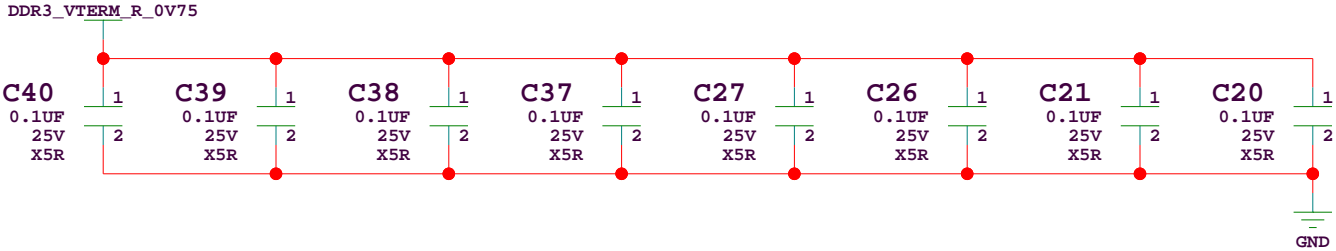
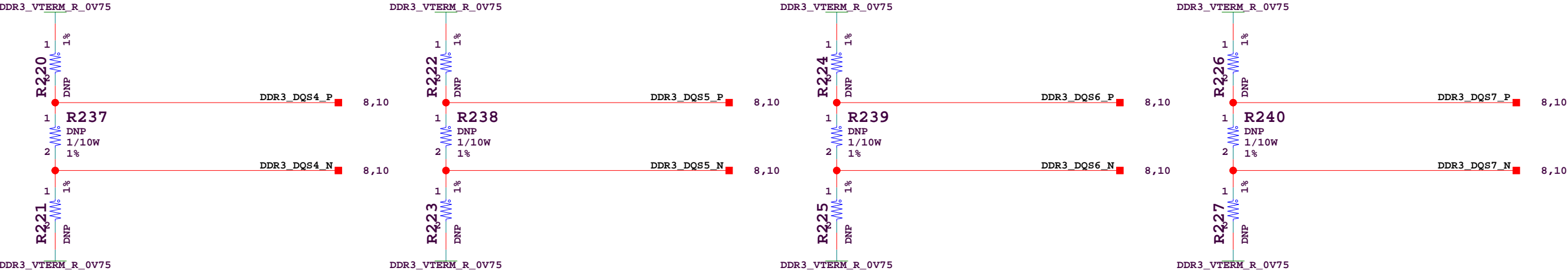
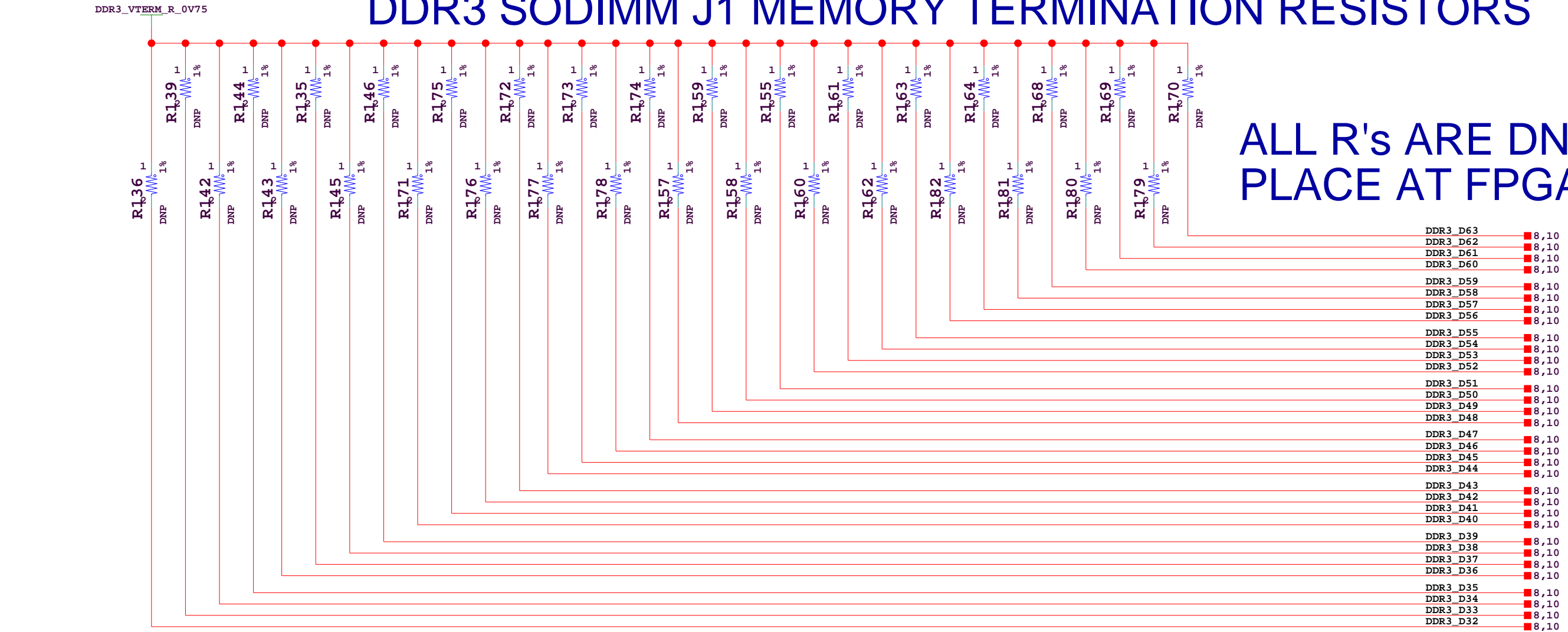


PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM TERM. RESISTORS	
Date: 2-14-2014_14:52	Ver: 2.0
Sheet Size: B	Rev: 02
Sheet 11 of 51	Drawn By DN

DDR3 SODIMM J1 MEMORY TERMINATION RESISTORS

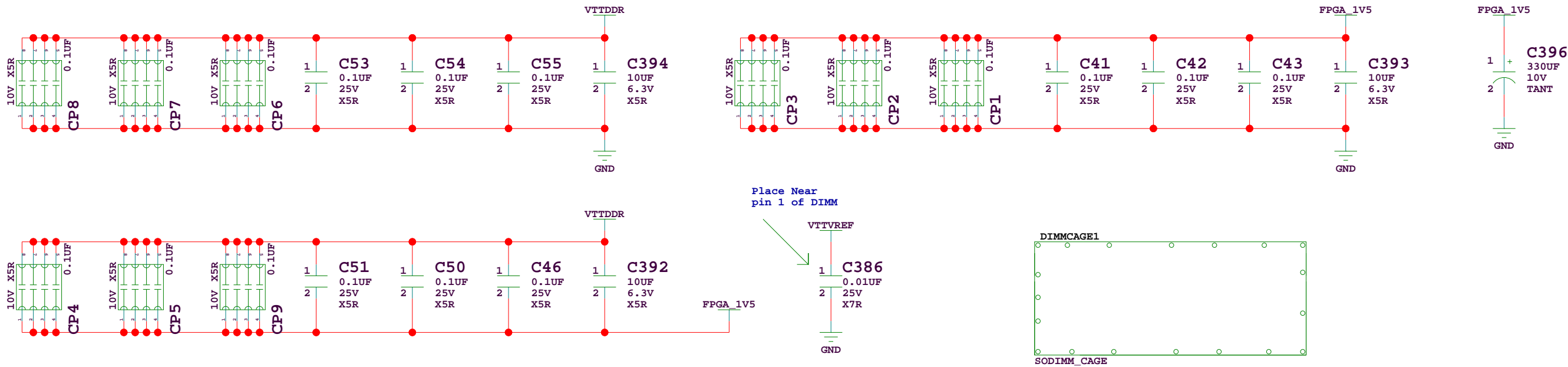
ALL R's ARE DNP
PLACE AT FPGA



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM TERM. RESISTORS	
Date: 2-14-2014_14:52	Ver: 2.0
Sheet Size: B	Rev: 02
Sheet 12 of 51	Drawn By DN

DDR3 SODIMM J1 MEMORY DECOUPLING CAPACITORS



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
DDR3 SODIMM DECOUPLING

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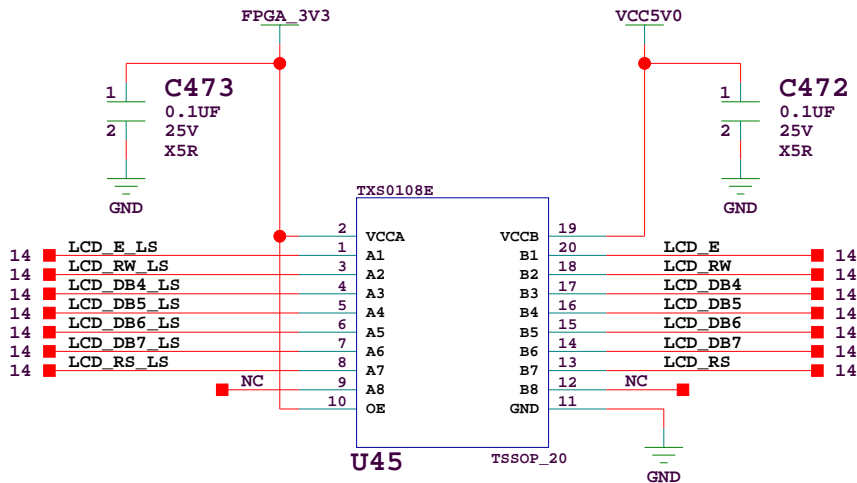
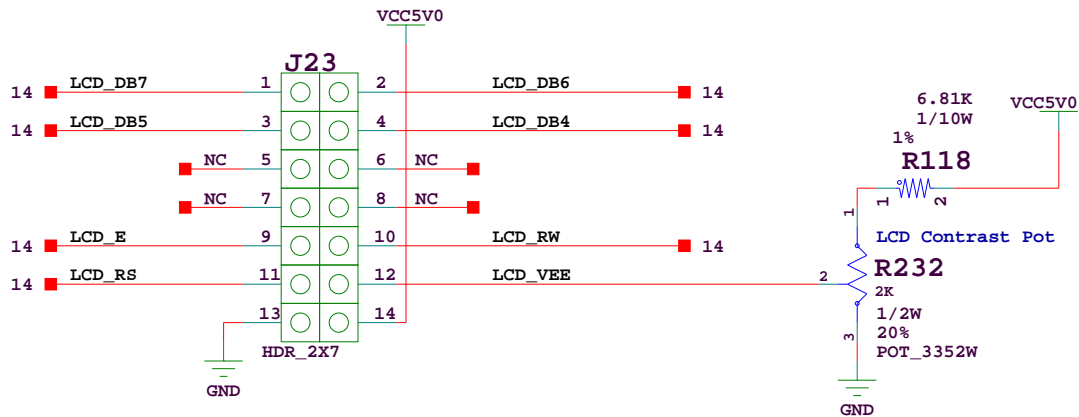
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Sheet 13 of 51 Drawn By DN

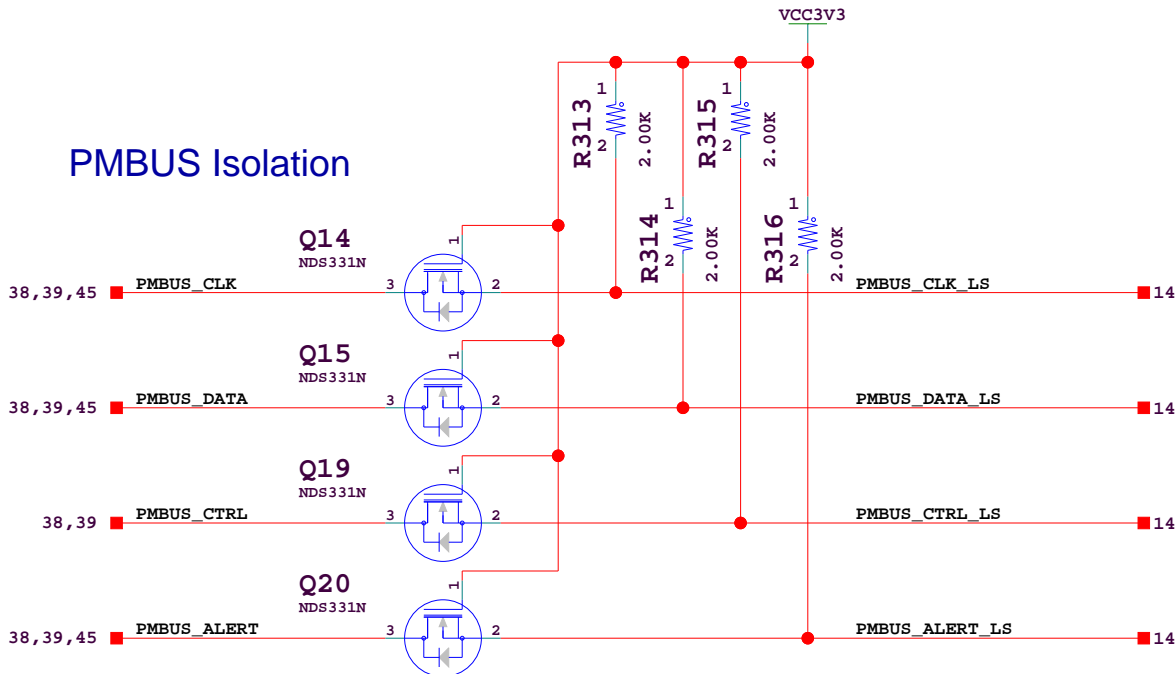
BANK 14
XC7A200TFBG676

IO_0_14_M19	M19	SI5324_INT_ALM_B	16
IO_L1P_T0_D00_MOSI_14_R14	R14	FLASH_D0	4
IO_L1N_T0_D01_DIN_14_R15	R15	FLASH_D1	4
IO_L2P_T0_D02_14_P14	P14	FLASH_D2	4
IO_L2N_T0_D03_14_N14	N14	FLASH_D3	4
IO_L3P_T0_DQS_PUDC_B_14_P15	P15	CTRL2_PWRGOOD	24, 39, 45
IO_L3N_T0_DQS_EMCCLK_14_P16	P16	FPGA_EMCCLK	3
IO_L4P_T0_D04_14_N16	N16	FMC1_HPC_PRSENT_M2C_B	24, 26
IO_L4N_T0_D05_14_N17	N17	FMC1_HPC_PG_M2C	25
IO_L5P_T0_D06_14_R16	R16	FMC_VADJ_ON_B	45
IO_L5N_T0_D07_14_R17	R17	IIC_MUX_RESET_B	6
IO_L6P_T0_FCS_B_14_P18	P18	QSPI_IC_CS_B	4
IO_L6N_T0_D08_VREF_14_N18	N18	IIC_SCL_MAIN	6
IO_L7P_T1_D09_14_K25	K25	IIC_SDA_MAIN	6
IO_L7N_T1_D10_14_K26	K26	PCIE_WAKE_B	28
IO_L8P_T1_D11_14_M20	M20	PCIE_PERST	28
IO_L8N_T1_D12_14_L20	L20	LCD_E_LS	14
IO_L9P_T1_DQS_14_L24	L24	LCD_RW_LS	14
IO_L9N_T1_DQS_D13_14_L25	L25	LCD_DB4_LS	14
IO_L10P_T1_D14_14_M24	M24	LCD_DB5_LS	14
IO_L10N_T1_D15_14_M25	M25	LCD_DB6_LS	14
IO_L11P_T1_SRCC_14_L22	L22	LCD_DB7_LS	14
IO_L11N_T1_SRCC_14_L23	L23	LCD_RS_LS	14
IO_L12P_T1_MRCC_14_M21	M21	USER_CLOCK_P	3
IO_L12N_T1_MRCC_14_M22	M22	USER_CLOCK_N	3
IO_L13P_T2_MRCC_14_N21	N21	ROTARY_PUSH	21
IO_L13N_T2_MRCC_14_N22	N22	ROTARY_INCA	21
IO_L14P_T2_SRCC_14_P20	P20	ROTARY_INCB	21
IO_L14N_T2_SRCC_14_P21	P21	SDIO_CD_DAT3	14
IO_L15P_T2_DQS_RDWR_B_14_N23	N23	SDIO_CMD	14
IO_L15N_T2_DQSDOUT_CSOB_14_N24	N24	SDIO_CLK	14
IO_L16P_T2_CSI_B_14_P19	P19	SDIO_DAT0	14
IO_L16N_T2_A15_D31_14_N19	N19	SDIO_DAT1	14
IO_L17P_T2_A14_D30_14_P23	P23	SDIO_DAT2	14
IO_L17N_T2_A13_D29_14_P24	P24	SDIO_SDDDET	14
IO_L18P_T2_A12_D28_14_R20	R20	SDIO_SDWP	14
IO_L18N_T2_A11_D27_14_R21	R21	PMBUS_CLK_LS	14
IO_L19P_T3_A10_D26_14_R25	R25	PMBUS_DATA_LS	14
IO_L19N_T3_A09_D25_VREF_14_P25	P25	PMBUS_CTRL_LS	14
IO_L20P_T3_A08_D24_14_N26	N26	PMBUS_ALERT_LS	14
IO_L20N_T3_A07_D23_14_M26	M26	GPIO_LED_0	21
IO_L21P_T3_DQS_14_T24	T24	GPIO_LED_1	21
IO_L21N_T3_DQS_A06_D22_14_T25	T25	GPIO_LED_2	21
IO_L22P_T3_A05_D21_14_R26	R26	GPIO_LED_3	21
IO_L22N_T3_A04_D20_14_P26	P26	PMOD_0	21
IO_L23P_T3_A03_D19_14_T22	T22	PMOD_1	21
IO_L23N_T3_A02_D18_14_R22	R22	PMOD_2	21
IO_L24P_T3_A01_D17_14_T23	T23	PMOD_3	21
IO_L24N_T3_A00_D16_14_R23	R23	SFP_LOS	21
IO_25_14_R18	R18	SFP_TX_DISABLE	20

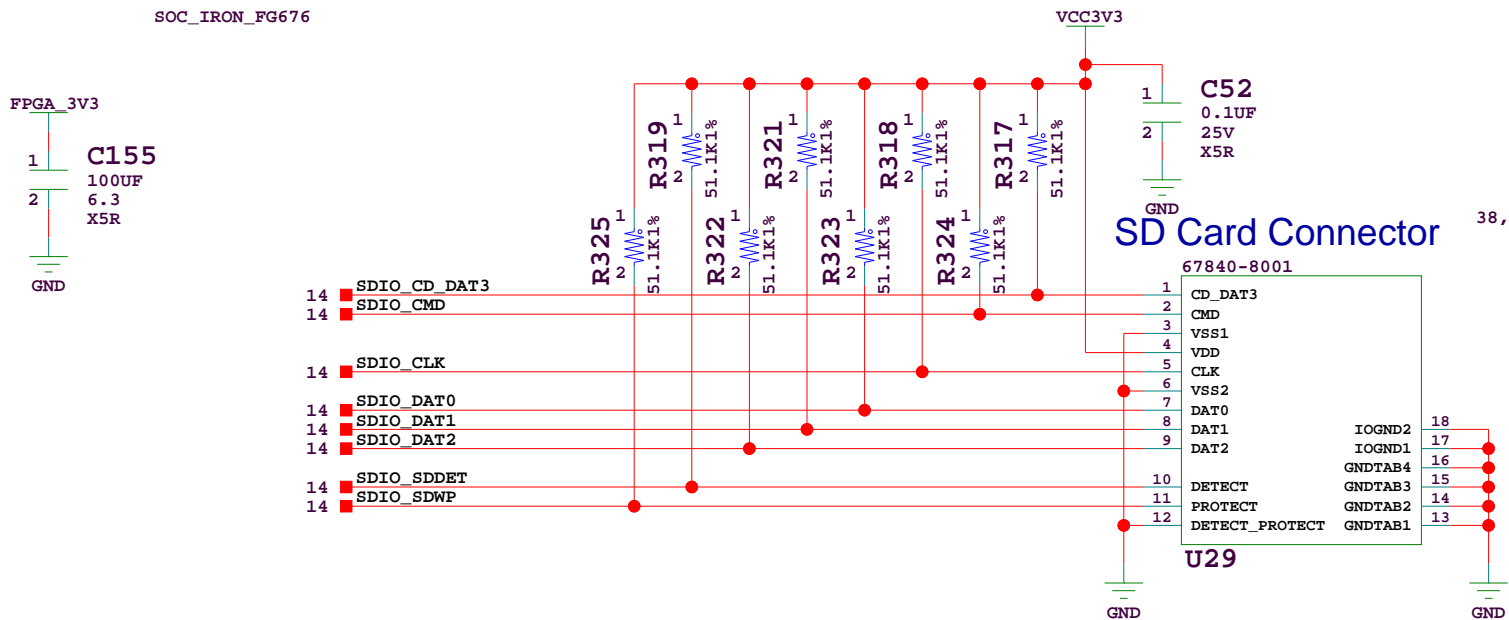
PWRCTL1_VCC4B_PG
CTRL2_PWRGOOD from TI controller U9
indicates both VCC3V3 and VCCO_VADJ
FMC power rails are OK



PMBUS Isolation



SD Card Connector



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
GPIO BANK14, SD SOCKET, LCD IF

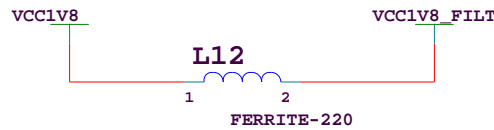
Date: 2-14-2014_14:52 Ver: 2.0

Sheet Size: B Rev: 02

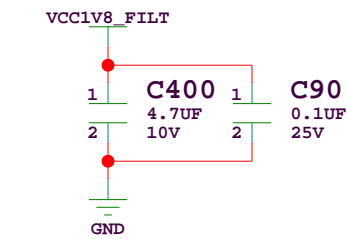
Sheet 14 of 51 Drawn By DN

CONFIGURATION MAPPING			
PIN	SETTING	CONFIGURATION	
CONFIG0	VCCO_MIO1	PHYAD[1]=1	PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2	GND	ENA_XC=0	PHYAD[4]=0
	EPHY_LED0	ENA_XC=0	PHYAD[4]=1
CONFIG3	VCCO_MIO1	ENA_XC=1	PHYAD[4]=1
	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=0	RGMII_RX=1
	EPHY_LED1	RGMII_TX=1	RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1	RGMII_RX=1

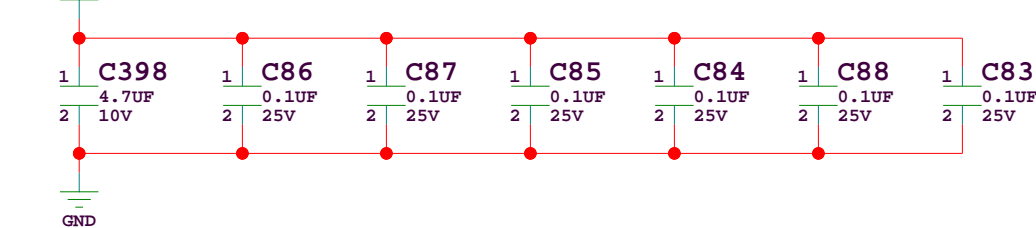
GEM / MDIO - POWER & DECOUPLING



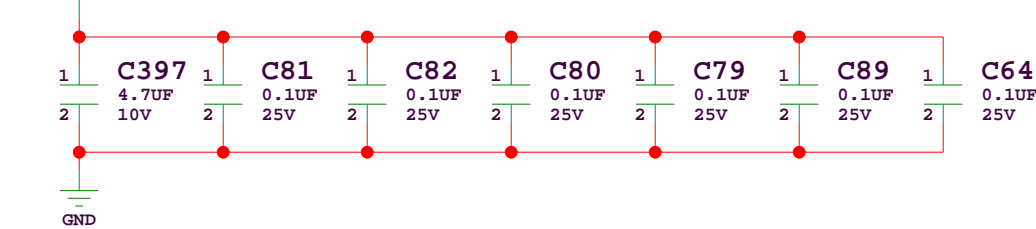
MAGNETICS / RJ45



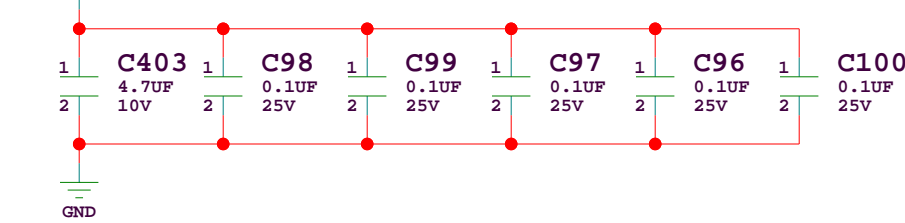
AVDDX, AVDDR, AVDDC



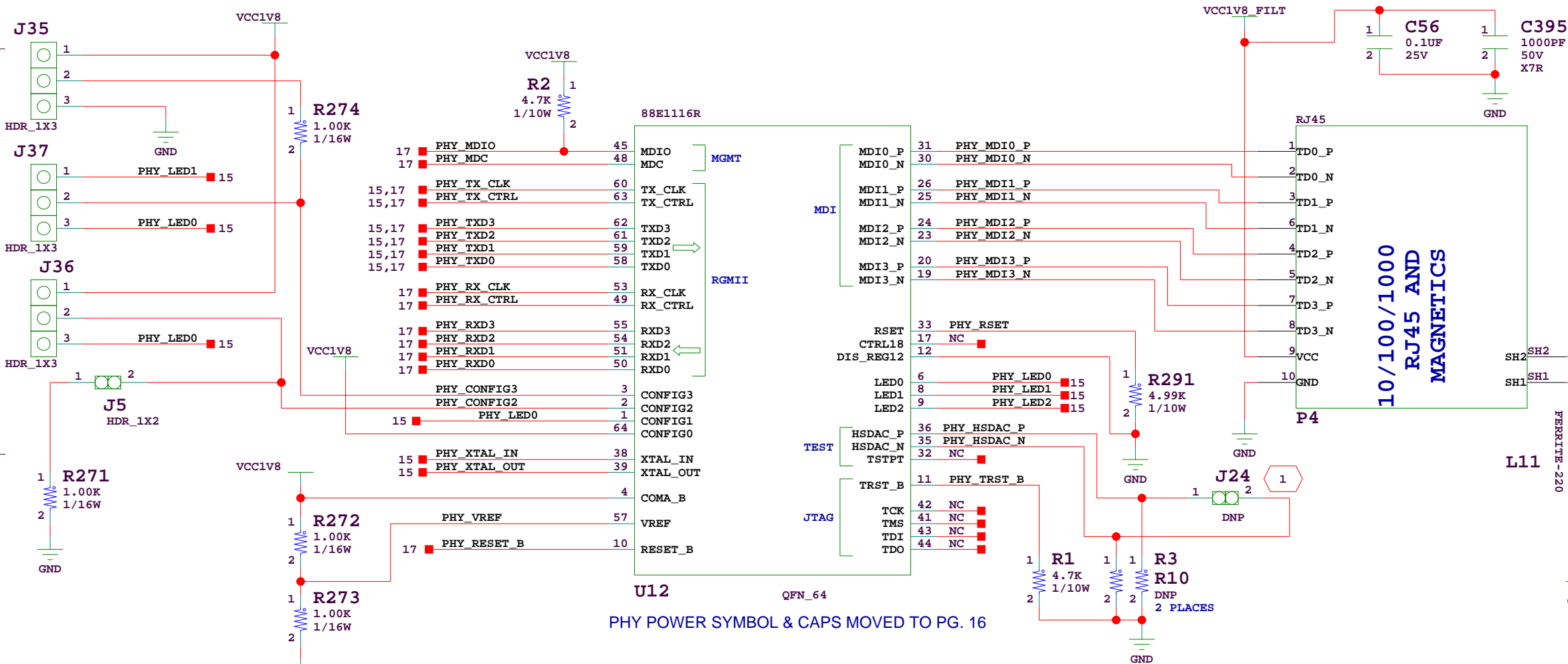
AVDD



VDDO, VDDOR



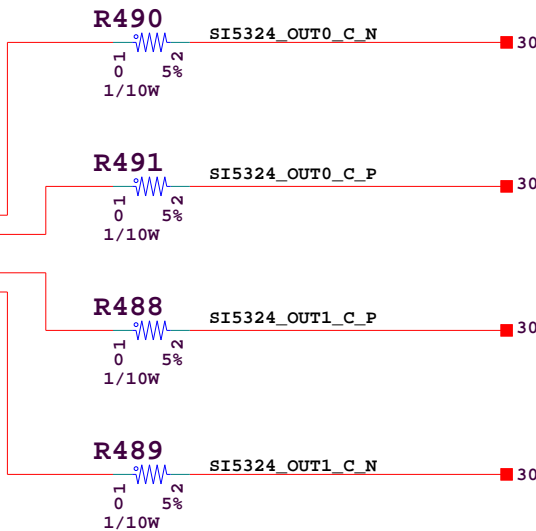
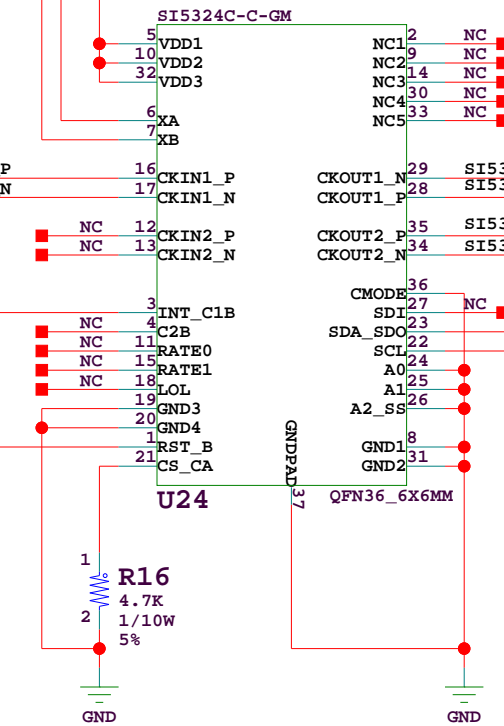
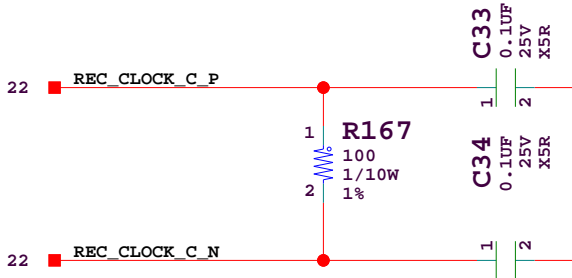
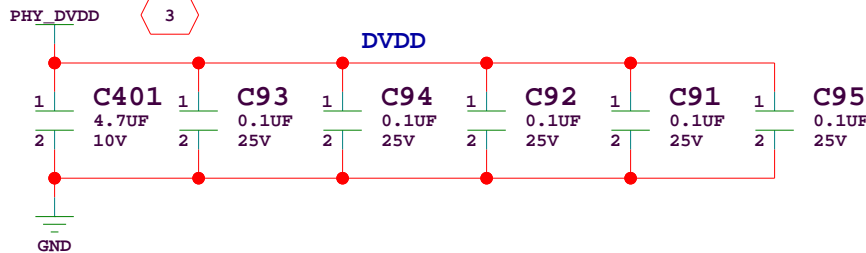
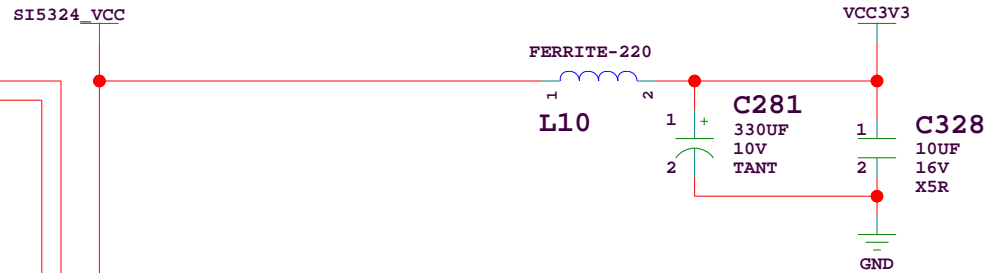
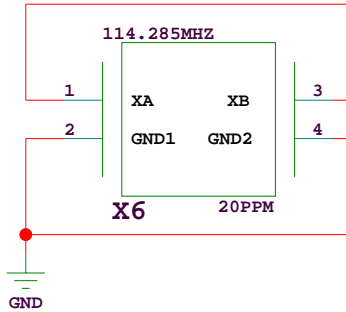
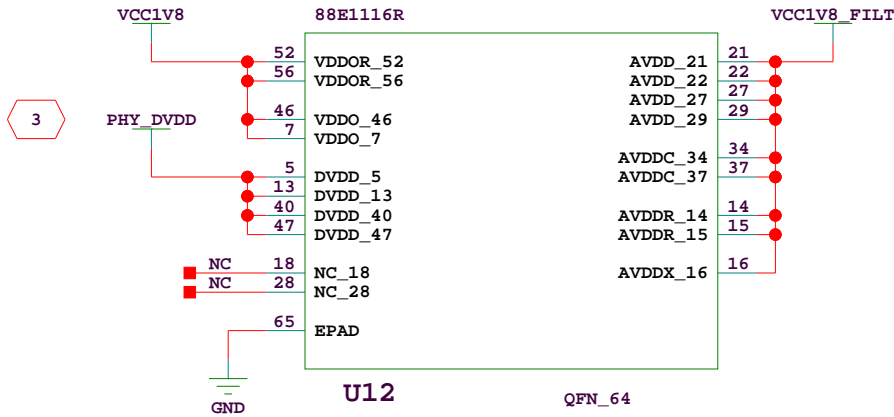
- 1 TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESISTORS ON HSDAC_P AND HSDAC_N.
- 2 SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS



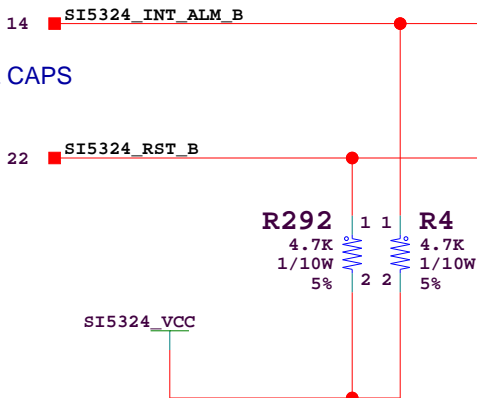
PHY POWER SYMBOL & CAPS MOVED TO PG. 16

GEM / MDIO

		PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD 10/100/1000 PHY	
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	15 of 51	Drawn By	DN



3 DVDD 1.2V IS SUPPLIED INTERNALLY. DVDD PINS 5,13,40,47 ARE FOR EXTERNAL CAPS



5324 Clock Recovery



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD SI5324 CLOCK RECOVERY	
Date: 2-14-2014_14:52	Ver: 2.0
Sheet Size: B	Rev: 02
Sheet 16 of 51	Drawn By DN

SOC_IRON_FG676

BANK 13
XC7A200TFBG676

IO_0_13_U24
IO_L1P_T0_13_U25
IO_L1N_T0_13_U26
IO_L2P_T0_13_V26
IO_L2N_T0_13_W26
IO_L3P_T0_DQS_13_AB26
IO_L3N_T0_DQS_13_AC26
IO_L4P_T0_13_W25
IO_L4N_T0_13_Y26
IO_L5P_T0_13_Y25
IO_L5N_T0_13_AA25
IO_L6P_T0_13_V24
IO_L6N_T0_VREF_13_W24
IO_L7P_T1_13_AA24
IO_L7N_T1_13_AB25
IO_L8P_T1_13_AA22
IO_L8N_T1_13_AA23
IO_L9P_T1_DQS_13_AB24
IO_L9N_T1_DQS_13_AC24
IO_L10P_T1_13_V23
IO_L10N_T1_13_W23
IO_L11P_T1_SRCC_13_Y22
IO_L11N_T1_SRCC_13_Y23
IO_L12P_T1_MRCC_13_U22
IO_L12N_T1_MRCC_13_V22
IO_L13P_T2_MRCC_13_U21
IO_L13N_T2_MRCC_13_V21
IO_L14P_T2_SRCC_13_W21
IO_L14N_T2_SRCC_13_Y21
IO_L15P_T2_DQS_13_T20
IO_L15N_T2_DQS_13_U20
IO_L16P_T2_13_W20
IO_L16N_T2_13_Y20
IO_L17P_T2_13_T19
IO_L17N_T2_13_U19
IO_L18P_T2_13_V19
IO_L18N_T2_13_W19
IO_L19P_T3_13_V18
IO_L19N_T3_VREF_13_W18
IO_L20P_T3_13_T14
IO_L20N_T3_13_T15
IO_L21P_T3_DQS_13_T17
IO_L21N_T3_DQS_13_T18
IO_L22P_T3_13_U15
IO_L22N_T3_13_U16
IO_L23P_T3_13_U14
IO_L23N_T3_13_V14
IO_L24P_T3_13_V16
IO_L24N_T3_13_V17
IO_25_13_U17

U24 HDMI_R_D21
U25 HDMI_R_D16
U26 HDMI_R_D11
V26 HDMI_R_D7
W26 HDMI_R_D8
AB26 HDMI_R_DE
AC26 HDMI_R_VSYNC
W25 HDMI_R_D9
Y26 HDMI_R_D6
Y25 HDMI_R_D5
AA25 HDMI_R_D29
V24 HDMI_R_D17
W24 HDMI_R_D10
AA24 HDMI_R_D4
AB25 HDMI_R_D30
AA22 HDMI_R_HSYNC
AA23 HDMI_R_D28
AB24 HDMI_R_D32
AC24 HDMI_R_D31
V23 HDMI_R_D23
W23 HDMI_R_D19
Y22 HDMI_R_D33
Y23 HDMI_R_D34
U22 PHY_TX_CLK
V22 HDMI_R_D35
U21 PHY_RX_CLK
V21 HDMI_R_CLK
W21 HDMI_INT
Y21 HDMI_R_SPDIF
T20 HDMI_SPDIF_OUT_LS
U20 HDMI_R_D18
W20 HDMI_R_D20
Y20 HDMI_R_D22
T19 USB_UART_TX
U19 USB_UART_RX
V19 USB_UART_RTS
W19 USB_UART_CTS
V18 PHY_RESET_B
W18 PHY_MDC
T14 PHY_MDIO
T15 PHY_TX_CTRL
T17 PHY_TXD3
T18 PHY_TXD2
U15 PHY_TXD1
U16 PHY_TXD0
U14 PHY_RX_CTRL
V14 PHY_RXD3
V16 PHY_RXD2
V17 PHY_RXD1
U17 PHY_RXD0

FPGA_1V8

Y24 VCCO_13_Y24
V20 VCCO_13_V20
U23 VCCO_13_U23
T26 VCCO_13_T26
T16 VCCO_13_T16
AC25 VCCO_13_AC25

U1

SOC_IRON_FG676

FPGA_1V8

C156
100UF
6.3
X5R

FPGA_1V8

C60
0.1UF
25V
X5R

VCC3V3

C59
0.1UF
25V
X5R

SN74AVC1T45

U38

HDMI_SPDIF_OUT_LS

HDMI_SPDIF_OUT



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
BANK13 HDIM/EPHY IF

Date: 2-14-2014_14:52 Ver: 2.0

Sheet Size: B Rev: 02

Sheet 17 of 51 Drawn By DN

D

C

B

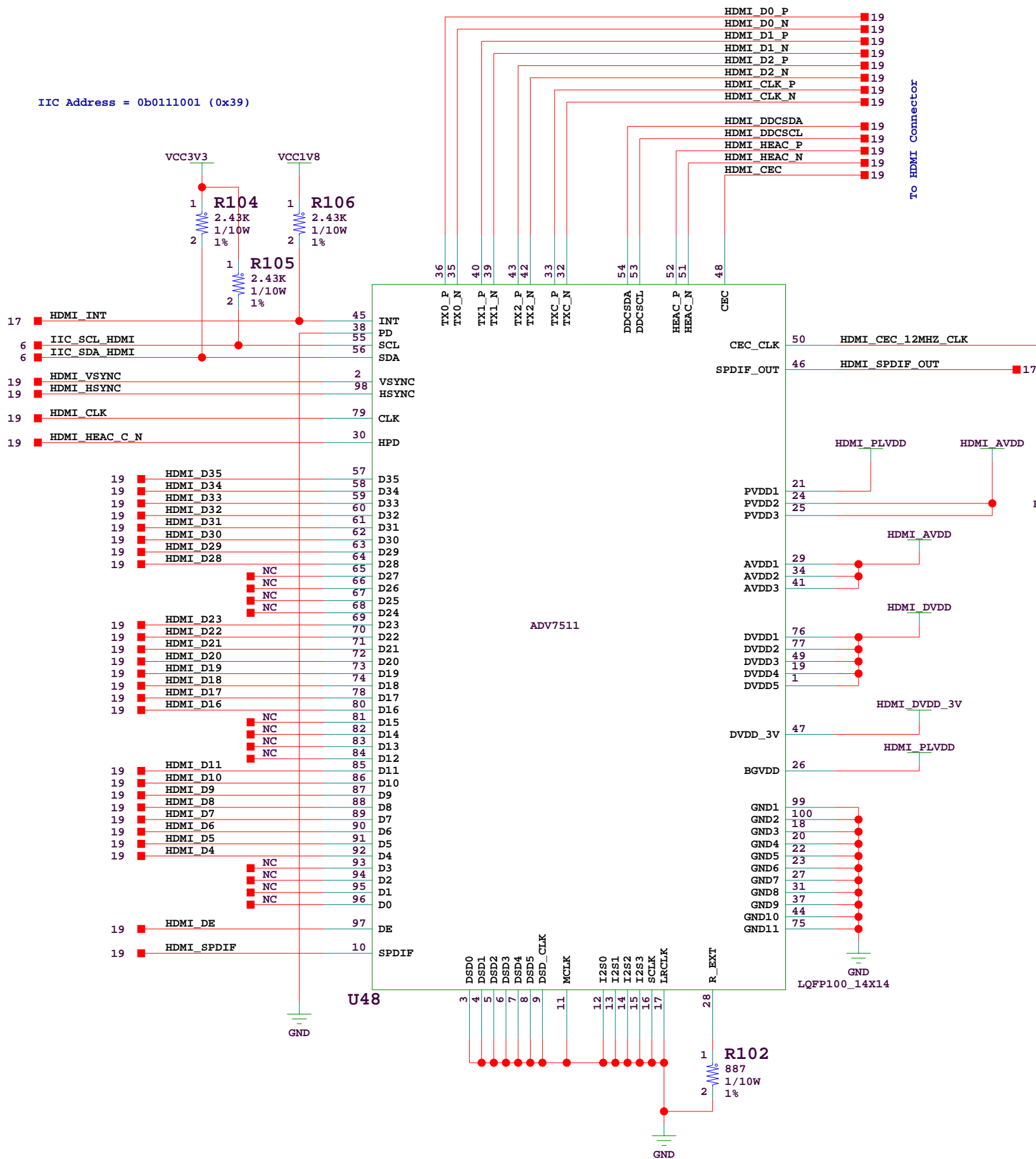
A

D

C

B

A



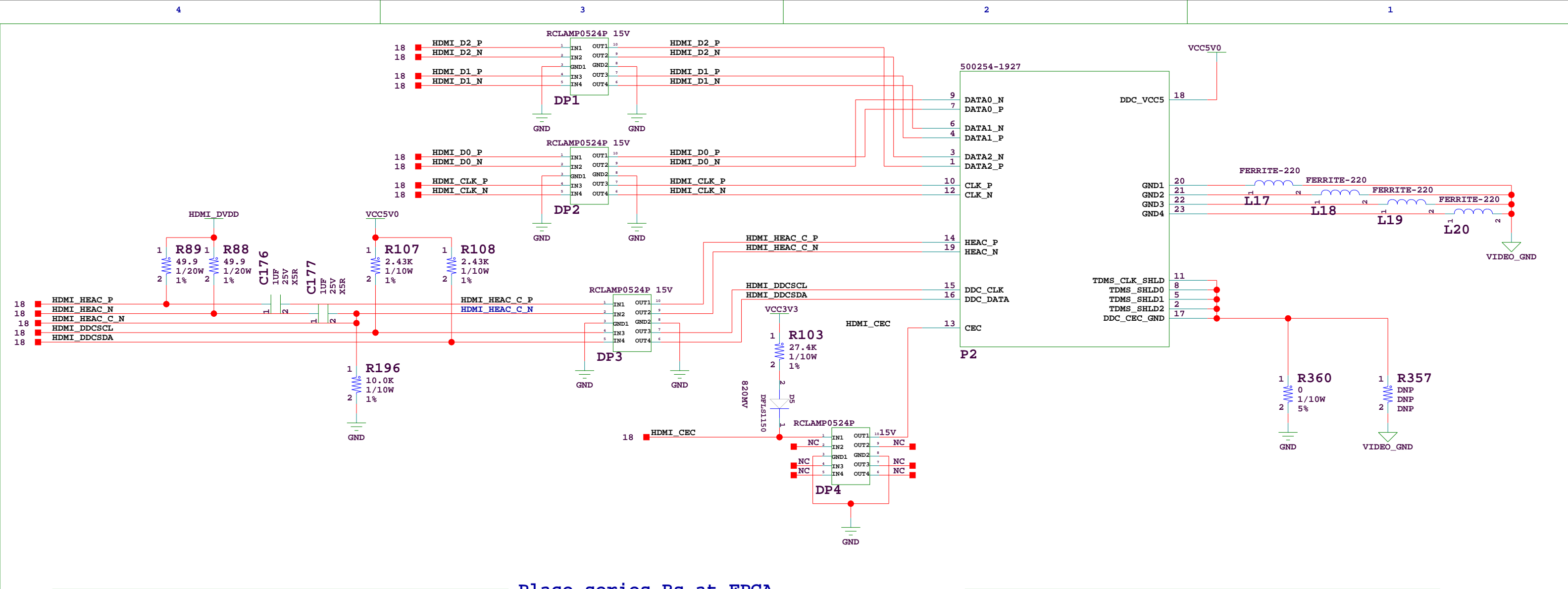
ADV7511 HDMI CODEC



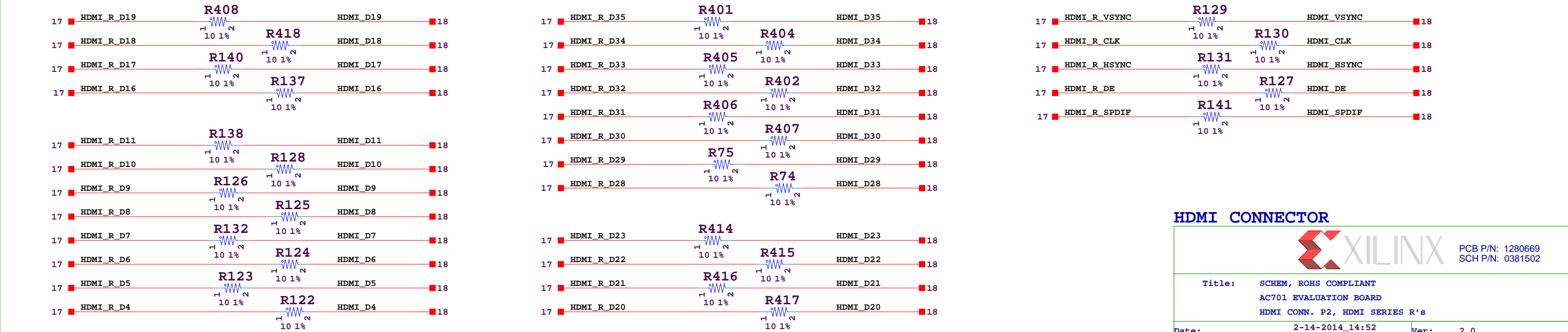
PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
ADV7511 HDMI CODEC

Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	18 of 51	Drawn By	DN



Place series Rs at FPGA



HDMI CONNECTOR

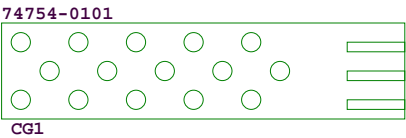
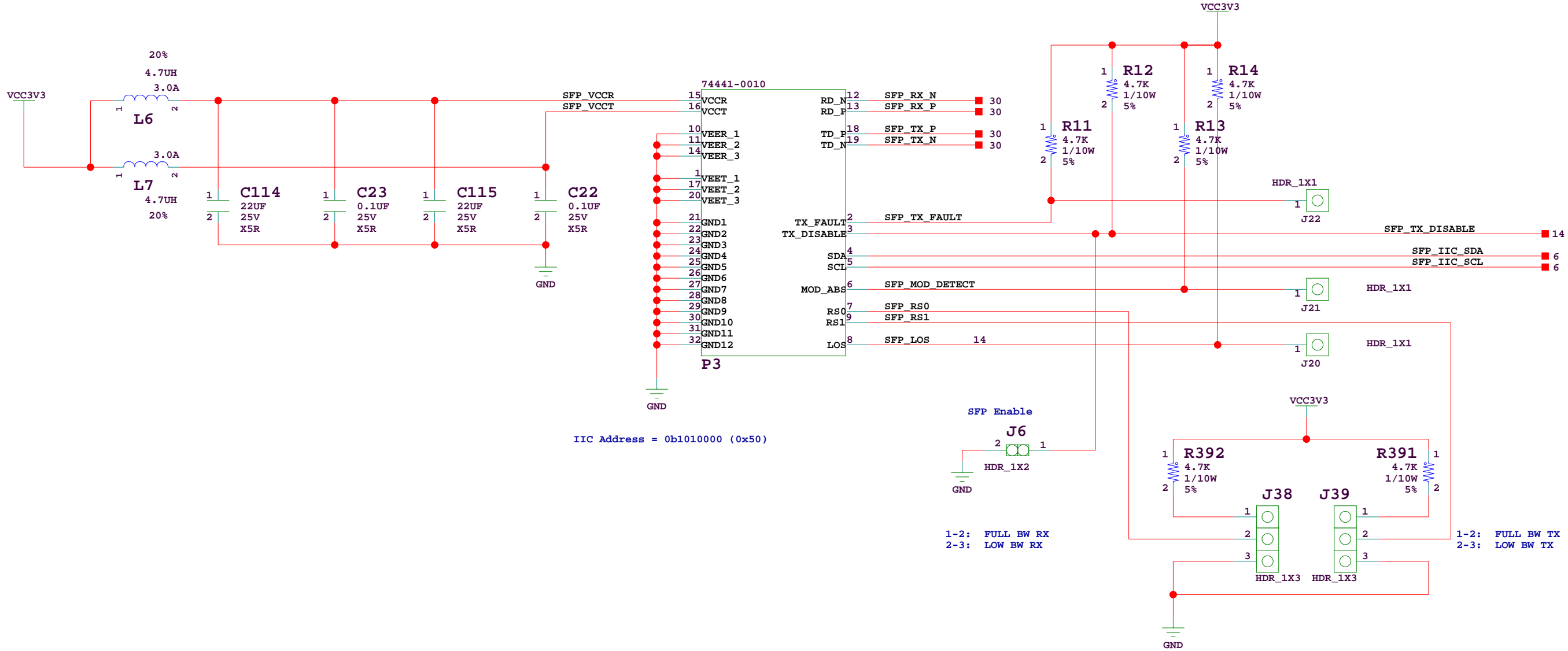
PCB P/N: 1280669
SCH P/N: 0381502

Title:SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
HDMI CONN. P2, HDMI SERIES R's


Date:2-14-2014_14:52Ver:2.0

Sheet Size: BRev: 02

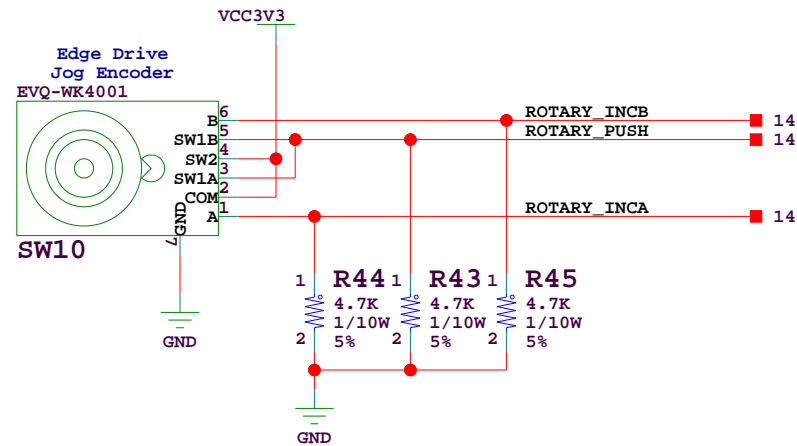
Sheet19 of 51Drawn ByDN



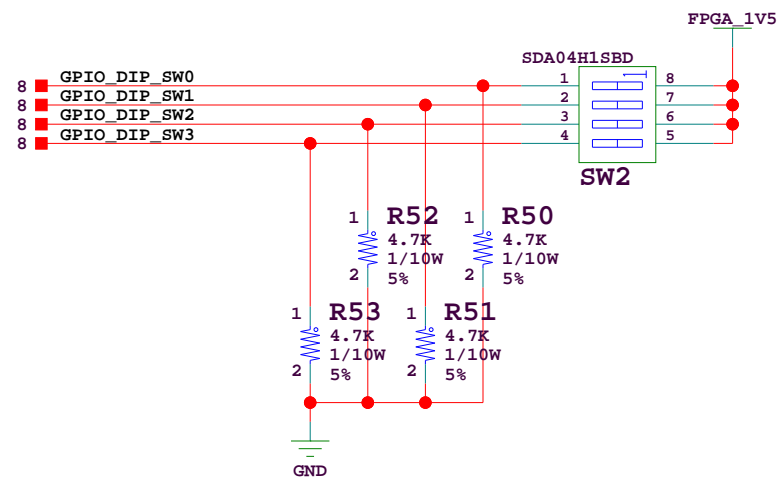
SFP+ Connector and Cage

		PCB P/N: 1280669 SCH P/N: 0381502	
Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD SFP+ CONN. P3			
Date: 2-14-2014_14:52		Ver: 2.0	
Sheet Size: B		Rev: 02	
Sheet 20 of 51		Drawn By DN	

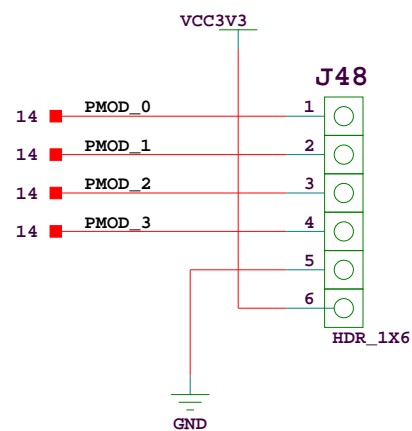
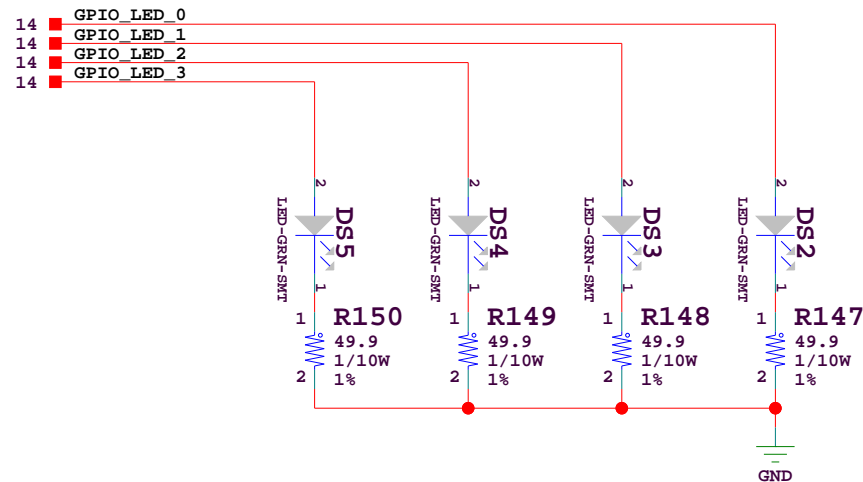
Rotary Switch



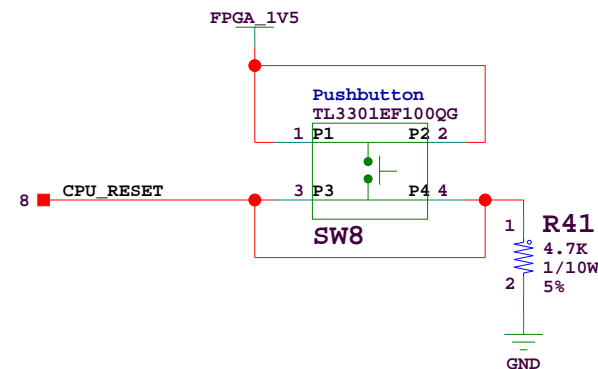
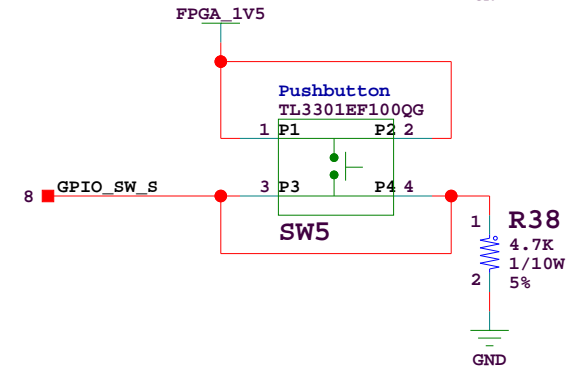
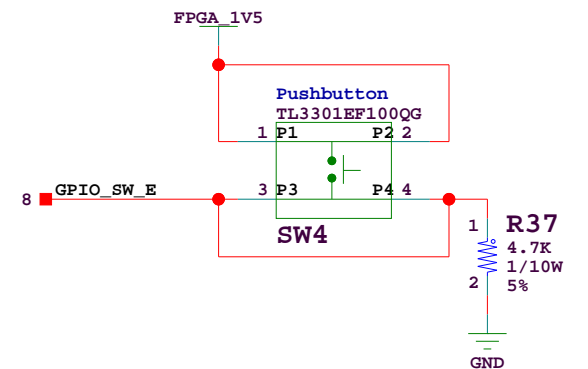
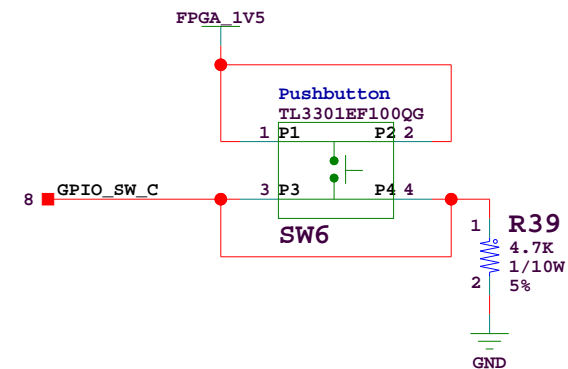
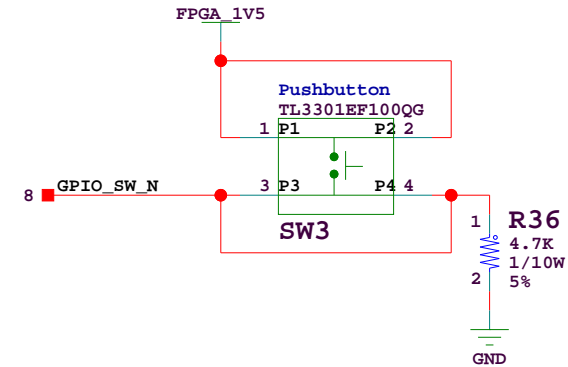
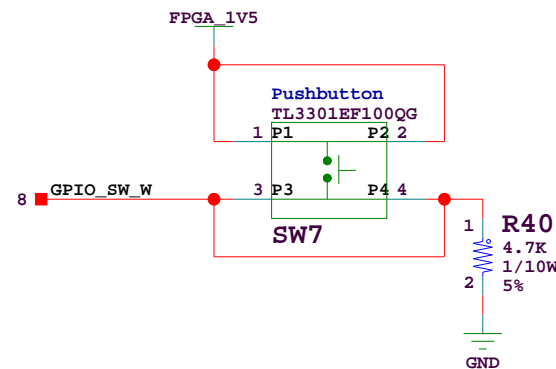
4-Pole DIP Switch



LEDs near top edge



Directional Push-Buttons



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
GPIO SWITCHES and LEDs

Date: 2-14-2014_14:52 Ver: 2.0

Sheet Size: B Rev: 02

Sheet 21 of 51 Drawn By DN

SOC_IRON_FG676

BANK 16
XC7A200TFBG676

IO_0_16_H17
IO_L1P_T0_16_H14
IO_L1N_T0_16_H15
IO_L2P_T0_16_G17
IO_L2N_T0_16_F17
IO_L3P_T0_DQS_16_F18
IO_L3N_T0_DQS_16_F19
IO_L4P_T0_16_G15
IO_L4N_T0_16_F15
IO_L5P_T0_16_G19
IO_L5N_T0_16_F20
IO_L6P_T0_16_H16
IO_L6N_T0_VREF_16_G16
IO_L7P_T1_16_C17
IO_L7N_T1_16_B17
IO_L8P_T1_16_E16
IO_L8N_T1_16_D16
IO_L9P_T1_DQS_16_A17
IO_L9N_T1_DQS_16_A18
IO_L10P_T1_16_B19
IO_L10N_T1_16_A19
IO_L11P_T1_SRCC_16_E17
IO_L11N_T1_SRCC_16_E18
IO_L12P_T1_MRCC_16_D18
IO_L12N_T1_MRCC_16_C18
IO_L13P_T2_MRCC_16_D19
IO_L13N_T2_MRCC_16_C19
IO_L14P_T2_SRCC_16_E20
IO_L14N_T2_SRCC_16_D20
IO_L15P_T2_DQS_16_B20
IO_L15N_T2_DQS_16_A20
IO_L16P_T2_16_C21
IO_L16N_T2_16_B21
IO_L17P_T2_16_B22
IO_L17N_T2_16_A22
IO_L18P_T2_16_E21
IO_L18N_T2_16_D21
IO_L19P_T3_16_C22
IO_L19N_T3_VREF_16_C23
IO_L20P_T3_16_B25
IO_L20N_T3_16_A25
IO_L21P_T3_DQS_16_A23
IO_L21N_T3_DQS_16_A24
IO_L22P_T3_16_C26
IO_L22N_T3_16_B26
IO_L23P_T3_16_C24
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IO_L24P_T3_16_D23
IO_L24N_T3_16_D24
IO_25_16_E22

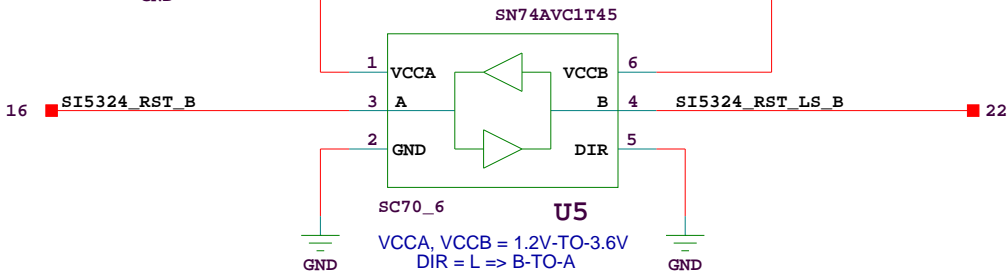
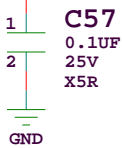
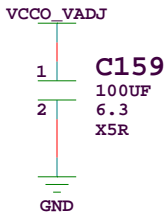
H17 XADC_GPIO_0 29
H14 FMC1_HPC_LA02_P 26
H15 FMC1_HPC_LA02_N 26
G17 FMC1_HPC_LA03_P 26
F17 FMC1_HPC_LA03_N 25
F18 FMC1_HPC_LA04_P 25
F19 FMC1_HPC_LA04_N 26
G15 FMC1_HPC_LA05_P 24
F15 FMC1_HPC_LA05_N 24
G19 FMC1_HPC_LA06_P 24
F20 FMC1_HPC_LA06_N 24
H16 FMC1_HPC_LA07_P 26
G16 FMC1_HPC_LA07_N 26
C17 FMC1_HPC_LA08_P 25
B17 FMC1_HPC_LA08_N 25
E16 FMC1_HPC_LA09_P 24
D16 FMC1_HPC_LA09_N 24
A17 FMC1_HPC_LA10_P 24
A18 FMC1_HPC_LA10_N 24
B19 FMC1_HPC_LA11_P 26
A19 FMC1_HPC_LA11_N 26
E17 FMC1_HPC_LA01_CC_P 24
E18 FMC1_HPC_LA01_CC_N 24
D18 FMC1_HPC_LA00_CC_P 24
C18 FMC1_HPC_LA00_CC_N 25
D19 FMC1_HPC_CLK0_M2C_P 25
C19 FMC1_HPC_CLK0_M2C_N 26
E20 FMC1_HPC_LA12_P 25
D20 FMC1_HPC_LA12_N 25
B20 FMC1_HPC_LA13_P 24
A20 FMC1_HPC_LA13_N 24
C21 FMC1_HPC_LA14_P 24
B21 FMC1_HPC_LA14_N 24
B22 FMC1_HPC_LA15_P 26
A22 FMC1_HPC_LA15_N 26
E21 FMC1_HPC_LA16_P 25
D21 FMC1_HPC_LA16_N 25
C22 NC 25
C23 NC 25
B25 XADC_MUX_ADDR0_LS 37
A25 XADC_MUX_ADDR1_LS 37
A23 XADC_MUX_ADDR2_LS 37
A24 PCIE_MGT_CLK_SEL0 30
C26 PCIE_MGT_CLK_SEL1 30
B26 SFP_MGT_CLK_SEL0 30
C24 SFP_MGT_CLK_SEL1 30
B24 SI5324_RST_LS_B 22
D23 REC_CLOCK_C_P 16
D24 REC_CLOCK_C_N 16
E22 XADC_GPIO_1 29

VCCO_VADJ

F16 VCCO_16_F16
E19 VCCO_16_E19
D22 VCCO_16_D22
C25 VCCO_16_C25
B18 VCCO_16_B18
A21 VCCO_16_A21

U1

SOC_IRON_FG676



SOC_IRON_FG676

BANK 15
XC7A200TFBG676

IO_0_15_K18
IO_L1P_T0_AD0P_15_K15
IO_L1N_T0_AD0N_15_J16
IO_L2P_T0_AD8P_15_J14
IO_L2N_T0_AD8N_15_J15
IO_L3P_T0_DQS_AD1P_15_K16
IO_L3N_T0_DQS_AD1N_15_K17
IO_L4P_T0_15_M14
IO_L4N_T0_15_L14
IO_L5P_T0_AD9P_15_M15
IO_L5N_T0_AD9N_15_L15
IO_L6P_T0_15_M16
IO_L6N_T0_VREF_15_M17
IO_L7P_T1_AD2P_15_J19
IO_L7N_T1_AD2N_15_H19
IO_L8P_T1_AD10P_15_L17
IO_L8N_T1_AD10N_15_L18
IO_L9P_T1_DQS_AD3P_15_K20
IO_L9N_T1_DQS_AD3N_15_J20
IO_L10P_T1_AD11P_15_J18
IO_L10N_T1_AD11N_15_H18
IO_L11P_T1_SRCC_15_G20
IO_L11N_T1_SRCC_15_G21
IO_L12P_T1_MRCC_15_K21
IO_L12N_T1_MRCC_15_J21
IO_L13P_T2_MRCC_15_H21
IO_L13N_T2_MRCC_15_H22
IO_L14P_T2_SRCC_15_J23
IO_L14N_T2_SRCC_15_H23
IO_L15P_T2_DQS_ADV_B_15_G22
IO_L15N_T2_DQS_ADV_B_15_F22
IO_L16P_T2_A28_15_J24
IO_L16N_T2_A27_15_H24
IO_L17P_T2_A26_15_F23
IO_L17N_T2_A25_15_E23
IO_L18P_T2_A24_15_K22
IO_L18N_T2_A23_15_K23
IO_L19P_T3_A22_15_G24
IO_L19N_T3_A21_VREF_15_F24
IO_L20P_T3_A20_15_E25
IO_L20N_T3_A19_15_D25
IO_L21P_T3_DQS_15_E26
IO_L21N_T3_DQS_A18_15_D26
IO_L22P_T3_A17_15_H26
IO_L22N_T3_A16_15_G26
IO_L23P_T3_FOE_B_15_G25
IO_L23N_T3_FWE_B_15_F25
IO_L24P_T3_RS1_15_J25
IO_L24N_T3_RS0_15_J26
IO_25_15_L19

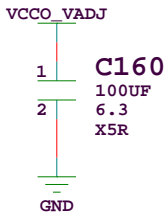
K18 XADC_GPIO_2 29
K15 XADC_VAUX0_R_P 29
J16 XADC_VAUX0_R_N 29
J14 XADC_VAUX8_R_P 29
J15 XADC_VAUX8_R_N 29
K16 XADC_AD1_R_P 37
K17 XADC_AD1_R_N 37
M14 FMC1_HPC_LA19_P 26
L14 FMC1_HPC_LA19_N 26
M15 XADC_AD9_R_P 37
L15 XADC_AD9_R_N 37
M16 FMC1_HPC_LA20_P 25
M17 FMC1_HPC_LA20_N 25
J19 FMC1_HPC_LA21_P 26
H19 FMC1_HPC_LA21_N 26
L17 FMC1_HPC_LA22_P 25
L18 FMC1_HPC_LA22_N 25
K20 FMC1_HPC_LA23_P 24
J20 FMC1_HPC_LA23_N 24
J18 FMC1_HPC_LA24_P 26
H18 FMC1_HPC_LA24_N 26
G20 FMC1_HPC_LA18_CC_P 24
G21 FMC1_HPC_LA18_CC_N 24
K21 FMC1_HPC_LA17_CC_P 24
J21 FMC1_HPC_LA17_CC_N 24
H21 FMC1_HPC_CLK1_M2C_P 25
H22 FMC1_HPC_CLK1_M2C_N 25
J23 USER_SMA_CLOCK_P 3
H23 USER_SMA_CLOCK_N 3
G22 FMC1_HPC_LA25_P 25
F22 FMC1_HPC_LA25_N 25
J24 FMC1_HPC_LA26_P 24
H24 FMC1_HPC_LA26_N 24
F23 FMC1_HPC_LA27_P 24
E23 FMC1_HPC_LA27_N 24
K22 FMC1_HPC_LA28_P 26
K23 FMC1_HPC_LA28_N 26
G24 FMC1_HPC_LA29_P 25
F24 FMC1_HPC_LA29_N 25
E25 FMC1_HPC_LA30_P 26
D25 FMC1_HPC_LA30_N 26
E26 FMC1_HPC_LA31_P 25
D26 FMC1_HPC_LA31_N 25
H26 FMC1_HPC_LA32_P 26
G26 FMC1_HPC_LA32_N 26
G25 FMC1_HPC_LA33_P 25
F25 FMC1_HPC_LA33_N 25
J25 SM_FAN_TACH 38
J26 SM_FAN_PWM 38
L19 XADC_GPIO_3 29

VCCO_VADJ

M18 VCCO_15_M18
K14 VCCO_15_K14
J17 VCCO_15_J17
H20 VCCO_15_H20
G23 VCCO_15_G23
F26 VCCO_15_F26

U1

SOC_IRON_FG676



PCB P/N: 1280669
SCH P/N: 0381502

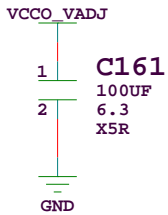
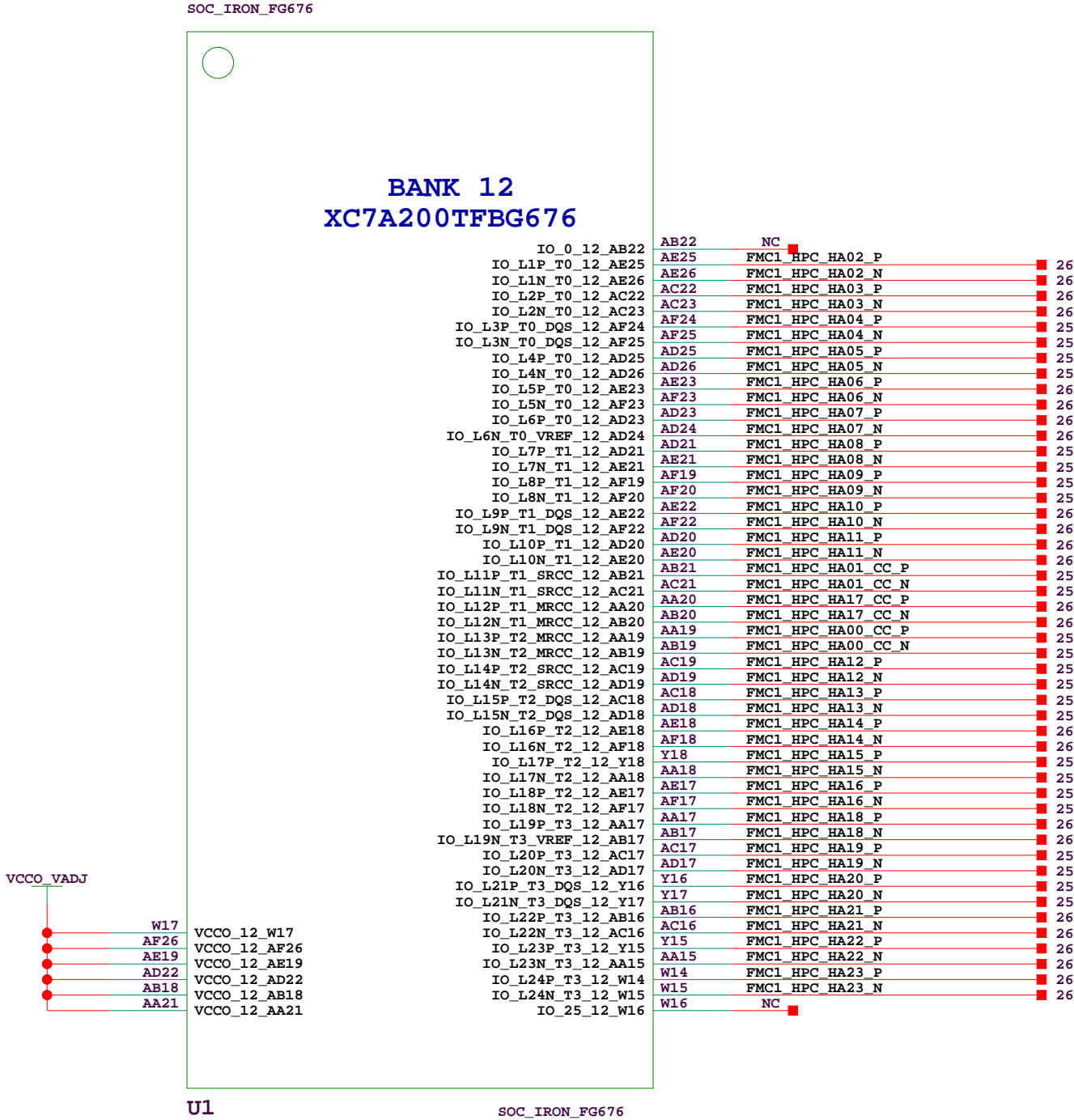
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
BANKS15,16 HPC FMC and XADC IF

Date: 2-14-2014_14:52 Ver: 2.0

Sheet Size: B Rev: 02

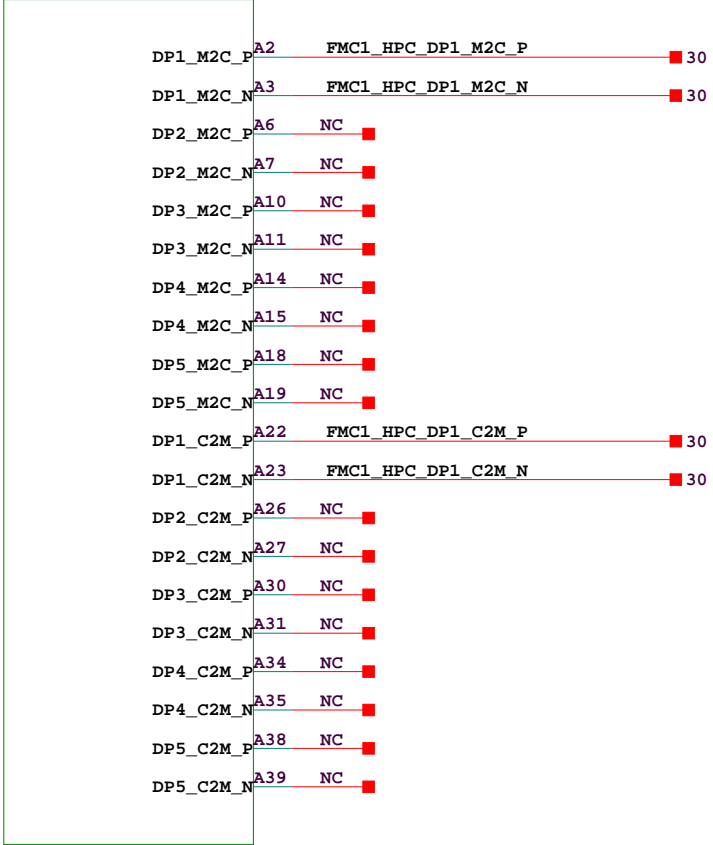
Sheet 22 of 51 Drawn By DN

XC7A200T-FBG676 ONLY



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANK12 HPC FMC IF	
Date: 2-14-2014_14:52	Ver: 2.0
Sheet Size: B	Rev: 02
Sheet 23 of 51	Drawn By DN

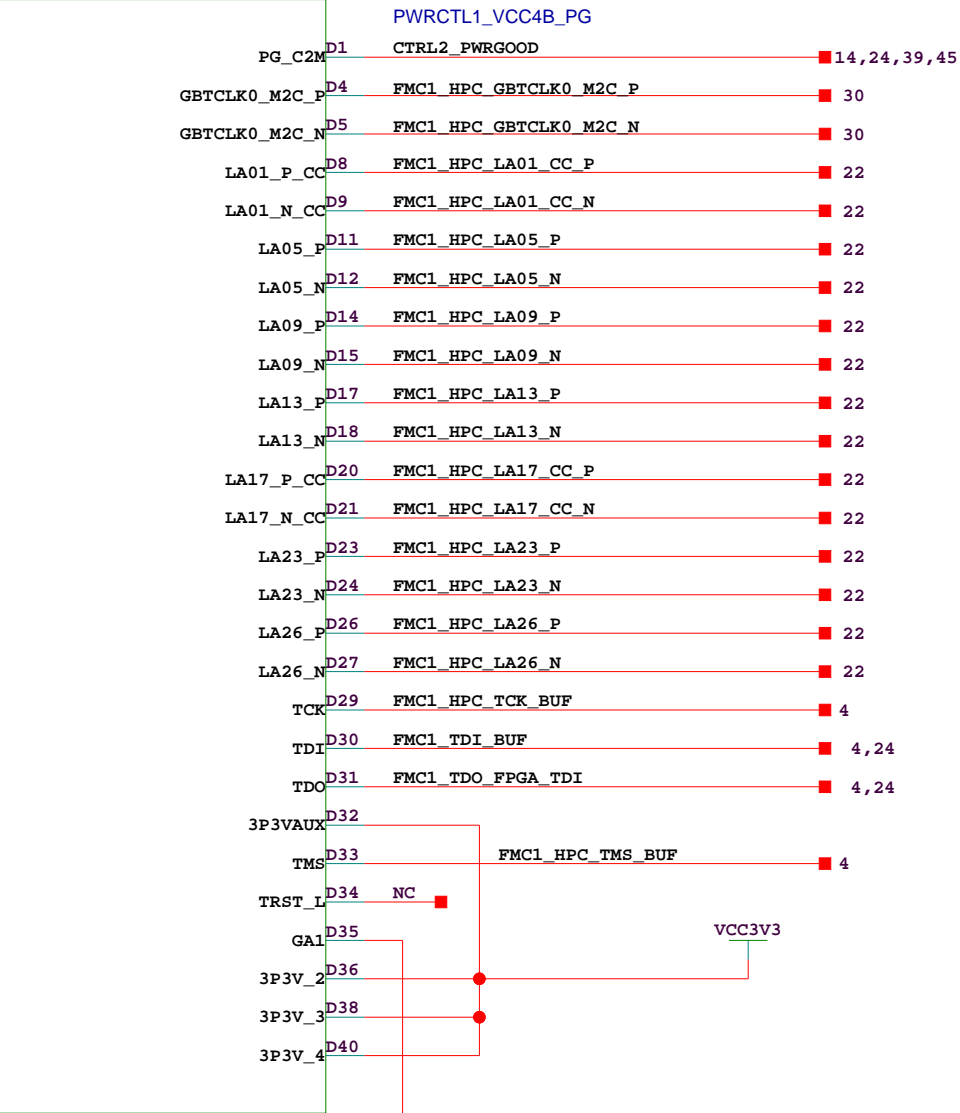


J30
ASP_134486_01

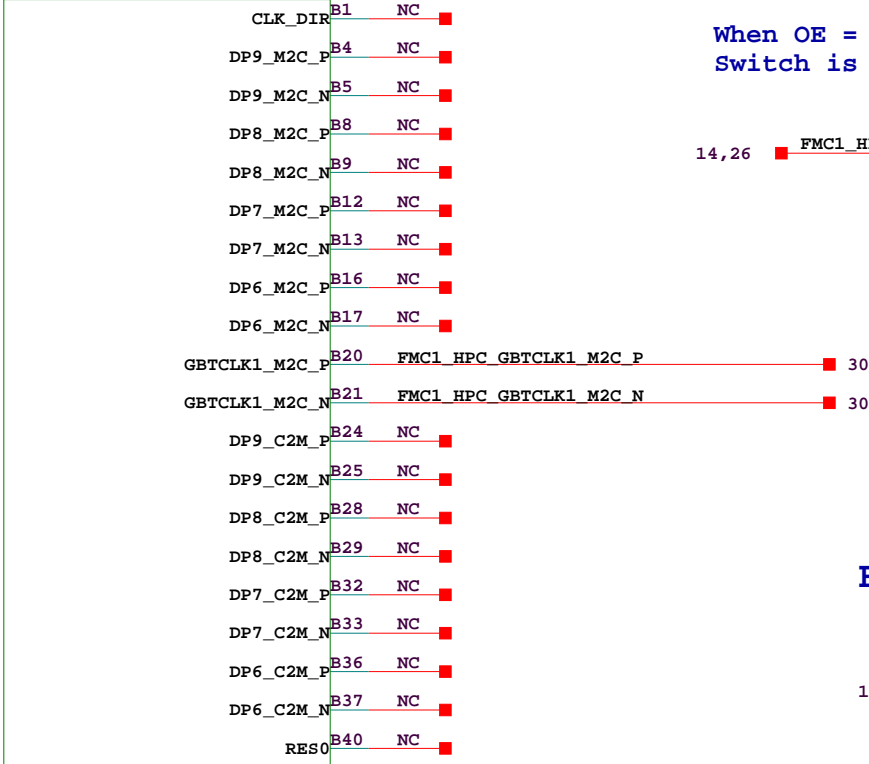


J30
ASP_134486_01

IIC Address = 0bxxxxxx00

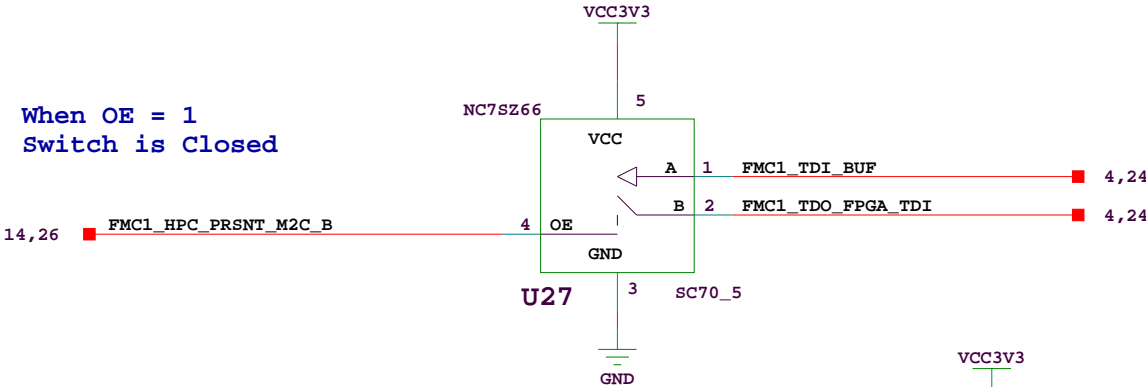


J30
ASP_134486_01



J30
ASP_134486_01

When OE = 1
Switch is Closed



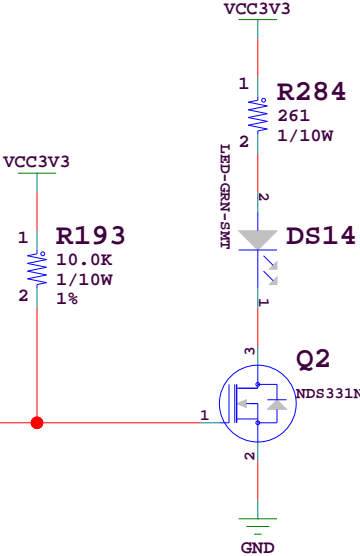
FMC Power Good

14,24,39,45


CTRL2_PWRGOOD

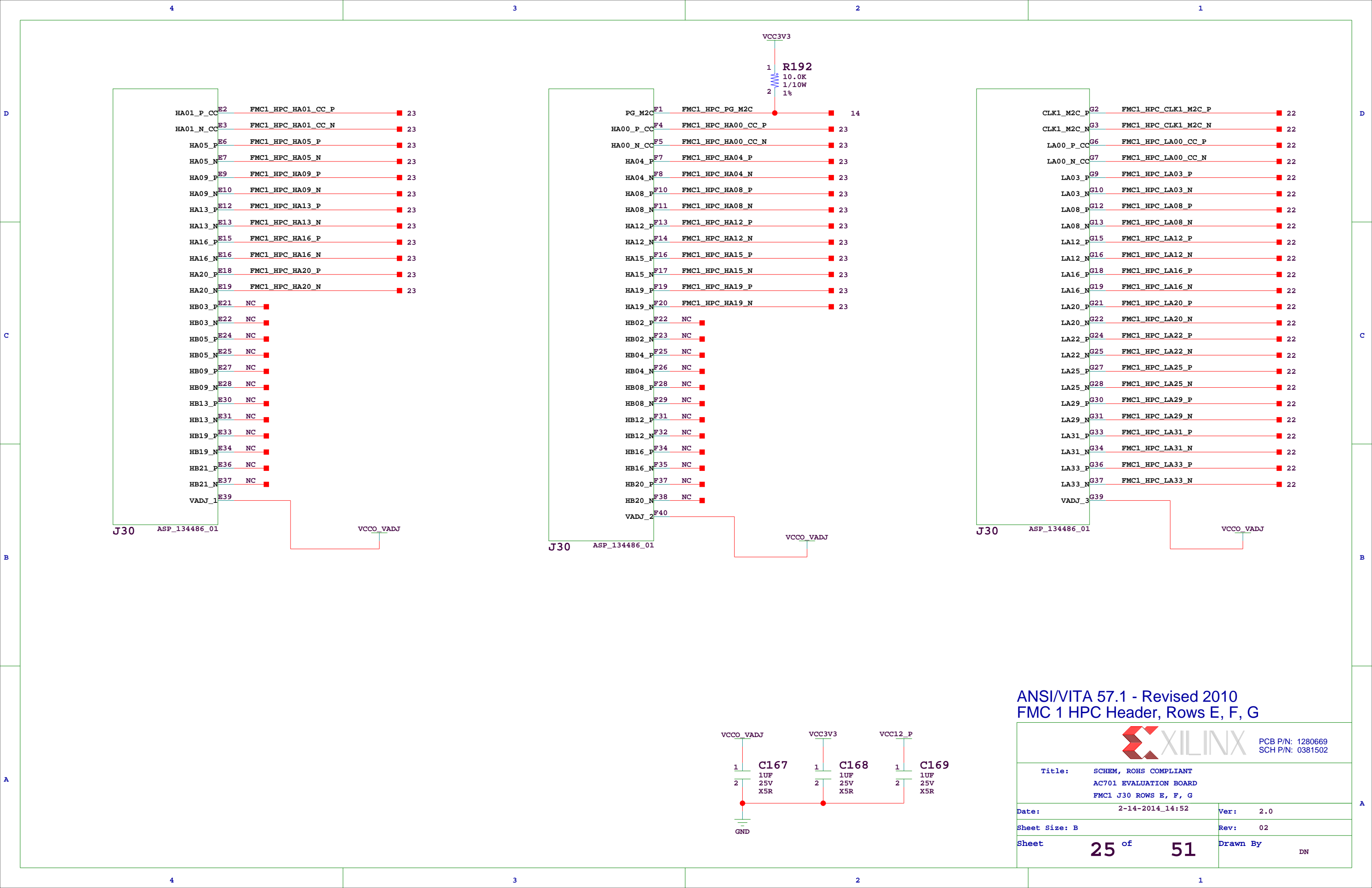
PWRCTL1_VCC4B_PG

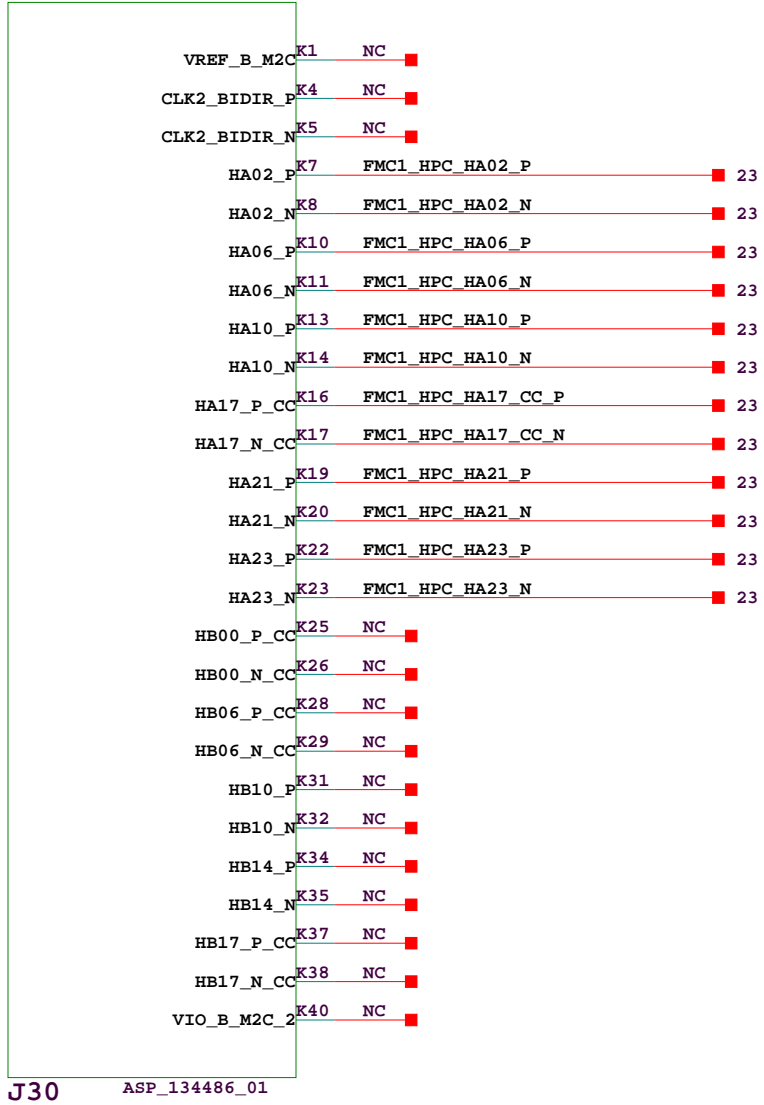
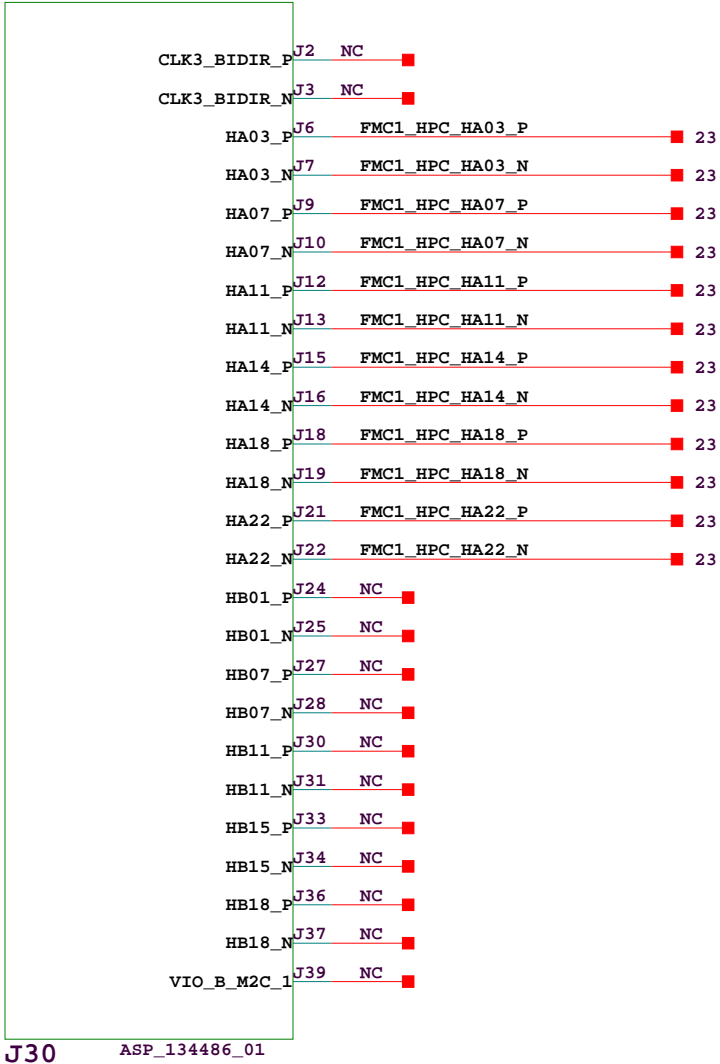
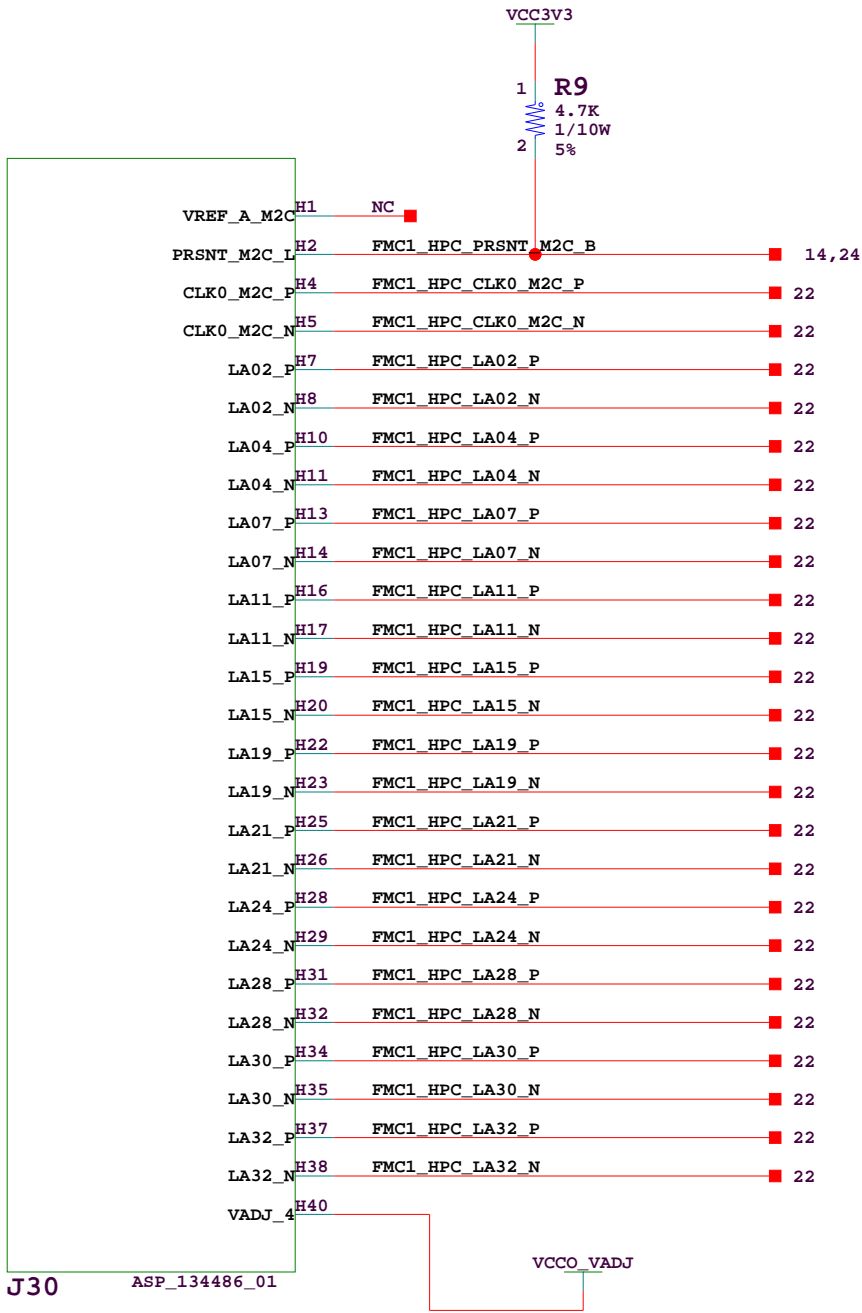
CTRL2_PWRGOOD from TI controller U9
indicates both VCC3V3 and VCCO_VADJ
FMC power rails are OK




ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows A, B, C, D

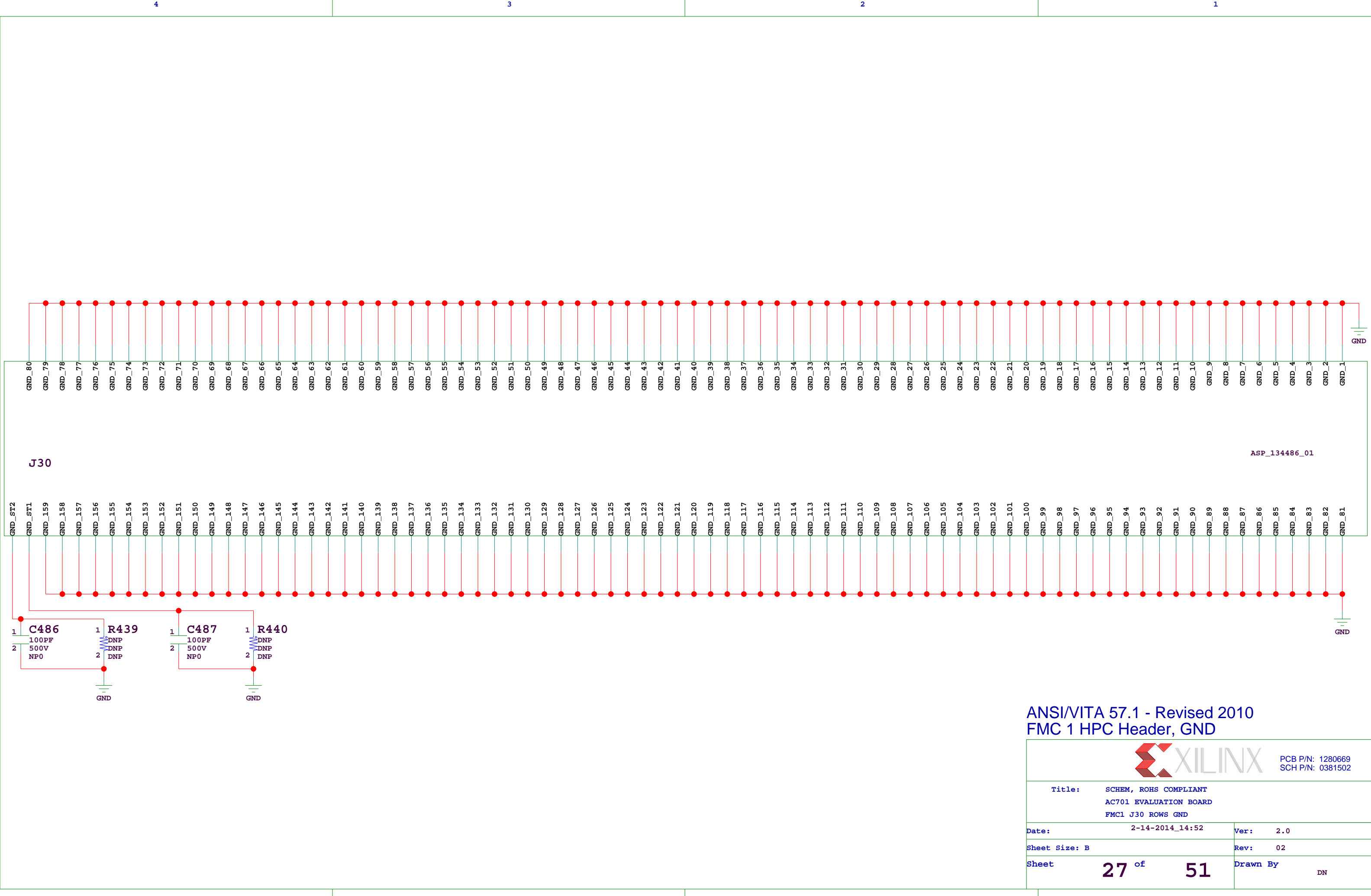
		PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS A, B, C, D	
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	24 of 51	Drawn By	DN





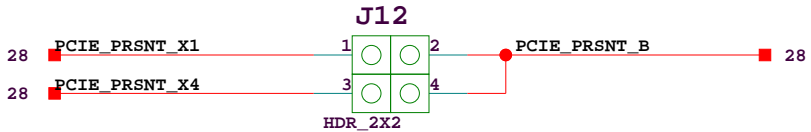
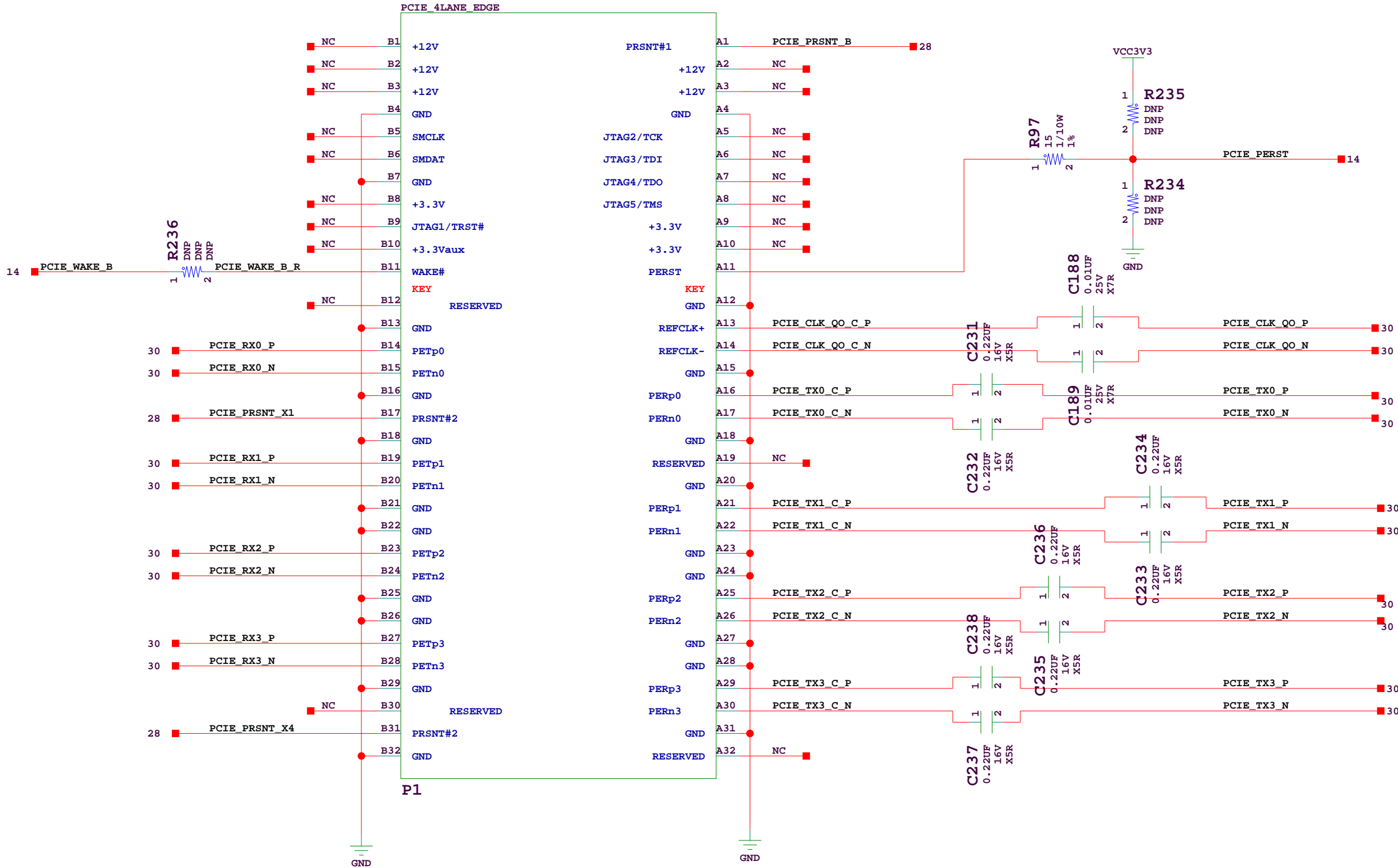
ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows H, J, K

		PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS H, J, K	
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	26 of 51	Drawn By	DN




ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, GND

<div><div>XILINX</div><div>PCB P/N: 1280669 SCH P/N: 0381502</div></div>	
Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS GND	
Date: 2-14-2014_14:52	Ver: 2.0
Sheet Size: B	Rev: 02
Sheet 27 of 51	Drawn By DN



PCIE 4X Card Edge

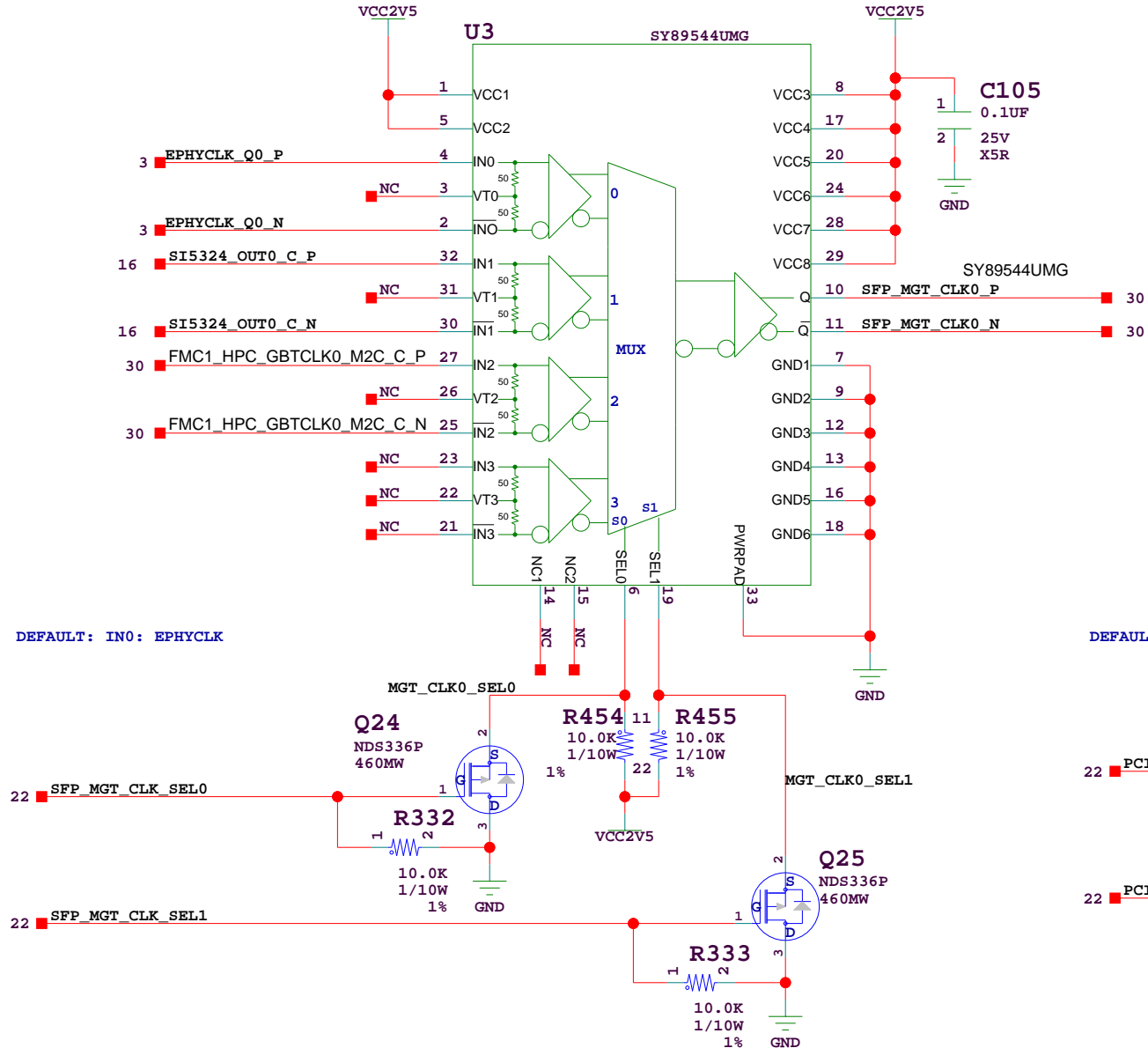
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Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD PCIe 4X CARD EDGE CONN. P1			
Date: 2-14-2014_14:52		Ver: 2.0	
Sheet Size: B		Rev: 02	
Sheet 28 of 51		Drawn By DN	

BANK 213
XC7A200TFBG676

MGTPTXP0_213_AC10	SFP_TX_P	20
MGTPTXN0_213_AD10	SFP_TX_N	20
MGTPRXP0_213_AC12	SFP_RX_P	20
MGTPRXN0_213_AD12	SFP_RX_N	20
MGTPTXP1_213_AE9	FMC1_HPC_DP0_C2M_P	24
MGTPTXN1_213_AF9	FMC1_HPC_DP0_C2M_N	24
MGTPRXP1_213_AE13	FMC1_HPC_DP0_M2C_P	24
MGTPRXN1_213_AF13	FMC1_HPC_DP0_M2C_N	24
MGTPTXP2_213_AC8	FMC1_HPC_DP1_C2M_P	24
MGTPTXN2_213_AD8	FMC1_HPC_DP1_C2M_N	24
MGTPRXP2_213_AC14	FMC1_HPC_DP1_M2C_P	24
MGTPRXN2_213_AD14	FMC1_HPC_DP1_M2C_N	24
MGTPTXP3_213_AE7	SMA_MGT_TX_P	3
MGTPTXN3_213_AF7	SMA_MGT_TX_N	3
MGTPRXP3_213_AE11	SMA_MGT_RX_P	3
MGTPRXN3_213_AF11	SMA_MGT_RX_N	3
MGTPRXN3_213_AF11	AA13	3
MGTRREFCLK0P_213_AA13	SFP_MGT_CLK0_C_P	30
MGTRREFCLK0N_213_AB13	SFP_MGT_CLK0_C_N	30
MGTRREFCLK1P_213_AA11	SFP_MGT_CLK1_C_P	30
MGTRREFCLK1N_213_AB11	SFP_MGT_CLK1_C_N	30
MGTRREF_213_AF15	MGTRREF_213	30

U1

SOC_IRON_FG676



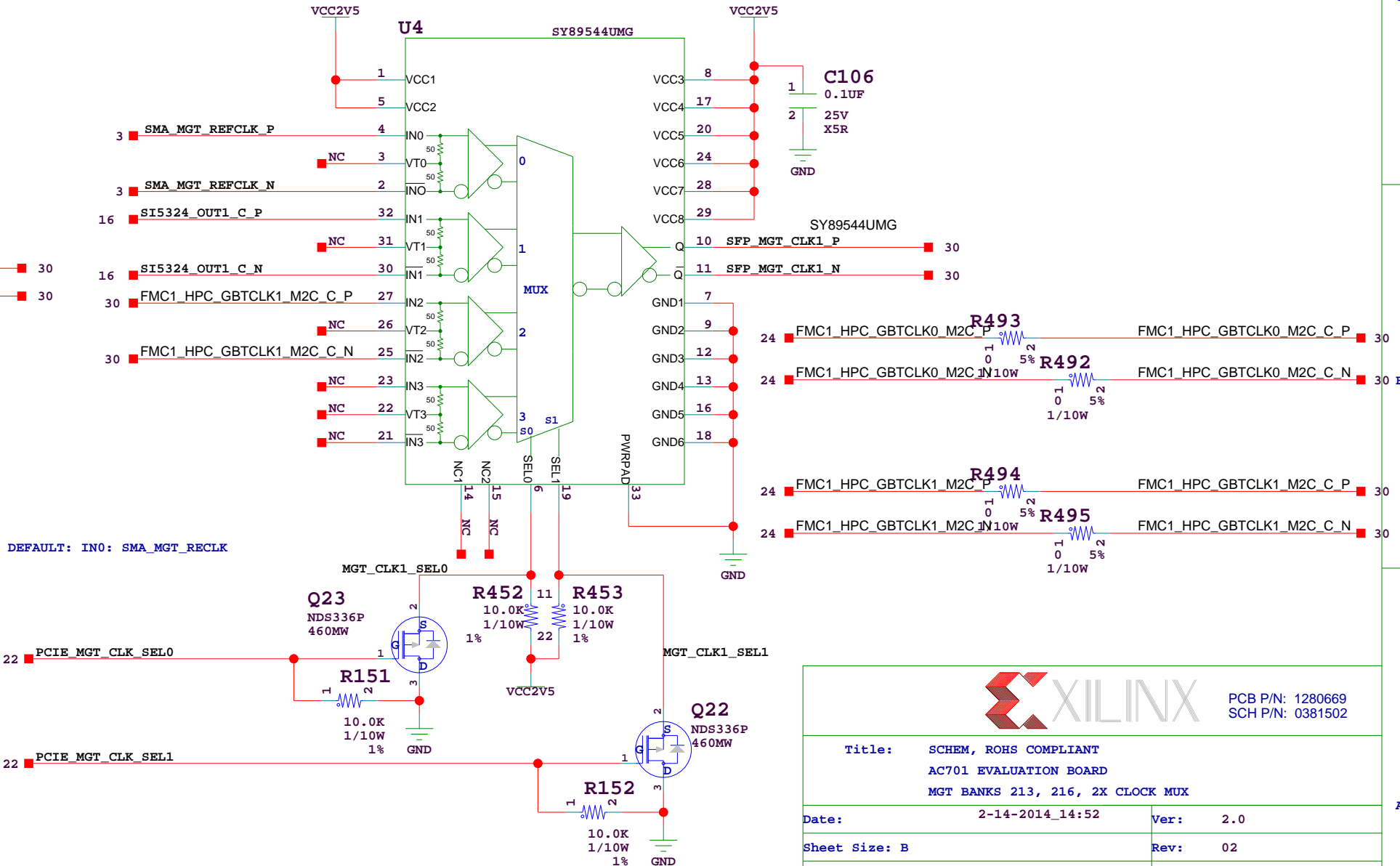
DEFAULT: IN0: EPHYCLK

BANK 216
XC7A200TFBG676

MGTPTXP0_216_B7	PCIE_TX3_P	28
MGTPTXN0_216_A7	PCIE_TX3_N	28
MGTPRXP0_216_B11	PCIE_RX3_P	28
MGTPRXN0_216_A11	PCIE_RX3_N	28
MGTPTXP1_216_D8	PCIE_TX2_P	28
MGTPTXN1_216_C8	PCIE_TX2_N	28
MGTPRXP1_216_D14	PCIE_RX2_P	28
MGTPRXN1_216_C14	PCIE_RX2_N	28
MGTPTXP2_216_B9	PCIE_TX1_P	28
MGTPTXN2_216_A9	PCIE_TX1_N	28
MGTPRXP2_216_B13	PCIE_RX1_P	28
MGTPRXN2_216_A13	PCIE_RX1_N	28
MGTPTXP3_216_D10	PCIE_TX0_P	28
MGTPTXN3_216_C10	PCIE_TX0_N	28
MGTPRXP3_216_D12	PCIE_RX0_P	28
MGTPRXN3_216_C12	PCIE_RX0_N	28
MGTRREFCLK0P_216_F11	PCIE_CLK_QO_P	28
MGTRREFCLK0N_216_E11	PCIE_CLK_QO_N	28
MGTRREFCLK1P_216_F13	NC	28
MGTRREFCLK1N_216_E13	NC	28
MGTRREF_216_A15	MGTRREF_216	28

U1

SOC_IRON_FG676



DEFAULT: IN0: SMA_MGT_RECLK

PCB P/N: 1280669
SCH P/N: 0381502Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
MGT BANKS 213, 216, 2X CLOCK MUX

Date: 2-14-2014_14:52

Ver: 2.0

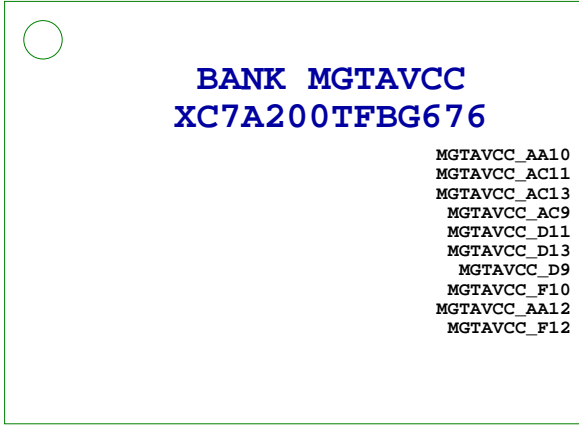
Sheet Size: B

Rev: 02

Sheet 30 of 51

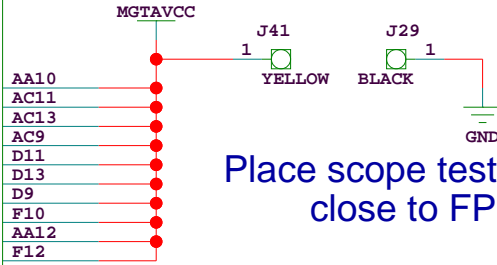
Drawn By DN

SOC_IRON_FG676



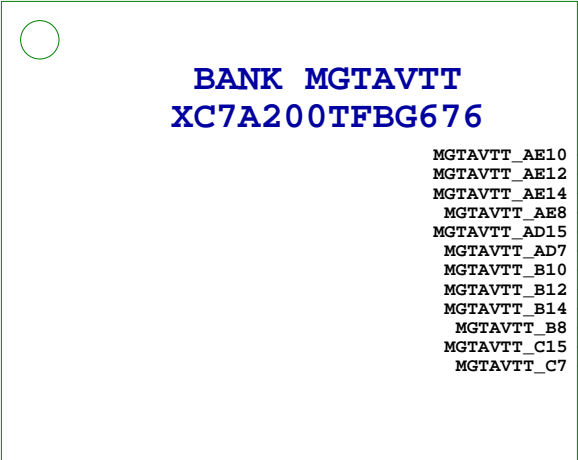
U1

SOC_IRON_FG676



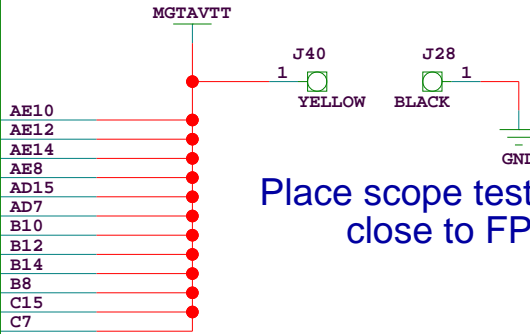
Place scope test points
close to FPGA

SOC_IRON_FG676

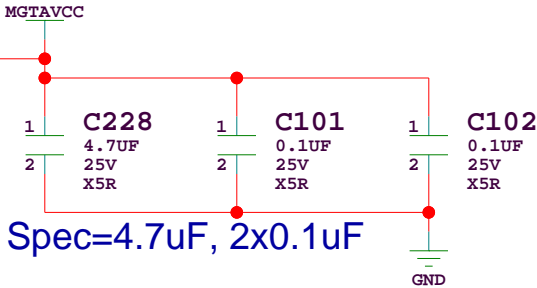


U1

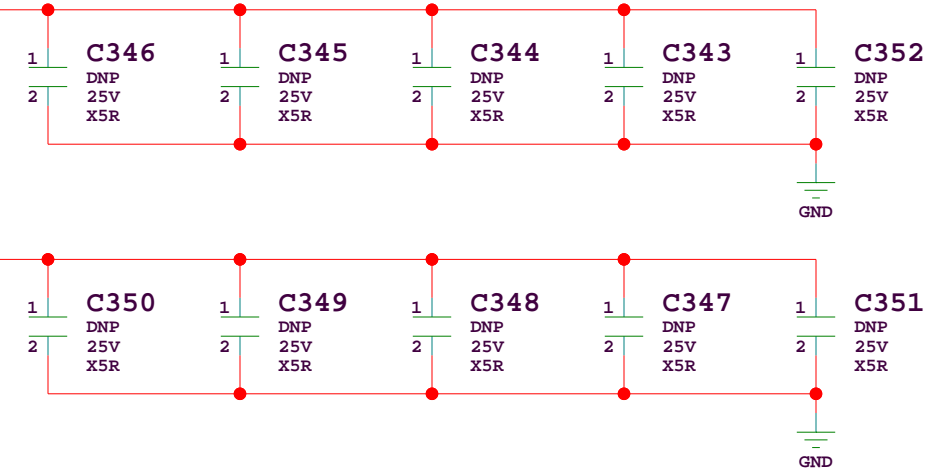
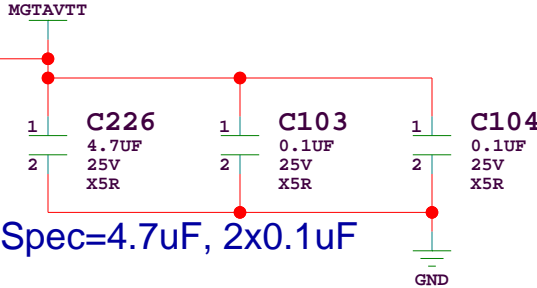
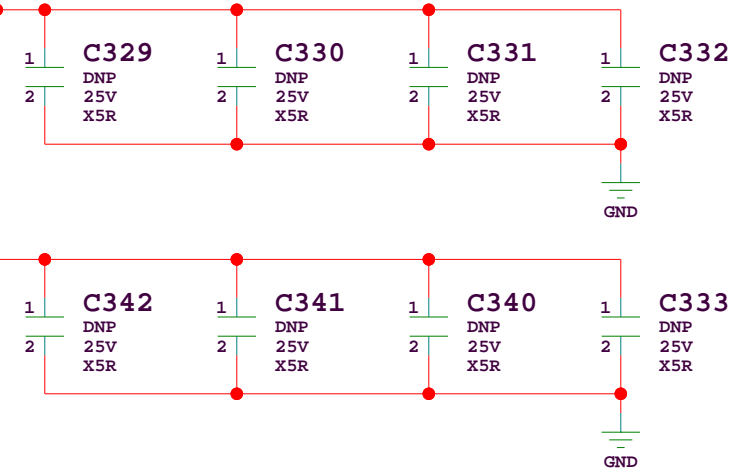
SOC_IRON_FG676



Place scope test points
close to FPGA



Place MGT 0.1uF caps within
the FPGA via field on the bottom
of the board, one for each
MGT power pin/GND pin pair



PCB P/N: 1280669
SCH P/N: 0381502

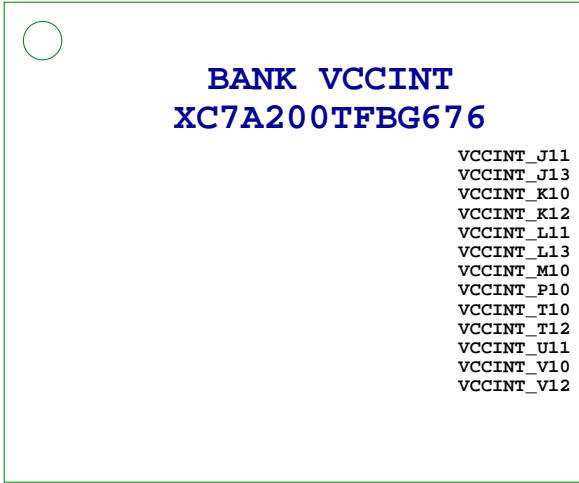
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
MGT PWR. BANKS AVCC and AVTT

Date: 2-14-2014_14:52 Ver: 2.0

Sheet Size: B Rev: 02

Sheet 31 of 51 Drawn By DN

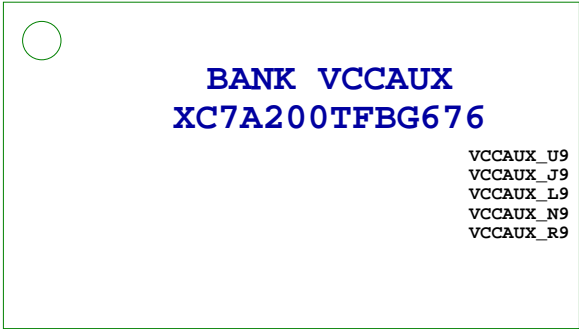
SOC_IRON_FG676



U1

SOC_IRON_FG676

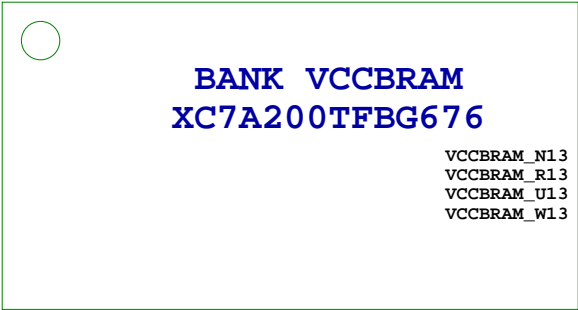
SOC_IRON_FG676



U1

SOC_IRON_FG676

SOC_IRON_FG676

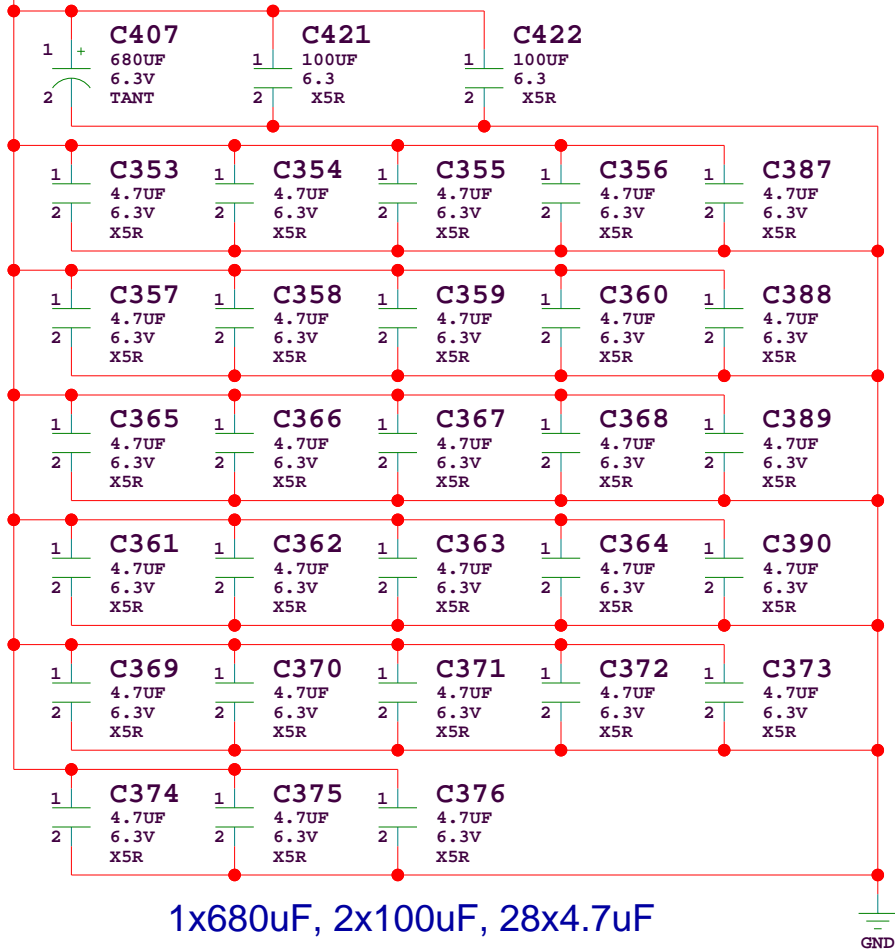


U1

SOC_IRON_FG676

VCCINT

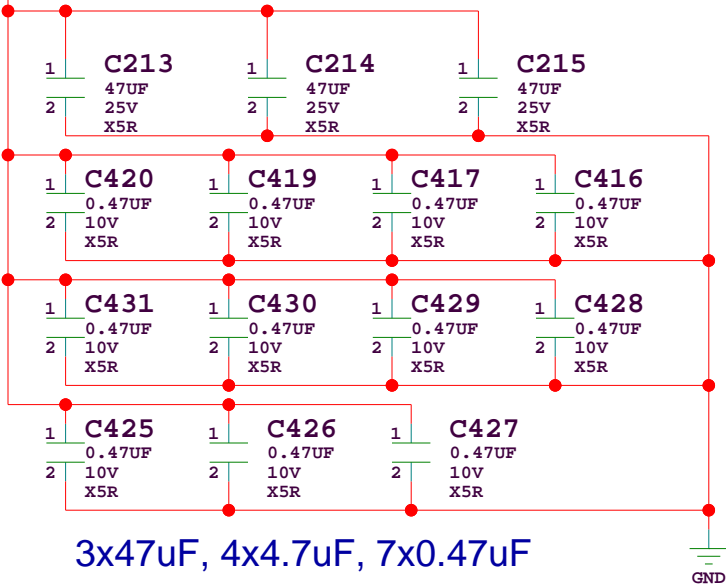
VCCINT



1x680uF, 2x100uF, 28x4.7uF
42x0.47uF on PG.34

VCCAUX

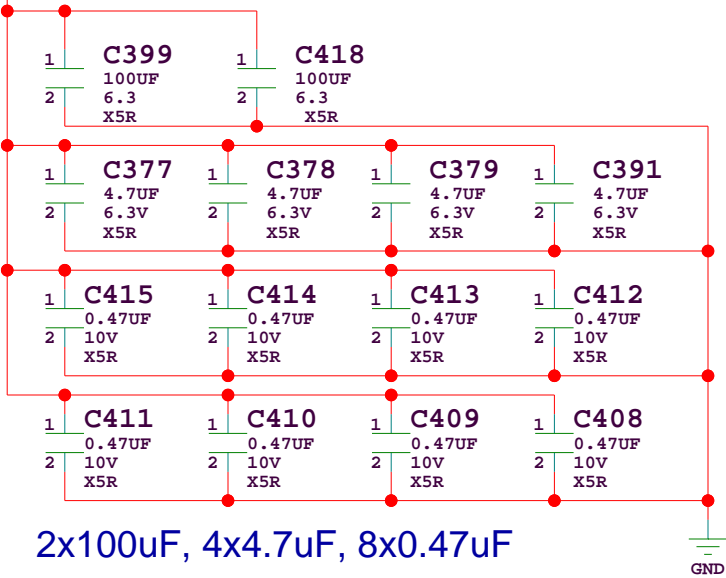
VCCAUX



3x47uF, 4x4.7uF, 7x0.47uF

VCCBRAM

VCCBRAM



2x100uF, 4x4.7uF, 8x0.47uF



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
FPGA CORE PWR. BANKS

Date: 2-14-2014_14:52

Ver: 2.0

Sheet Size: B

Rev: 02

Sheet

32

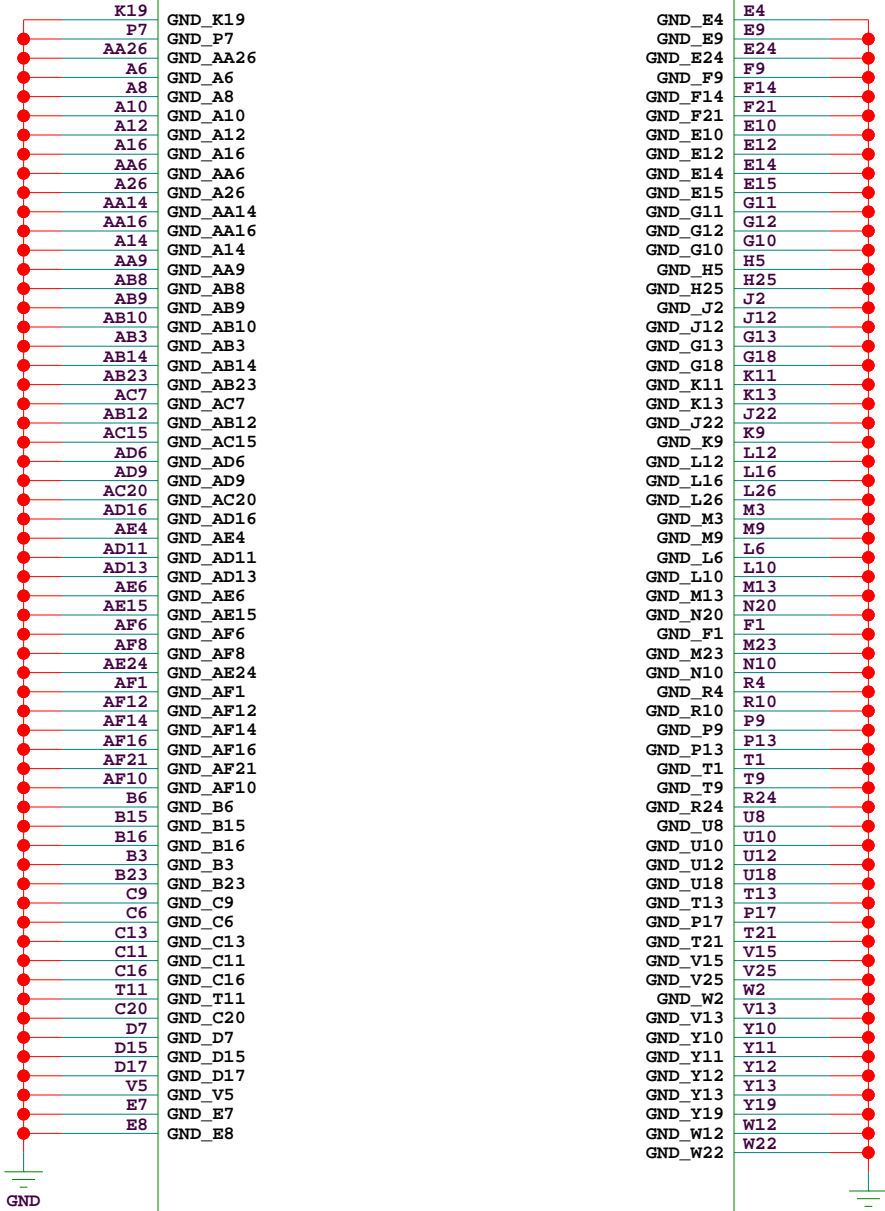
of

51

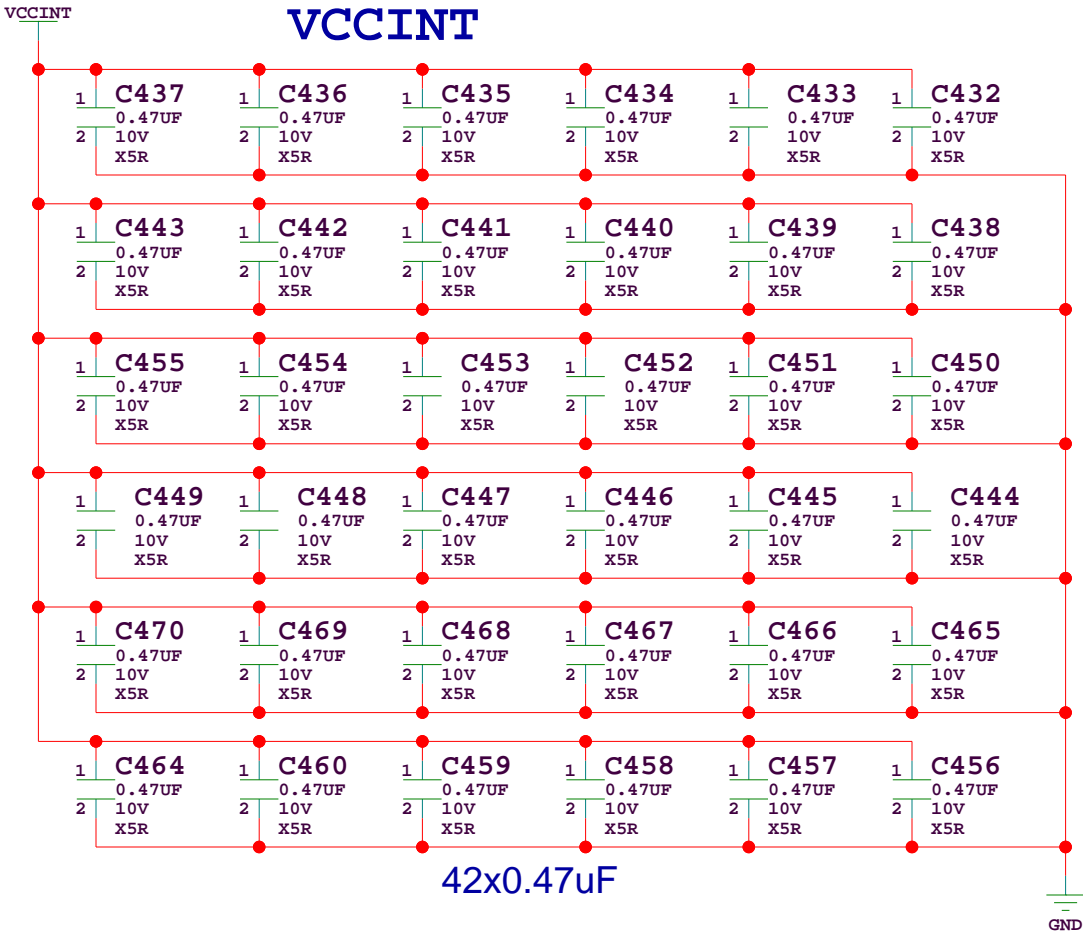
Drawn By

DN

BANK GND
XC7A200TFBG676



VCCINT



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
FPGA PWR. BANK GND

Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size: B		Rev:	02
Sheet	33 of 51	Drawn By	DN

XADC I/F MONITORING CIRCUIT PAGE 1

VCCINT 0A-10A => CS = 0V - 1.009V G=20, Rg=5.21K
VCCINT 0A-4A => CS = 0V - 0.996V G=50, Rg=2.05K
J11 ON = 4A RANGE
J11 OFF = 10A RANGE

Rsense
IR drop

CHAN. 1

VCCAUX 0A-6.0A => CS = 0V - 0.9124V
G=30, Rg=3.40K

CHAN. 2

VCCBRAM 0A-1.8A => CS = 0V - 0.9090V
G=100, Rg=1.00K

CHAN. 3

FPGA_1V5 0A-6.0A => CS = 0V - 0.6036V
G=20, Rg=5.23K

CHAN. 4

CONTROLLER #1&2
OP AMP SUPPLY


Note 1: See LMZ31704 datasheet
pg. 26 for Vin and Vout CAP layouts

Note 2: See LMZ31704
datasheet pg. 26 for PH
copper island layout

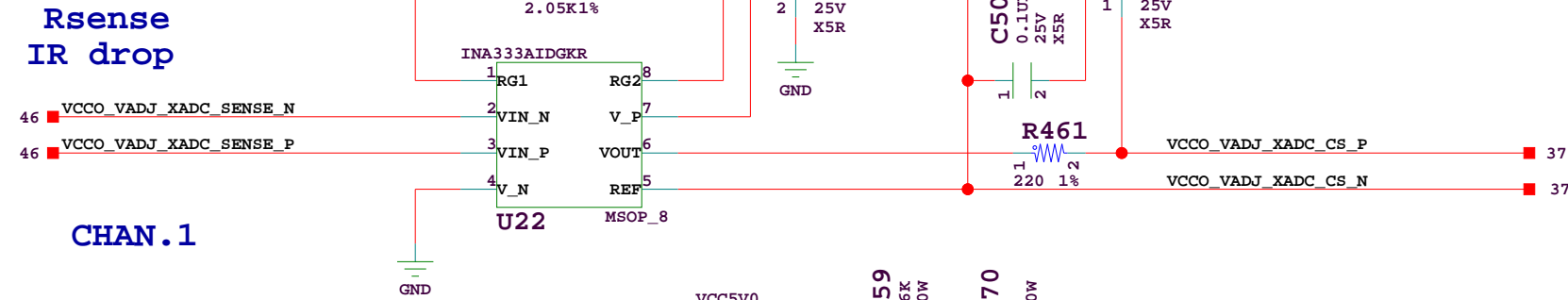
Note 3: No external AGND-to-PGND
is required for the LMZ31704
per TI on 2-7-2014

Note 4:
See LMZ31704 datasheet
pg. 26 for Rset resistor
placement close to package
between pins 26 and 23

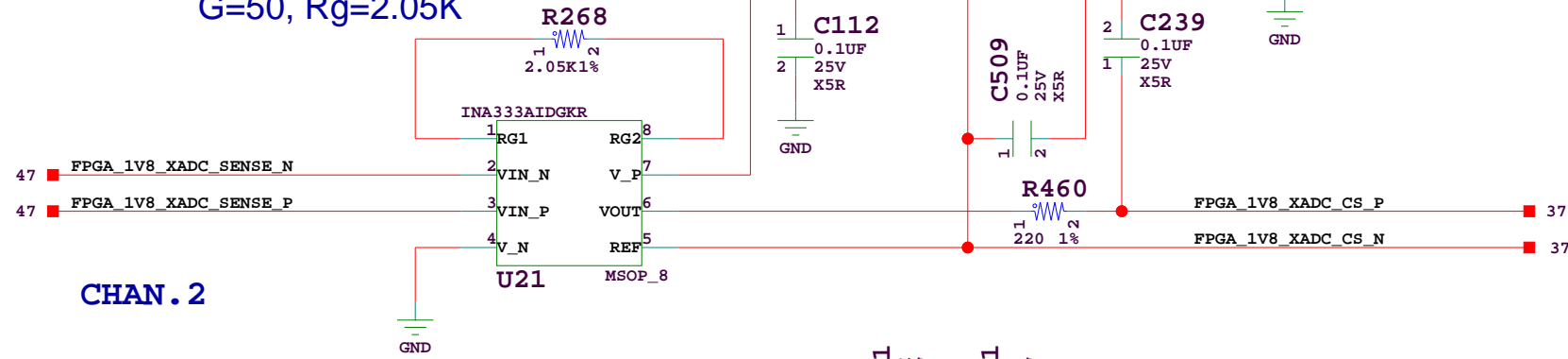
3.3V IMMEDIATE ON FIXED SUPPLY

		PCB P/N: 1280669 SCH P/N: 0381502	
Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. OP AMPS			
Date: 2-14-2014_14:52		Ver: 2.0	
Sheet Size: B		Rev: 02	
Sheet 34 of 51		Drawn By DN	

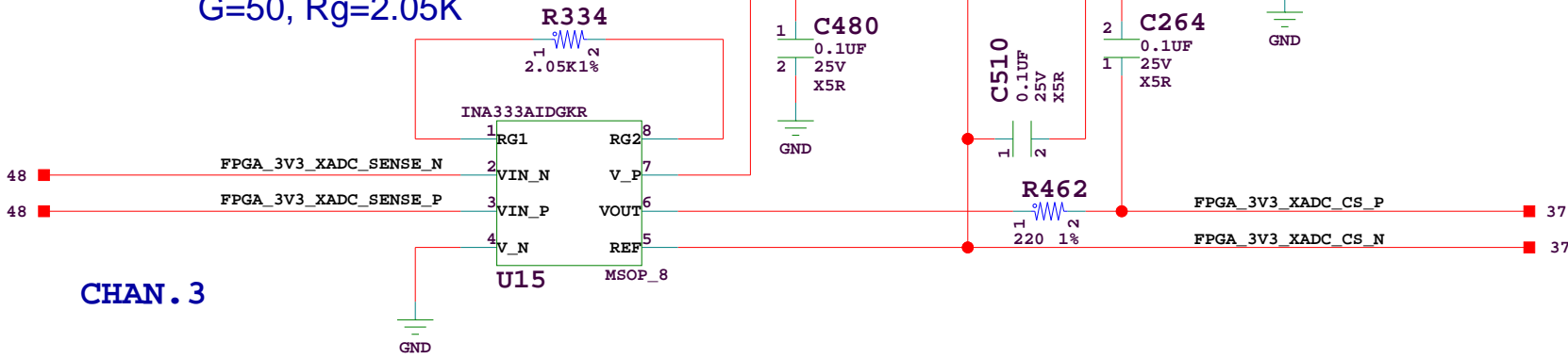
VCCO_VADJ 0A-3.2A => CS = 0V - 0.7965V
G=50, Rg=2.05K



FPGA_1V8 0A-3.0A => CS = 0V - 0.7467V
G=50, Rg=2.05K



VCC3V3 0A-3.2A => CS = 0V - 0.7965V
G=50, Rg=2.05K



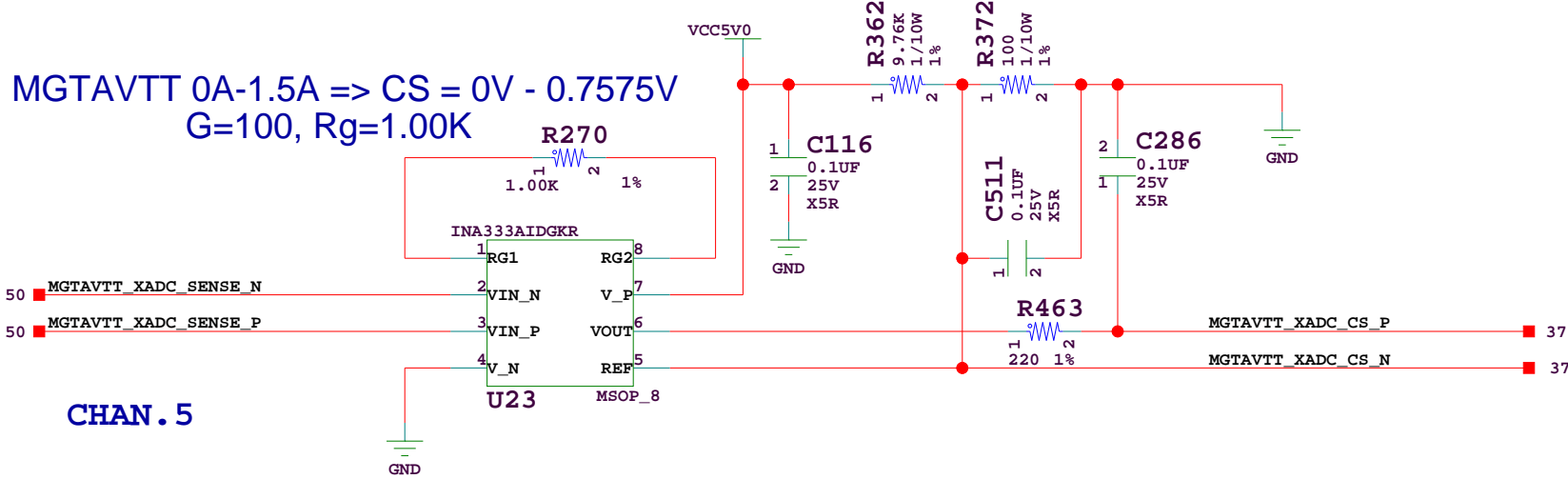
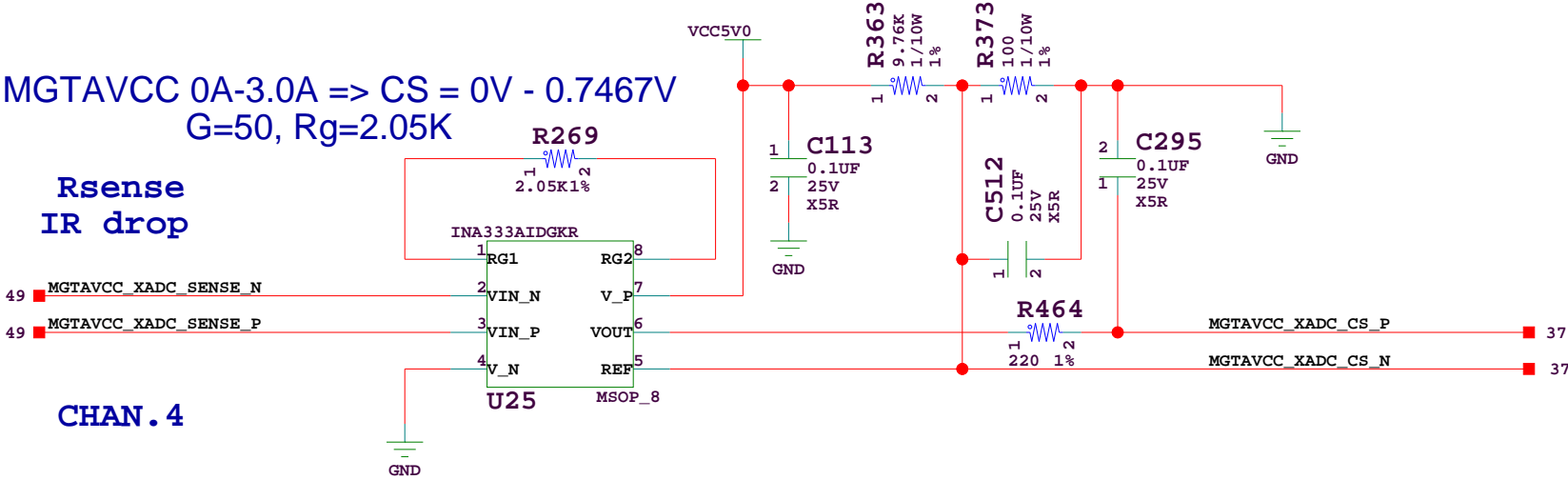
PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
XADC MON. OP AMPS

Date: 2-14-2014_14:52 Ver: 2.0

Sheet Size: B Rev: 02

Sheet 35 of 51 Drawn By DN



PCB P/N: 1280669
SCH P/N: 0381502

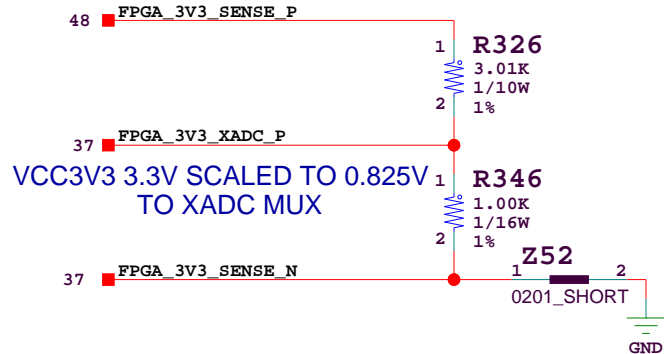
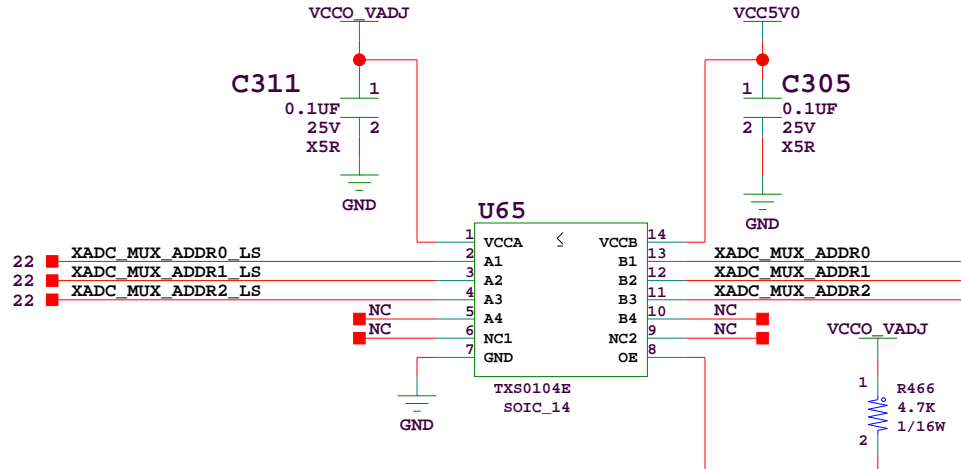
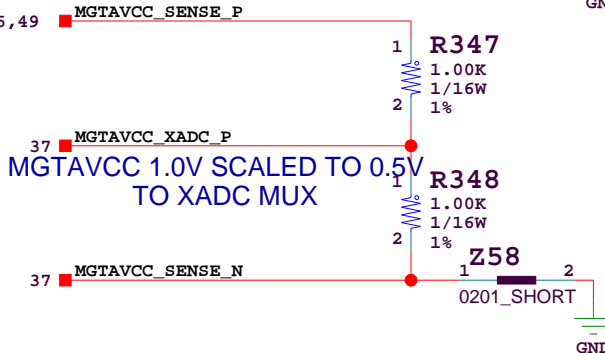
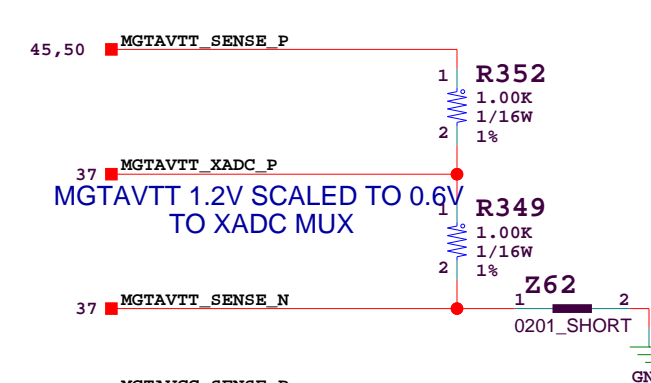
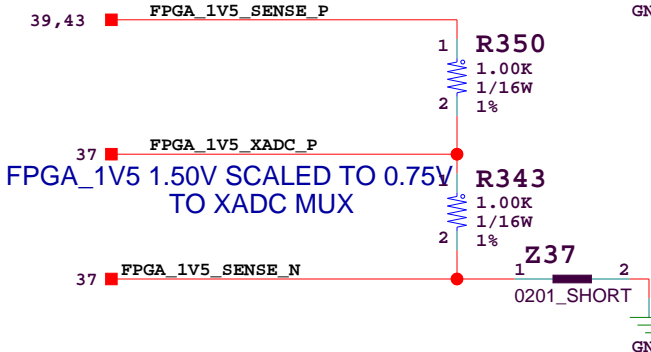
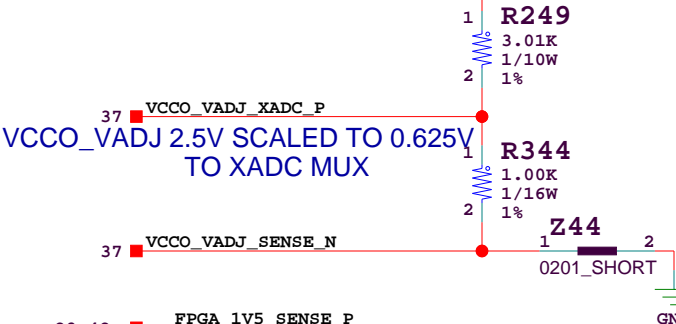
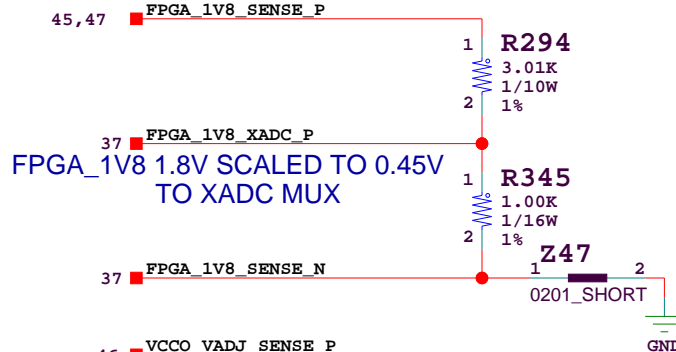
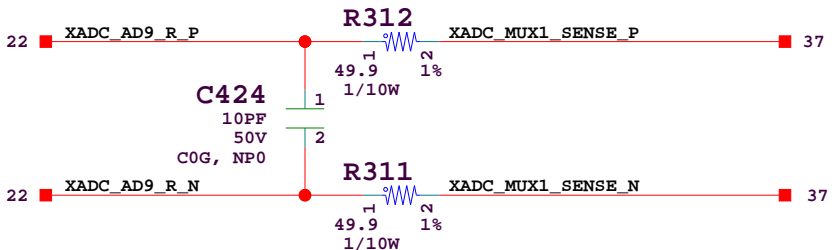
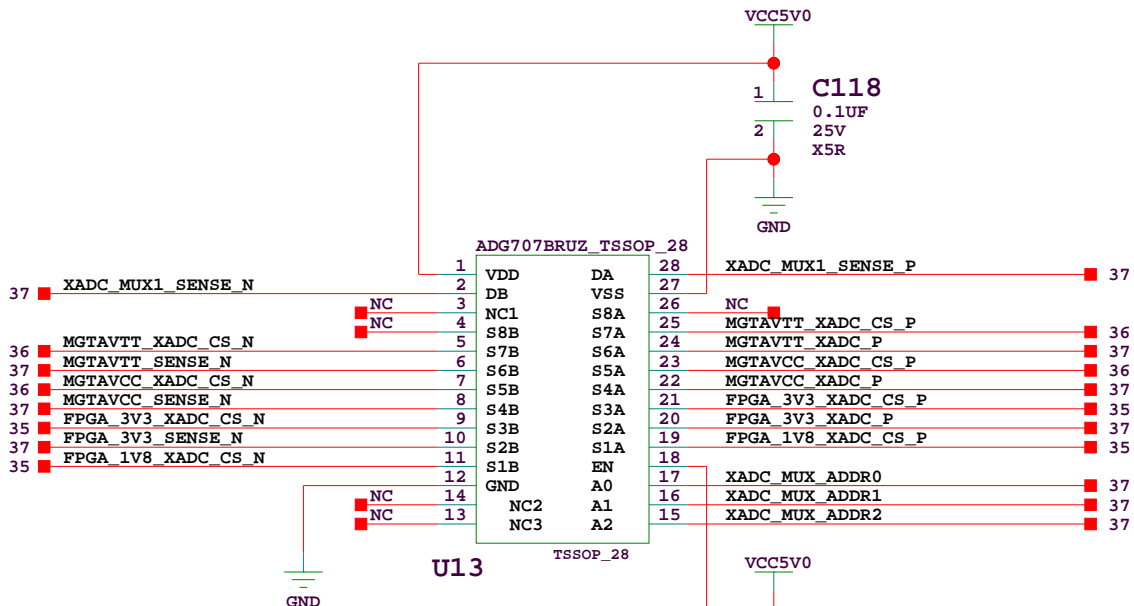
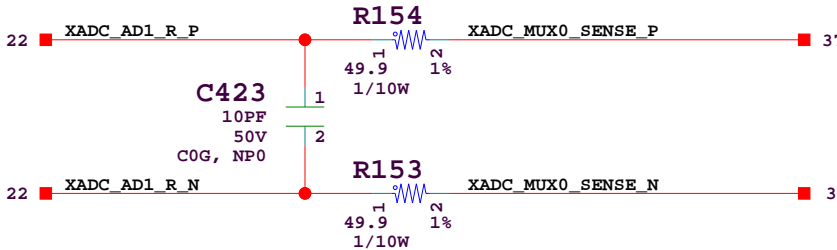
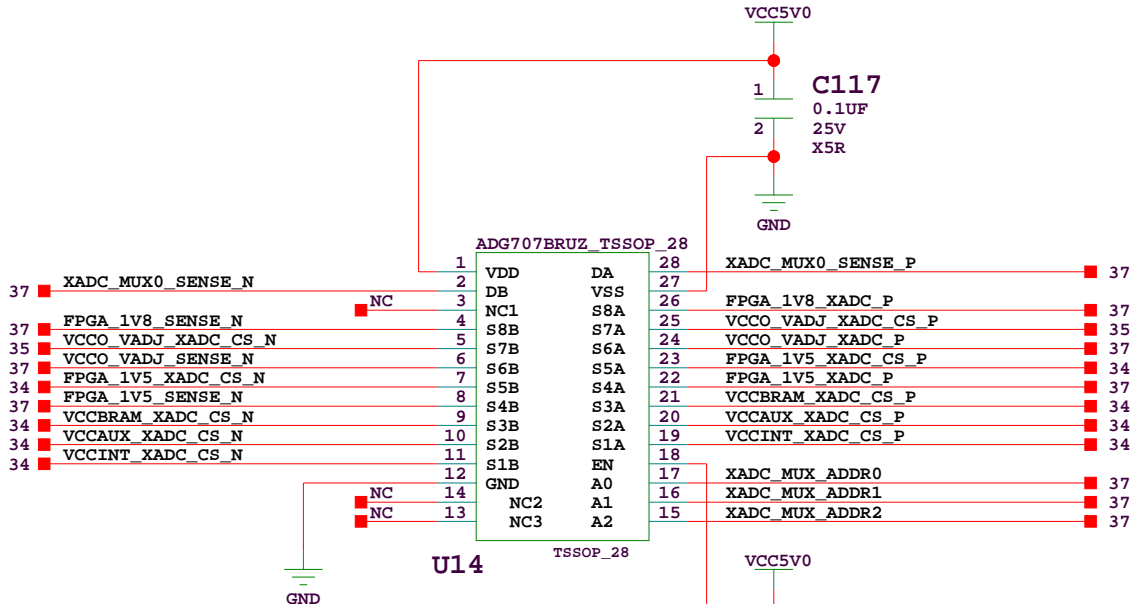
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
XADC MON. OP AMPS

Date: 2-14-2014_14:52 Ver: 2.0

Sheet Size: B Rev: 02

Sheet 36 of 51 Drawn By DN

XADC I/F MONITORING CIRCUIT PAGE 4



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
XADC MON. 2X MUX

Date: 2-14-2014_14:52

Sheet Size: B

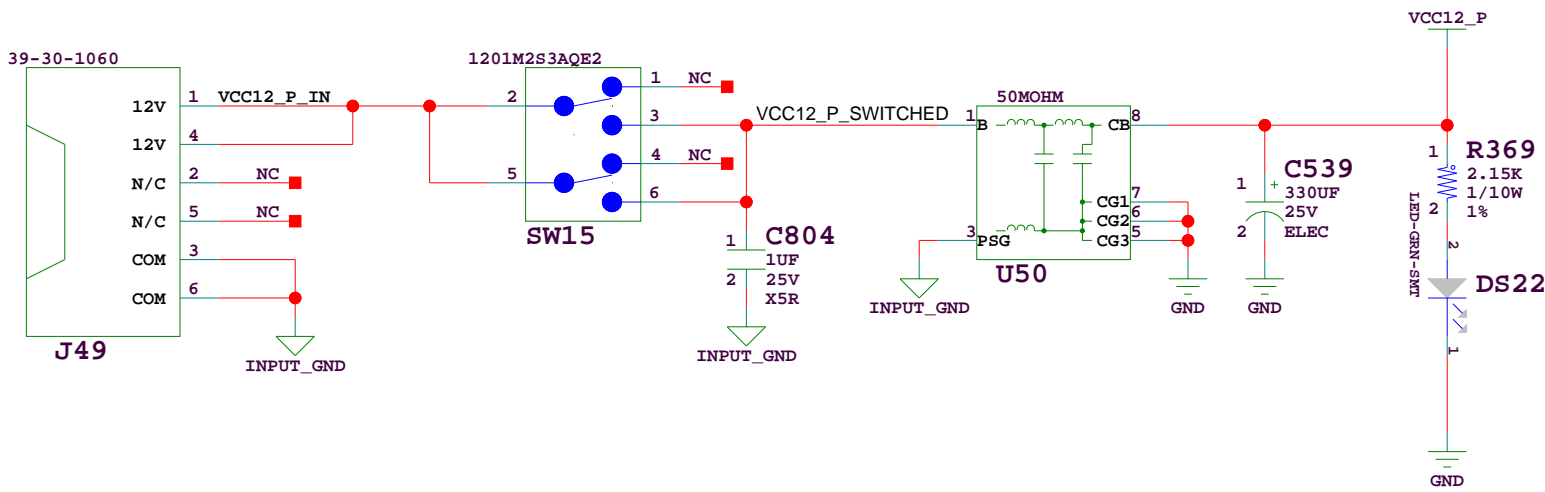
Sheet 37 of 51

Ver: 2.0

Rev: 02

Drawn By DN

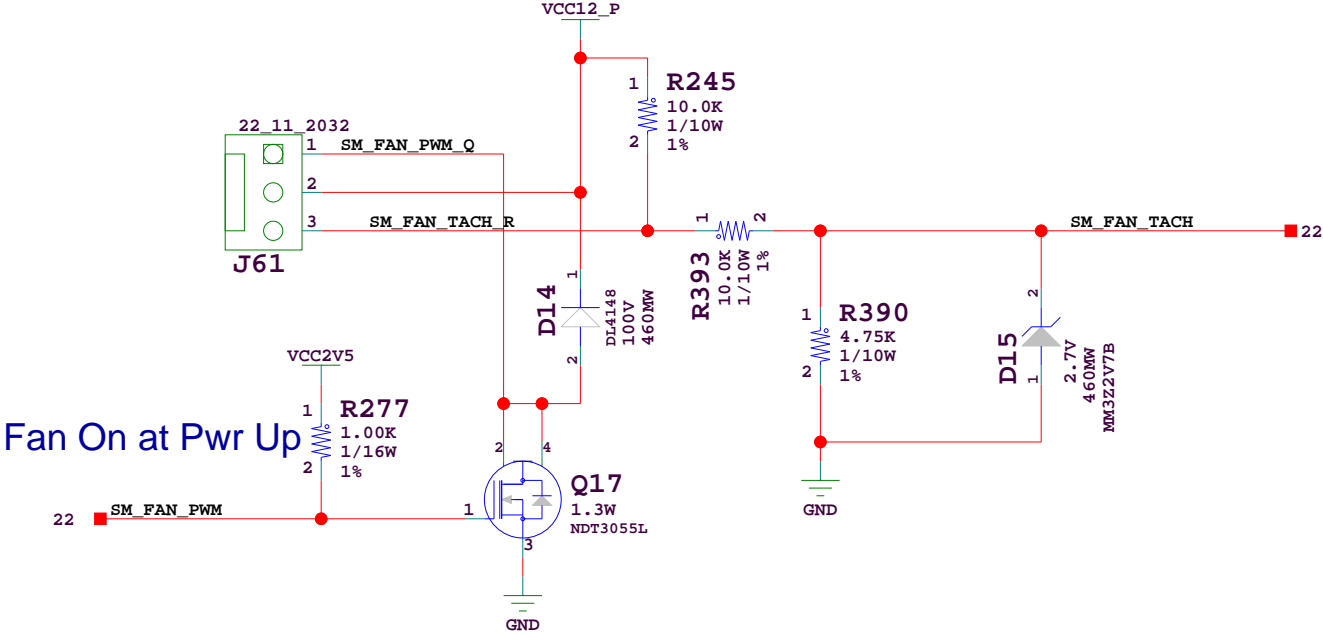
POWER SYSTEM SCHEMATIC STARTS HERE



AC701 POWER SYSTEM CONFIGURATION

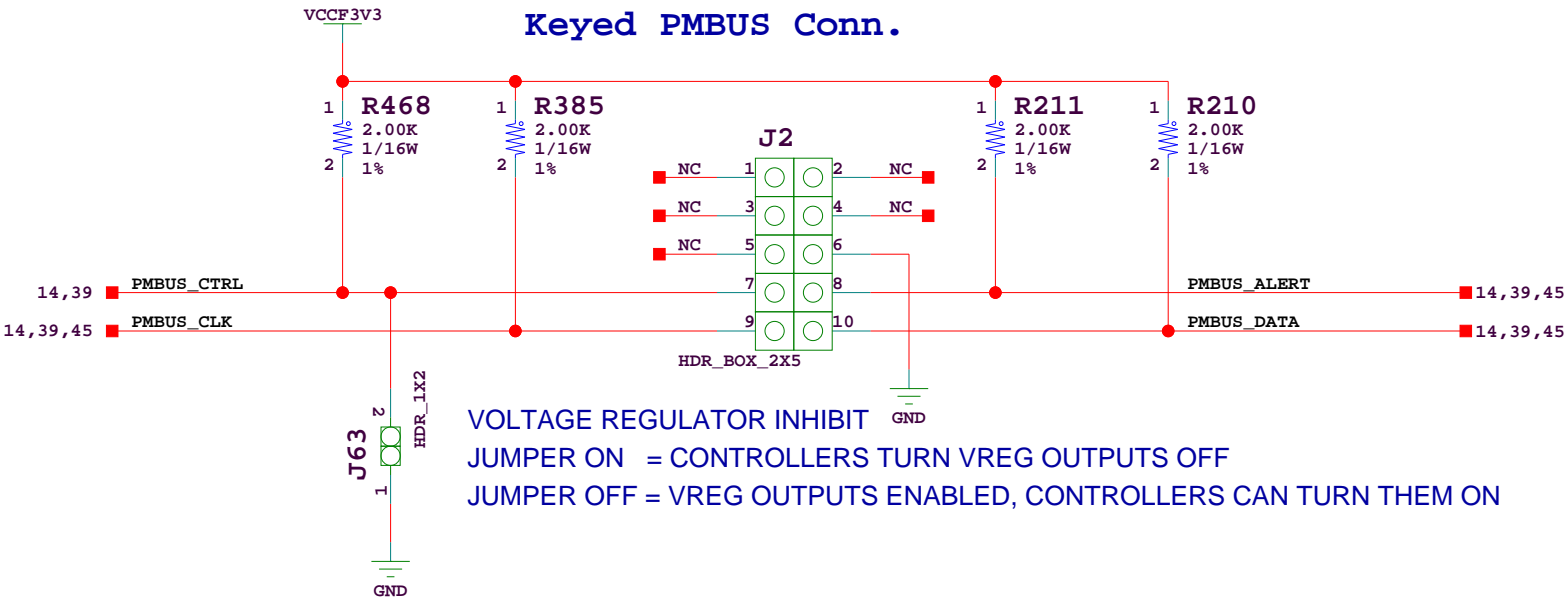
CTLR REF	PAGE	PMBUS ADDR/RAIL	NET NAME	VOLTAGE	VREG-TYPE	MAX I
#1 U8	PG 39 101	UCD90120A	4 RAILS:			
	PG 40 101	1	VCCINT	1.0V	LMZ31710 U49	10A
	PG 41 101	2	VCCAUX	1.8V	LMZ31506 U53	6A
	PG 42 101	3	VCCBRAM	1.0V	LMZ31503 U54	3A
	PG 43 101	4	FPGA_1V5	1.5V	LMZ31506 U55	6A
#2 U9	PG 45 102	UCD90120A	5 RAILS:			
	PG 46 102	1	VCCO_VADJ	2.5V	LMZ31506 U56	6A
	PG 47 102	2	FPGA_1V8	1.8V	LMZ31503 U57	3A
	PG 48 102	3	FPGA_3V3	3.3V	LMZ31506 U58	6A
	PG 49 102	4	MGTAVCC	1.0V	LMZ31503 U59	3A
	PG 49 102	5	MGTAVTT	1.2V	LMZ31503 U60	3A

Keyed Fan Header



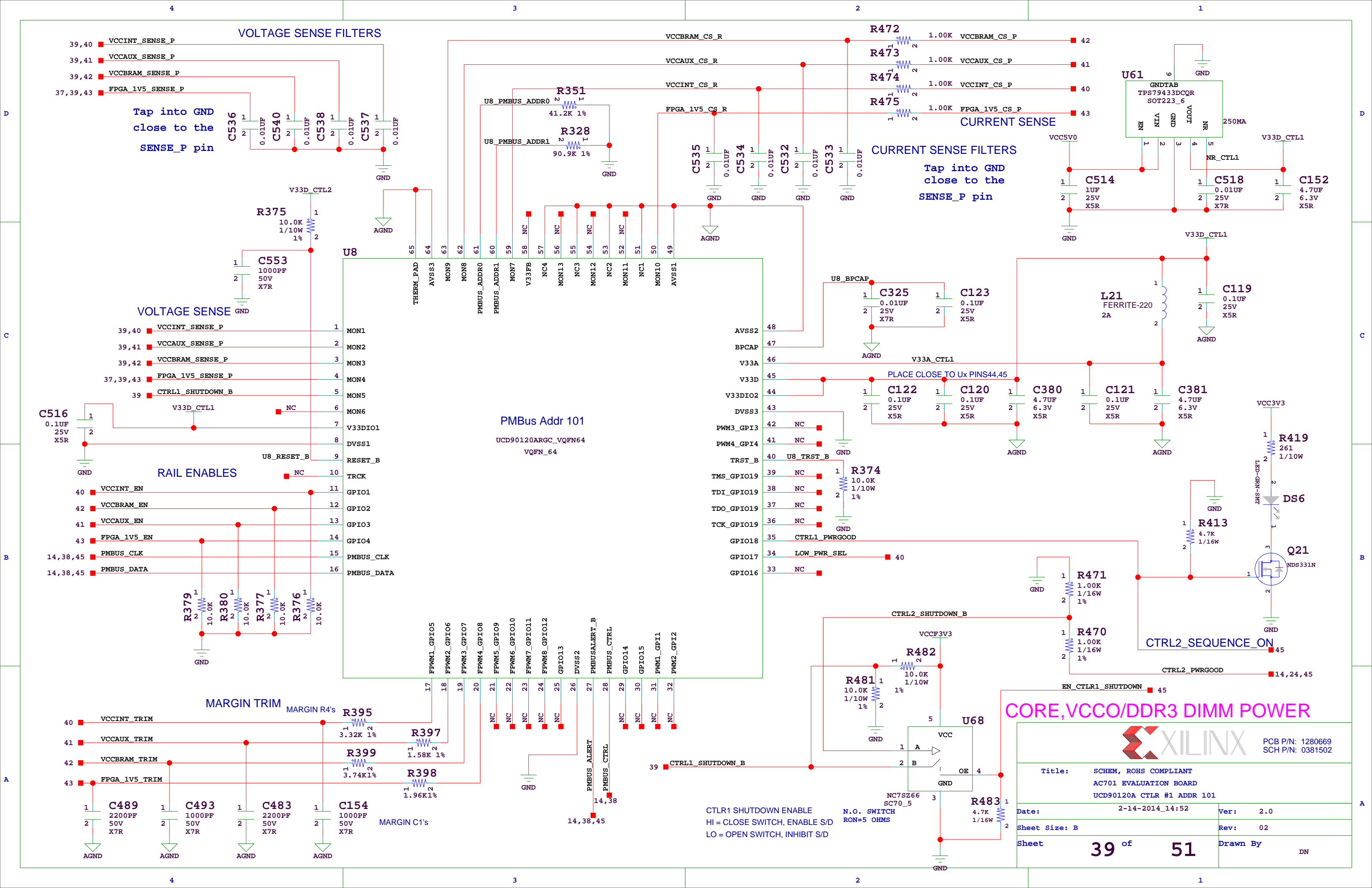
Fan On at Pwr Up

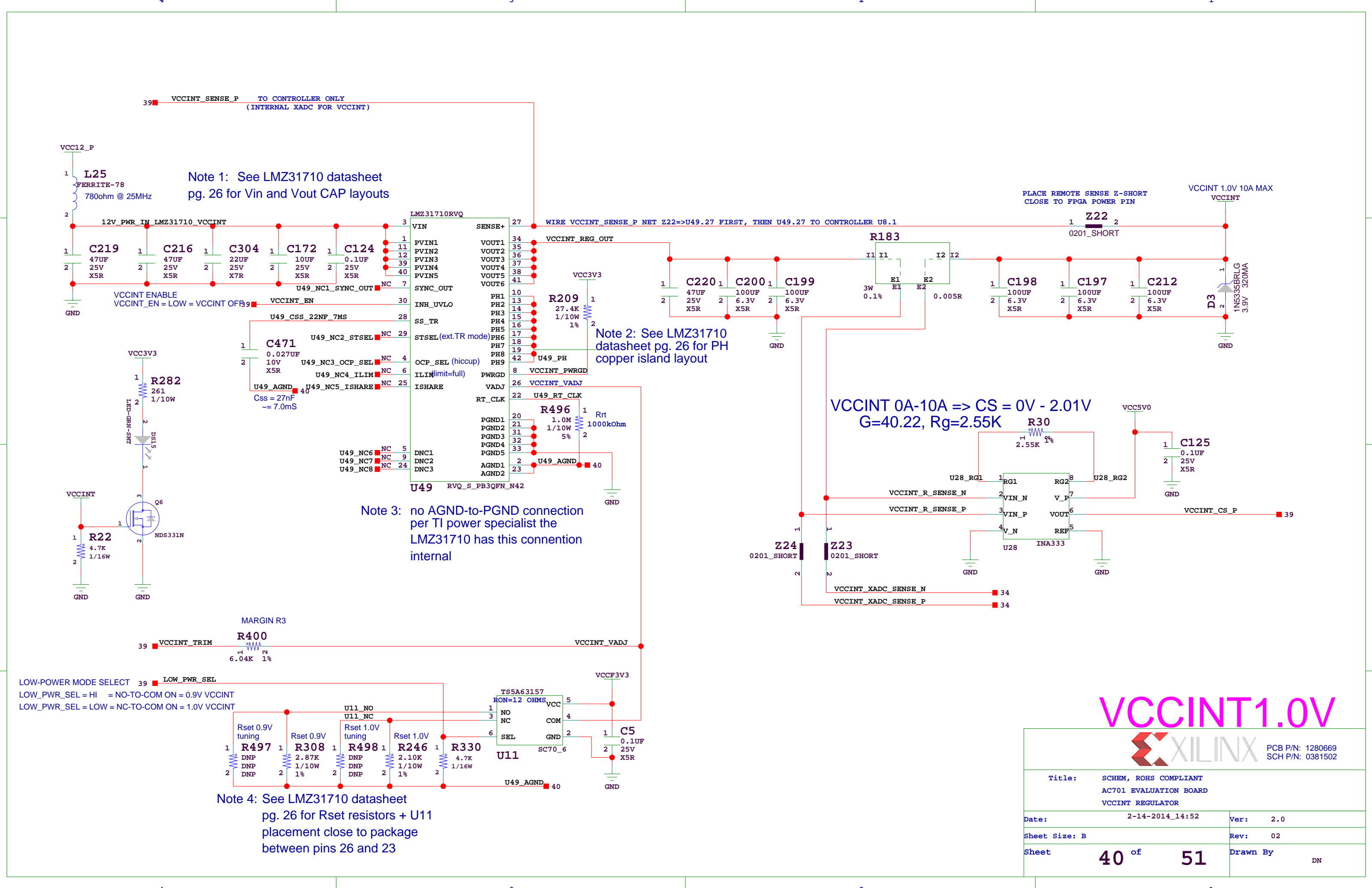
Keyed PMBUS Conn.



Power Connector and switch, PMBus Header

		PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD POWER CONN.,SWITCH,PMBUS HEADER,FAN CONTROL	
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	38 of 51	Drawn By	DN





Note 1: See LMZ31710 datasheet
pg. 26 for Vin and Vout CAP layouts

Note 2: See LMZ31710
datasheet pg. 26 for PH
copper island layout

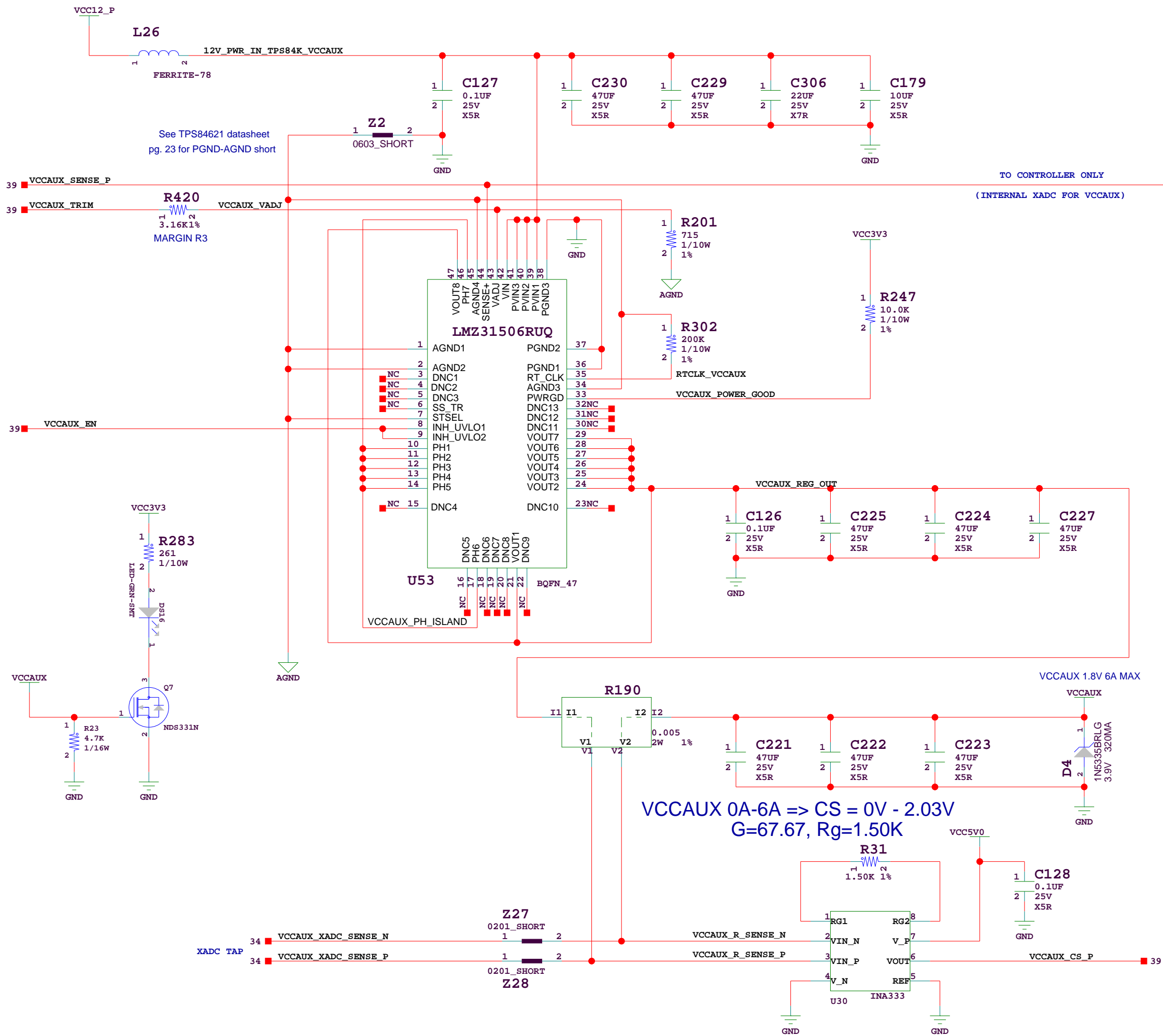
Note 3: no AGND-to-PGND connection
per TI power specialist the
LMZ31710 has this connention
internal

Note 4: See LMZ31710 datasheet
pg. 26 for Rset resistors + U11
placement close to package
between pins 26 and 23

VCCINT1.0V



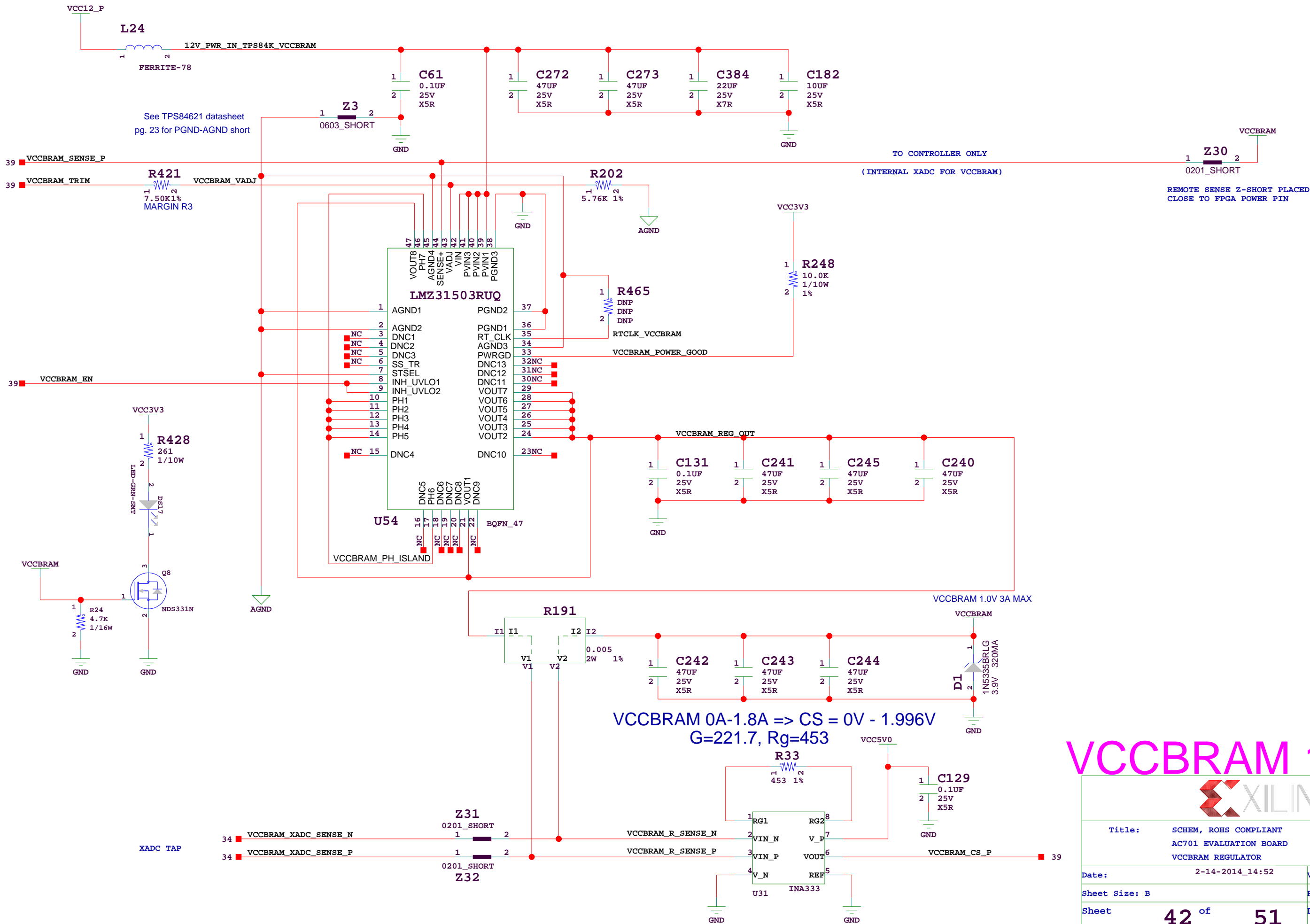
Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCINT REGULATOR			
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	40 of 51	Drawn By	DN



VCCAUX 1.8V



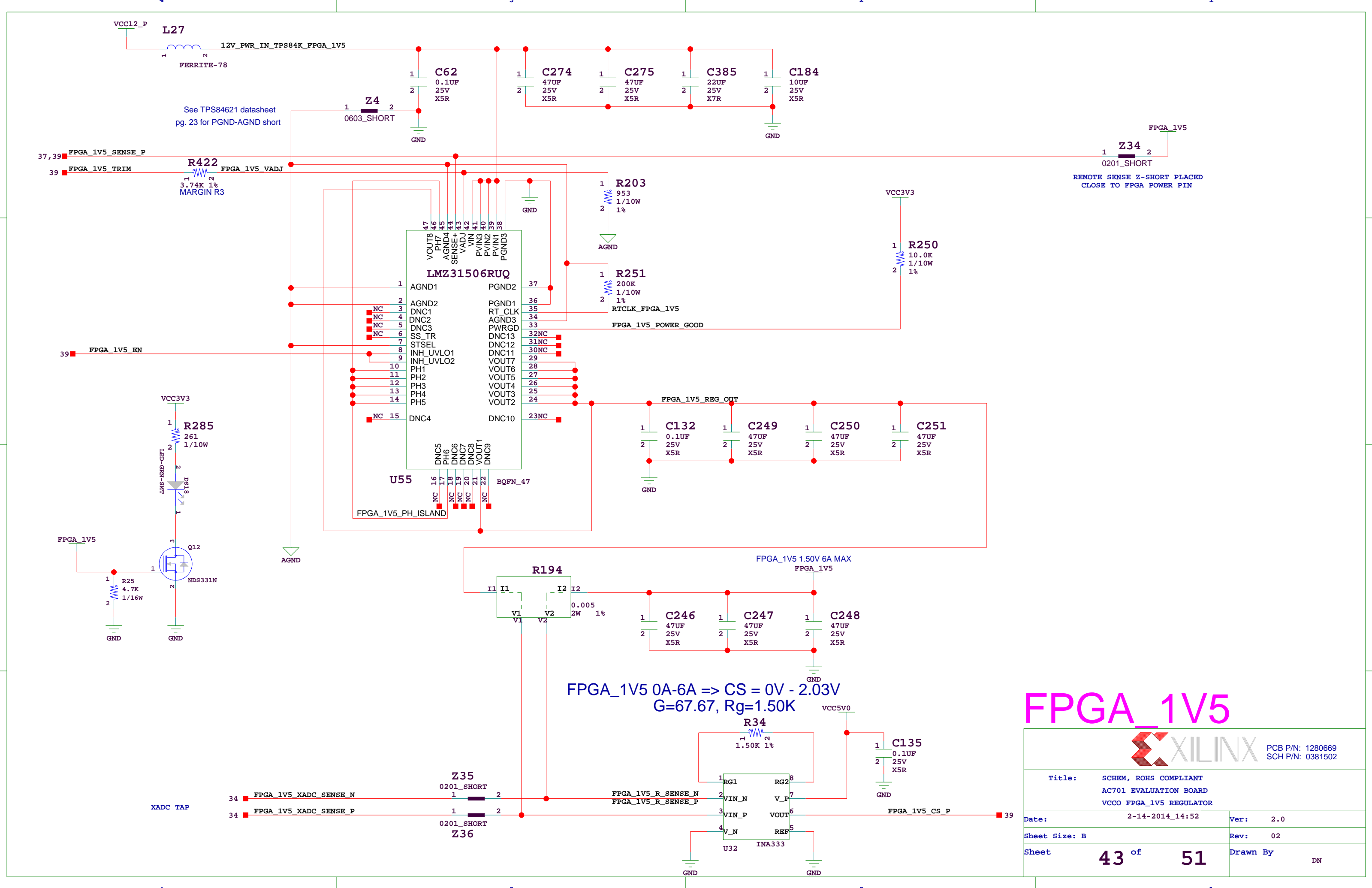
Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCAUX REGULATOR			
Date: 2-14-2014_14:52	Ver: 2.0	PCB P/N: 1280669 SCH P/N: 0381502	
Sheet Size: B	Rev: 02		
Sheet 41 of 51	Drawn By DN		



VCCBRAM 1.0V



Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCBRAM REGULATOR			
Date: 2-14-2014_14:52	Ver: 2.0	PCB P/N: 1280669 SCH P/N: 0381502	
Sheet Size: B	Rev: 02		
Sheet 42 of 51	Drawn By DN		

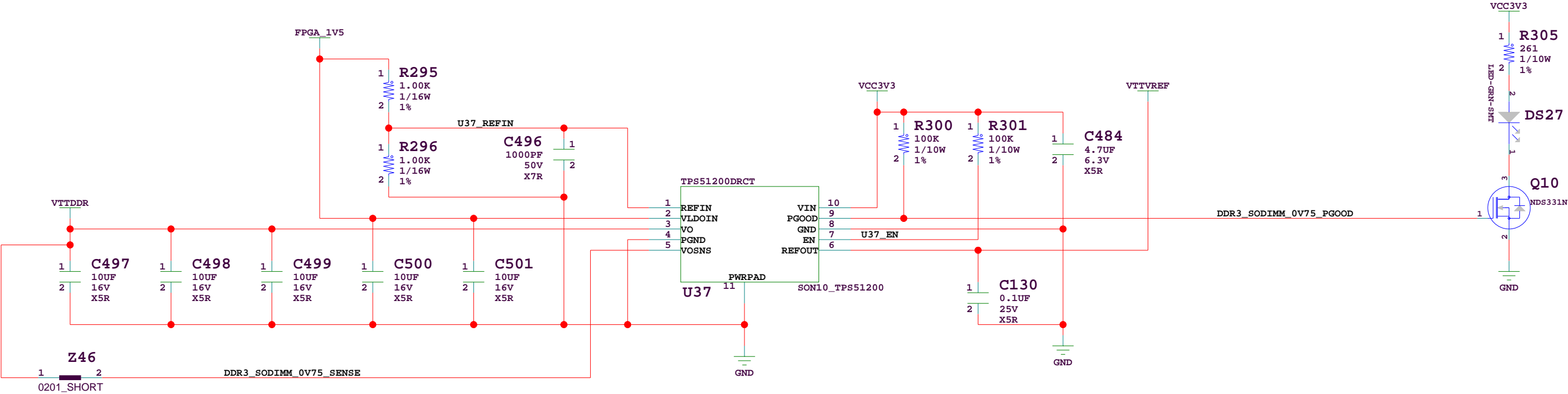


FPGA_1V5 0A-6A => CS = 0V - 2.03V
G=67.67, Rg=1.50K

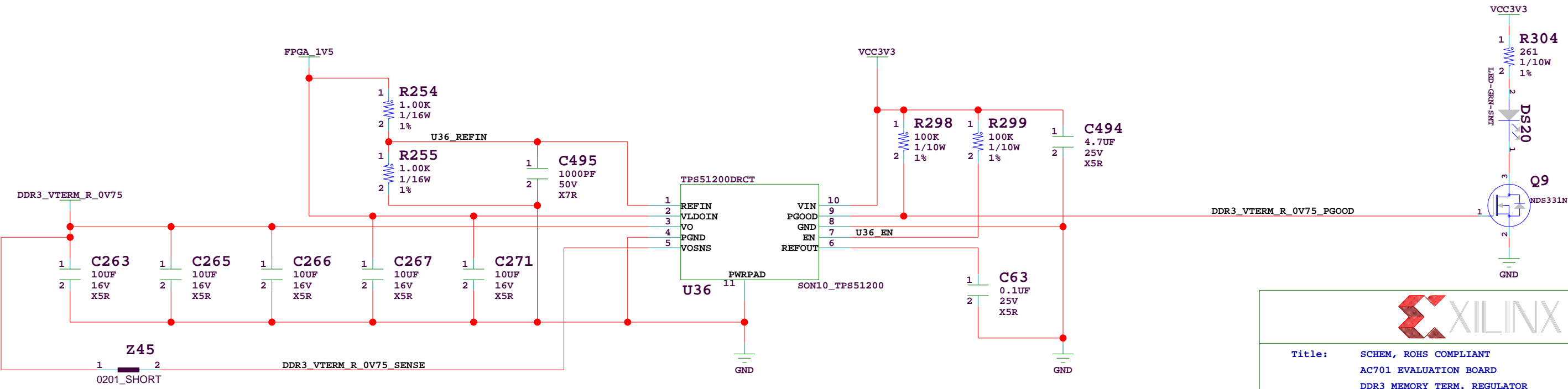
FPGA_1V5

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCO FPGA_1V5 REGULATOR	
Date: 2-14-2014_14:52	Ver: 2.0
Sheet Size: B	Rev: 02
Sheet 43 of 51	Drawn By DN

DDR3 SODIMM TERM. REGULATOR, 0.75v @ 3A



DDR3 SODIMM MEM. TERM. RESISTOR REGULATOR, 0.75v @ 3A



PCB P/N: 1280669
SCH P/N: 0381502

Title:

SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
DDR3 MEMORY TERM. REGULATOR

Date:

2-14-2014_14:52

Ver:

2.0

Sheet Size:

B

Rev:

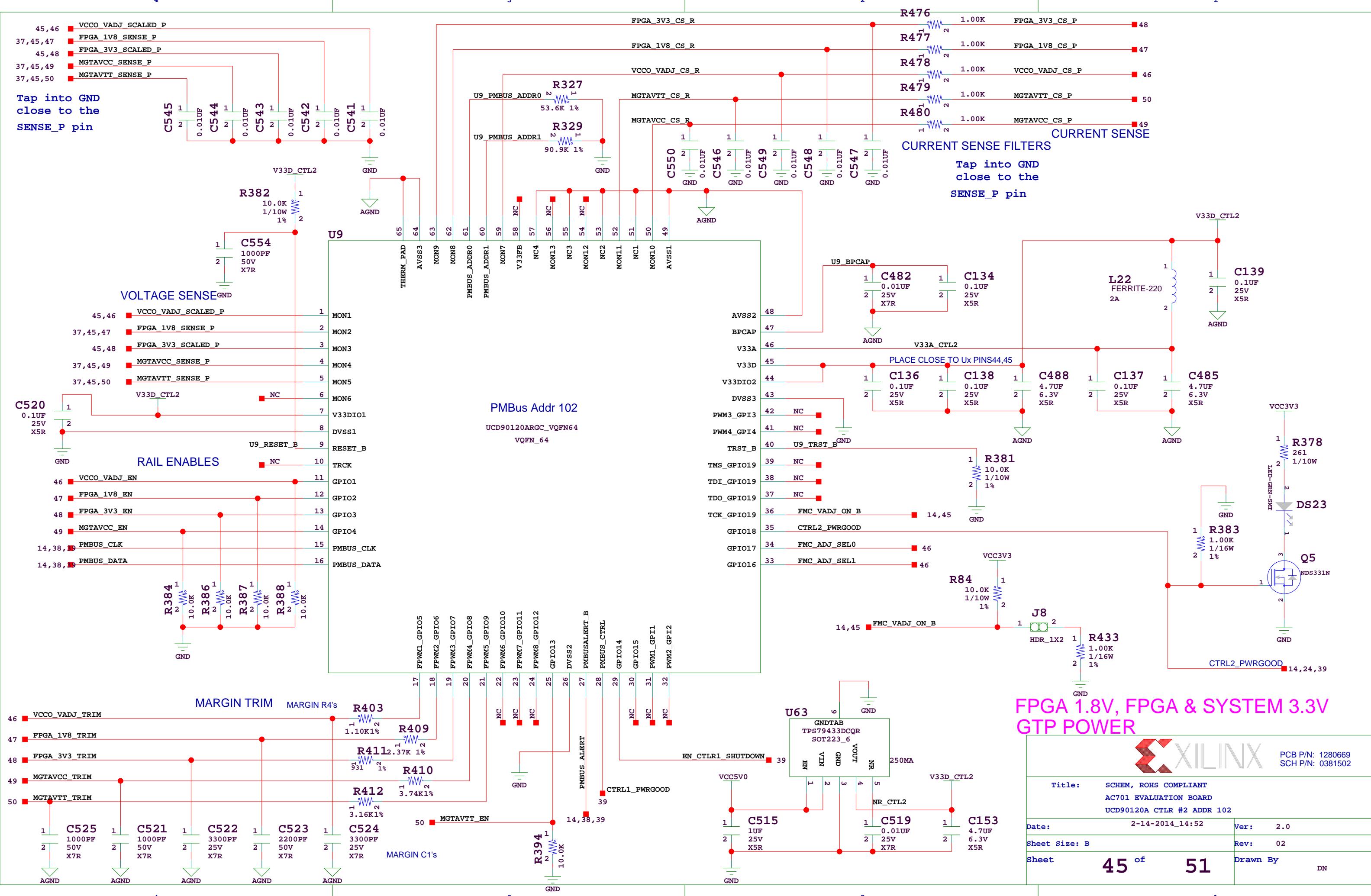
02

Sheet

44 of 51

Drawn By

DN



Tap into GND close to the SENSE_P pin

VOLTAGE SENSE

RAIL ENABLES

MARGIN TRIM

CURRENT SENSE FILTERS

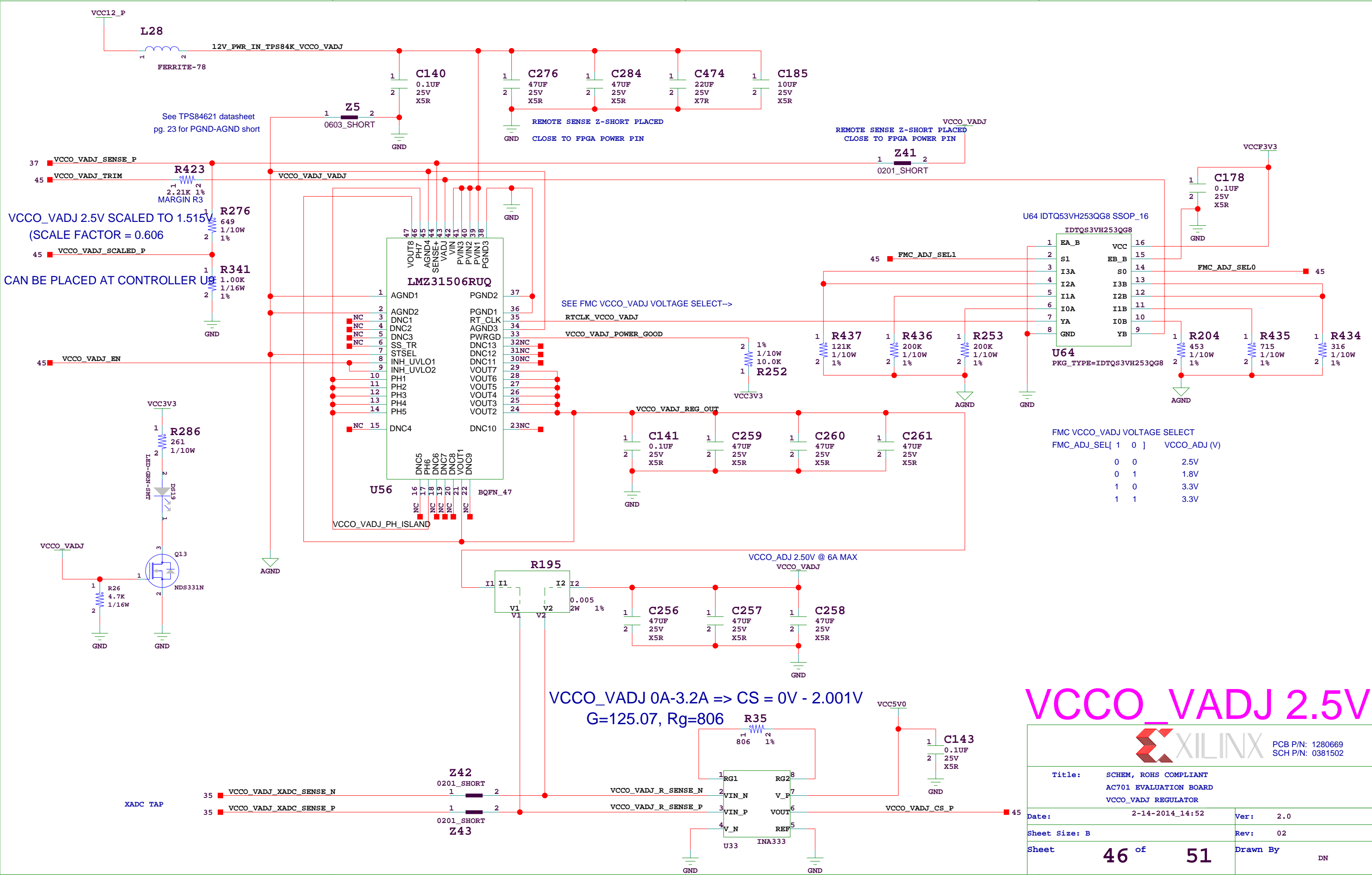
Tap into GND close to the SENSE_P pin

CURRENT SENSE

FPGA 1.8V, FPGA & SYSTEM 3.3V GTP POWER

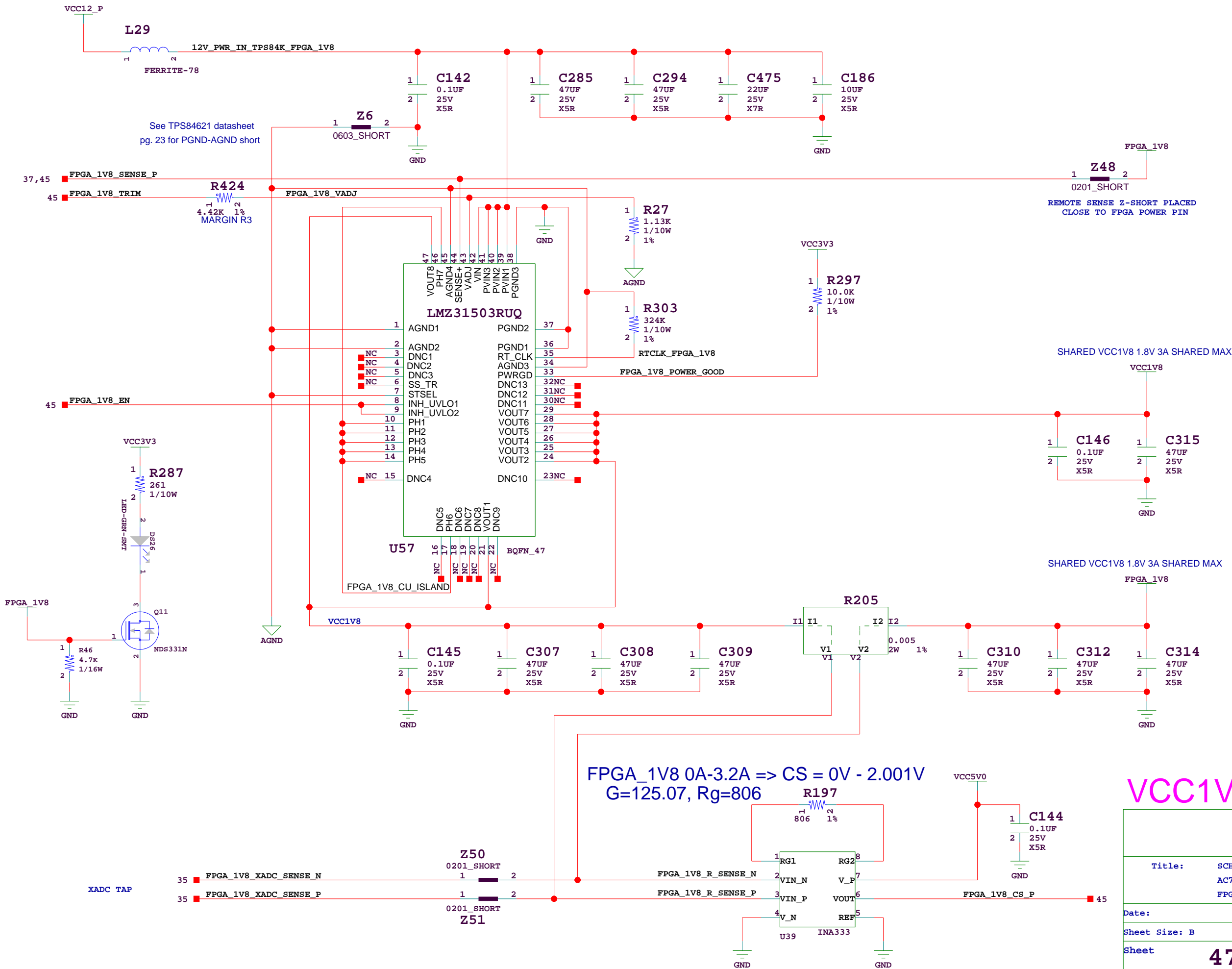


PCB P/N: 1280669 SCH P/N: 0381502	
Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD UCD90120A CTRLR #2 ADDR 102	
Date: 2-14-2014_14:52	Ver: 2.0
Sheet Size: B	Rev: 02
Sheet 45 of 51	Drawn By DN



VCCO_VADJ 2.5V

		PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCO_VADJ REGULATOR	
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	46 of 51	Drawn By	DN

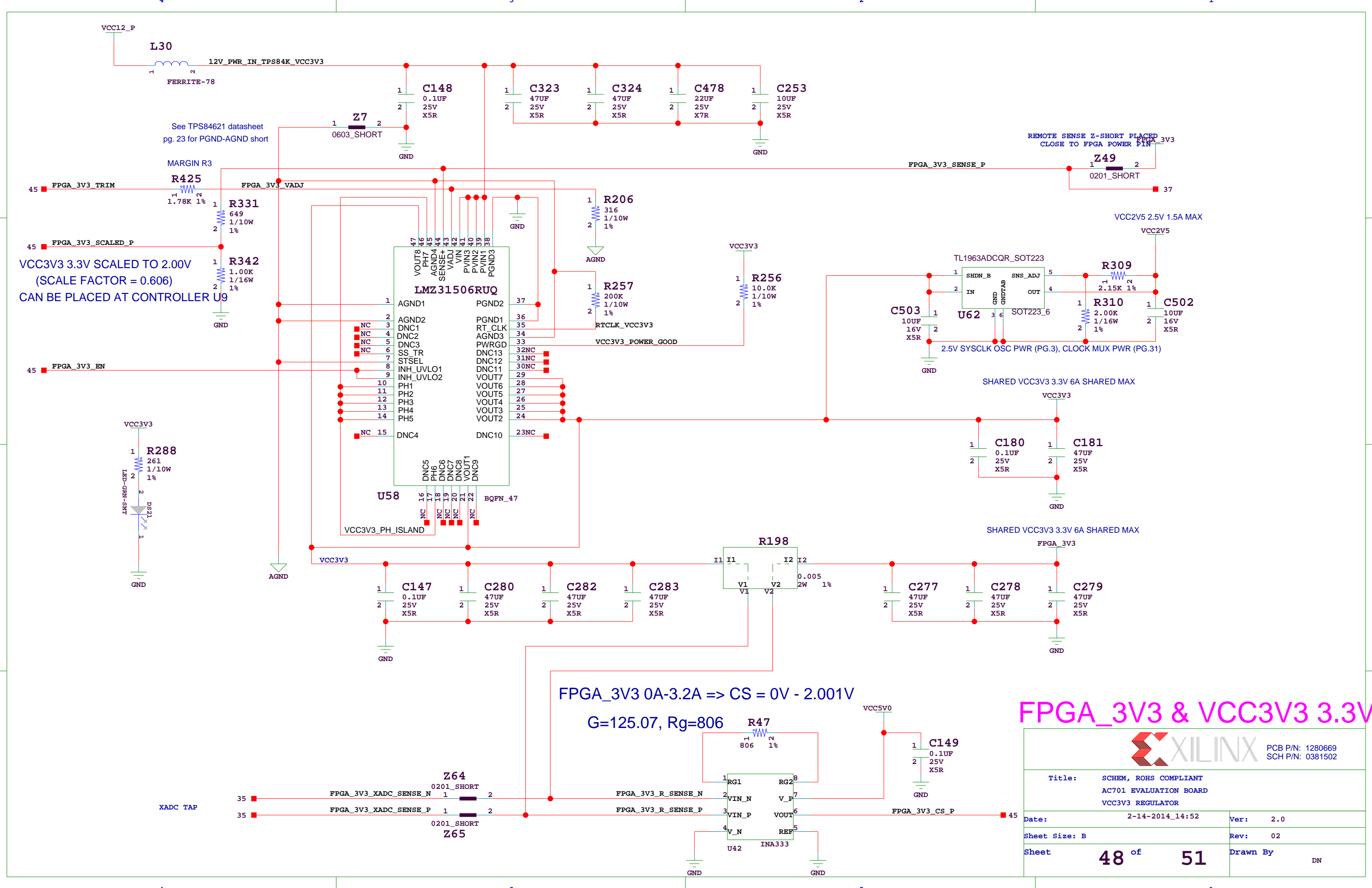


VCC1V8 & FPGA_1V8



PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FPGA_1V8 REGULATOR			
Date: 2-14-2014_14:52	Ver: 2.0		
Sheet Size: B	Rev: 02		
Sheet 47 of 51	Drawn By DN		

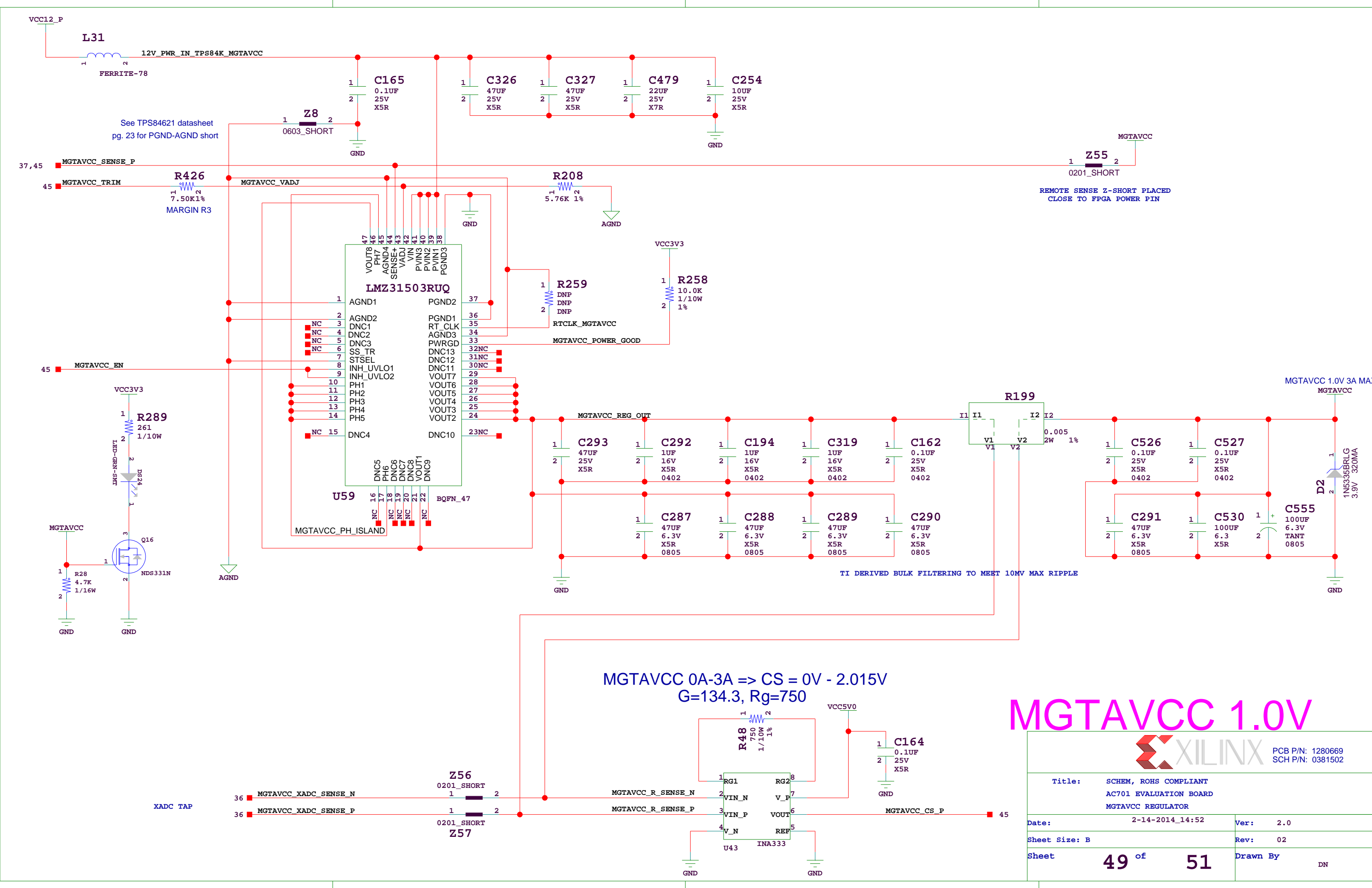


VCC3V3 3.3V SCALED TO 2.00V
(SCALE FACTOR = 0.606)
CAN BE PLACED AT CONTROLLER U9

FPGA_3V3 0A-3.2A => CS = 0V - 2.001V
G=125.07, Rg=806

FPGA_3V3 & VCC3V3 3.3V

		PCB P/N: 1280669 SCH P/N: 0381502	
Title:		SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCC3V3 REGULATOR	
Date:	2-14-2014_14:52	Ver:	2.0
Sheet Size:	B	Rev:	02
Sheet	48 of 51	Drawn By	DN



MGTAVCC 0A-3A => CS = 0V - 2.015V
G=134.3, Rg=750

MGTAVCC 1.0V



Title: SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD MGTAVCC REGULATOR			
Date: 2-14-2014_14:52	Ver: 2.0		
Sheet Size: B	Rev: 02		
Sheet 49 of 51	Drawn By DN		

