

This chapter describes the electrical characteristics, switching characteristics, and configuration specifications for Arria® V devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, and core and periphery performance. Configuration specifications include power-on reset (POR) specification, initialization clock source option and timing, various configuration mode timing parameters, remote system upgrades timing, and user watchdog internal oscillator frequency specification. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

 For more information about the densities and packages of devices in the Arria V family, refer to the *Overview for Arria V Device Family* chapter.

Electrical Characteristics

The following sections describe the electrical characteristics of Arria V devices.

Operating Conditions

When you use Arria V devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this chapter.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in -4 (fastest), -5, and -6 speed grades. Industrial grade devices are offered in the -5 speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in [Table 2-1](#) may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2-1. Absolute Maximum Ratings for Arria V Devices—Preliminary

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage and periphery circuitry power supply	-0.5	1.35	V
V _{CCPGM}	Configuration pins power supply	-0.5	3.75	V
V _{CCAUX}	Auxiliary supply	-0.5	3.75	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.75	V
V _{CCIO}	I/O power supply	-0.5	3.9	V
V _{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	-0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	-0.5	3.75	V
V _{CCA_GXB}	Transceiver high voltage power	-0.5	3.75	V
V _{CCH_GXB}	Transmitter output buffer power	-0.5	1.8	V
V _{CCR_GXB}	Receiver power	-0.5	1.21	V
V _{CCT_GXB}	Transmitter power	-0.5	1.21	V
V _{CCL_GXB}	Clock network power	-0.5	1.21	V
V _I	DC input voltage	-0.5	4	V
I _{OUT}	DC output current per pin	-25	40	mA
T _J	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (No bias)	-65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in Table 2–2 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 2–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 3.95 V can only be at 3.95 V for ~5% over the lifetime of the device; for a device lifetime of 10 years, this amounts to half a year.

Table 2–2. Maximum Allowed Overshoot During Transitions for Arria V Devices—Preliminary

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.7	100	%
		3.75	59.79	%
		3.8	33.08	%
		3.85	18.45	%
		3.9	10.36	%
		3.95	5.87	%
		4	3.34	%
		4.05	1.92	%
		4.1	1.11	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices. Table 2–3 lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 2–3. Recommended Operating Conditions for Arria V Devices—Preliminary (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V _{CC}	Core voltage and periphery circuitry power supply	—	1.07	1.1	1.13	V
V _{CCAUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V _{CCPD} ⁽¹⁾	I/O pre-driver (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V

Table 2-3. Recommended Operating Conditions for Arria V Devices—Preliminary (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O buffers (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.418	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.3 V) power supply	—	3.135	3.3	3.465	V
	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.425	1.5	1.575	V
V_{CCBAT} ⁽²⁾	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_I	DC input voltage	—	-0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	-40	—	100	°C
t_{RAMP} ⁽³⁾	Power supply ramp time	Slow POR (PORSEL=0)	200 μ s	—	100 ms	—
		Fast POR (PORSEL=1)	200 μ s	—	4 ms	—

Notes to Table 2-3:

- V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.
- If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V or 3.0-V power supply. Arria V POR circuitry monitors V_{CCBAT} . Arria V devices do not exit POR if V_{CCBAT} stays low.
- When power is applied to an Arria V device, a POR occurs if the power supply reaches the recommended operating range in the maximum power supply ramp.

Table 2-4 lists the transceiver power supply recommended operating conditions for Arria V devices.

Table 2-4. Transceiver Power Supply Operating Conditions for Arria V GX and GT Devices—Preliminary (Part 1 of 2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_GXBL}	Transceiver high voltage power (left side)	2.375	2.5	2.625	V
V_{CCA_GXBR}	Transceiver high voltage power (right side)				
V_{CCR_GXBL}	Receiver power (left side)	1.07	1.1	1.13	V
V_{CCR_GXBR}	Receiver power (right side)				
V_{CCT_GXBL}	Transmitter power (left side)	1.07	1.1	1.13	V
V_{CCT_GXBR}	Transmitter power (right side)				

Table 2-4. Transceiver Power Supply Operating Conditions for Arria V GX and GT Devices—Preliminary (Part 2 of 2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V _{CCH_GXBL}	Transmitter output buffer power (left side)	1.425	1.5	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power (right side)				
V _{CCL_GXBL}	Clock network power (left side)	1.07	1.1	1.13	V
V _{CCL_GXBR}	Clock network power (right side)	1.07	1.1	1.13	V

Table 2-5 lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) FPGA with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus.

Table 2-5. HPS Power Supply Operating Conditions for Arria V Sx and ST Devices—Preliminary


Symbol	Description	Minimum	Typical	Maximum	Unit
V _{CC_HPS}	HPS Core voltage and periphery circuitry power supply	1.07	1.1	1.13	V
V _{CCPD_HPS}	HPS I/O pre-driver (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O pre-driver (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O pre-driver (2.5 V) power supply	2.375	2.5	2.625	V
V _{CCIO_HPS}	HPS I/O buffers (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O buffers (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O buffers (2.5 V) power supply	2.375	2.5	2.625	V
	HPS I/O buffers (1.8 V) power supply	1.71	1.8	1.89	V
	HPS I/O buffers (1.5 V) power supply	1.425	1.5	1.575	V
	HPS I/O buffers (1.2 V) power supply	1.14	1.2	1.26	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins (3.3 V) power supply	3.135	3.3	3.465	V
	HPS reset and clock input pins (3.0 V) power supply	2.85	3.0	3.15	V
	HPS reset and clock input pins (2.5 V) power supply	2.375	2.5	2.625	V
	HPS reset and clock input pins (1.8 V) power supply	1.71	1.8	1.89	V
V _{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	2.375	2.5	2.625	V

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to estimate supply current for your design because these currents vary greatly with the resources you use.

 For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 2-6 lists the Arria V I/O pin leakage current specifications.

Table 2-6. I/O Pin Leakage Current for Arria V Devices—Preliminary

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0\text{ V to }V_{CCIO\text{MAX}}$	-30	—	30	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIO\text{MAX}}$	-30	—	30	μA

Bus Hold Specifications

Table 2-7 lists the Arria V device bus hold specifications.

Table 2-7. Bus Hold Parameters for Arria V Devices—Preliminary⁽¹⁾

Parameter	Symbol	Conditions	$V_{CCIO}\text{ (V)}$												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max.)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min.)	-8	—	-12	—	-30	—	-50	—	-70	—	-70	—	μA
Bus-hold, low, overdrive current	I_{ODL}	$0\text{V} < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus-hold, high, overdrive current	I_{ODH}	$0\text{V} < V_{IN} < V_{CCIO}$	—	-125	—	-175	—	-200	—	-300	—	-500	—	-500	μA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 2-7:

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

(OCT) Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block. Table 2-8 lists the Arria V OCT termination calibration accuracy specifications.

Table 2-8. OCT Calibration Accuracy Specifications for Arria V Devices—Preliminary⁽¹⁾

Symbol	Description	Conditions (V)	Calibration Accuracy			Unit
			C4	C5, I5	C6	
25-Ω R _S	Internal series termination with calibration (25-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R _S	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R _S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R _S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V _{CCIO} = 1.2	±15	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25	-10 to +40	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCIO} = 1.2	-10 to +40	-10 to +40	-10 to +40	%
25-Ω R _{S_left_shift}	Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

Note to Table 2-8:

(1) OCT calibration accuracy is valid at the time of calibration only.

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 2-9 lists the Arria V OCT without calibration resistance tolerance to PVT changes.

Table 2-9. OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices—Preliminary

Symbol	Description	Conditions (V)	Resistance Tolerance			Unit
			C4	C5, I5	C6	
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 3.0 and 2.5	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.8 and 1.5	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.2	±35	±50	±50	%
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 3.0 and 2.5	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 1.8 and 1.5	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 1.2	±35	±50	±50	%
100-Ω R _D	Internal differential termination (100-Ω setting)	V _{CCIO} = 2.5	±25	TBD	TBD	%

OCT calibration is automatically performed at power up for OCT-enabled I/Os. Table 2-10 lists OCT variation with temperature and voltage after power-up calibration. Use Table 2-10 to determine the OCT variation after power-up calibration and Equation 2-1 to determine the OCT variation without recalibration.

Equation 2-1. OCT Variation Without Recalibration—Preliminary^{(1), (2), (3), (4), (5), (6)}

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

Notes to Equation 2-1:

- (1) The R_{OCT} value calculated from Equation 2-1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- (2) R_{SCAL} is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power up.
- (4) ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- (5) dR/dT is the percentage change of R_{SCAL} with temperature.
- (6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2-10 lists the OCT variation after the power-up calibration.

Table 2-10. OCT Variation after Power-Up Calibration for Arria V Devices—Preliminary (1)

Symbol	Description	V _{CCIO} (V)	Value	Unit
dR/dV	OCT variation of voltage without recalibration	3.0	0.0297	% / mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation of temperature without recalibration	3.0	0.189	% / °C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Note to Table 2-10:

(1) Valid for a V_{CCIO} range of ±5% and temperature range of 0° to 85°C.

Pin Capacitance

Table 2-11 lists the Arria V pin capacitance.

Table 2-11. Pin Capacitance for Arria V Devices

Symbol	Description	Value	Unit
C _{IOTB}	Input capacitance on top/bottom I/O pins	5.5	pF
C _{IOLR}	Input capacitance on left/right I/O pins	5.5	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	5.5	pF

Hot Socketing

Table 2-12 lists the hot socketing specifications for Arria V devices.

Table 2-12. Hot Socketing Specifications for Arria V Devices—Preliminary

Symbol	Description	Maximum
I _{IOPIN (DC)}	DC current per I/O pin	300 μA
I _{IOPIN (AC)}	AC current per I/O pin	8 mA (1)
I _{XCVR-TX (DC)}	DC current per transceiver transmitter (TX) pin	100 mA
I _{XCVR-RX (DC)}	DC current per transceiver receiver (RX) pin	50 mA

Note to Table 2-12:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |I_{IOPIN}| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 2-13 lists the weak pull-up resistor values for Arria V devices.

Table 2-13. Internal Weak Pull-Up Resistor Values for Arria V Devices—Preliminary (1), (2)

Symbol	Description	Conditions (V) (3)	Value (4)	Unit
R _{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V _{CCIO} = 3.3 ±5%	25	kΩ
		V _{CCIO} = 3.0 ±5%	25	kΩ
		V _{CCIO} = 2.5 ±5%	25	kΩ
		V _{CCIO} = 1.8 ±5%	25	kΩ
		V _{CCIO} = 1.5 ±5%	25	kΩ
		V _{CCIO} = 1.35 ±5%	25	kΩ
		V _{CCIO} = 1.25 ±5%	25	kΩ
		V _{CCIO} = 1.2 ±5%	25	kΩ

Notes to Table 2-13:

- (1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) Valid with ±10% tolerances to cover changes over PVT.

I/O Standard Specifications

Table 2-14 through Table 2-19 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria V devices. The I/O standards tables also list the Arria V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} respectively.

For an explanation of terms used in Table 2-14 through Table 2-19, refer to “Glossary” on page 2-47.

Table 2-14. Single-Ended I/O Standards for Arria V Devices—Preliminary (Part 1 of 2)

I/O Standard	V _{CCIO} (V)			V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} - 0.2	2	-2
3.0-V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.0-V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} - 0.2	0.1	-0.1
3.0-V PCI	2.85	3	3.15	—	0.3 × V _{CCIO}	0.5 × V _{CCIO}	V _{CCIO} + 0.3	0.1 × V _{CCIO}	0.9 × V _{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 × V _{CCIO}	0.5 × V _{CCIO}	V _{CCIO} + 0.3	0.1 × V _{CCIO}	0.9 × V _{CCIO}	1.5	-0.5
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 × V _{CCIO}	0.65 × V _{CCIO}	V _{CCIO} + 0.3	0.45	V _{CCIO} - 0.45	2	-2

Table 2-14. Single-Ended I/O Standards for Arria V Devices—Preliminary (Part 2 of 2)

I/O Standard	V _{CCIO} (V)			V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.5 V	1.425	1.5	1.575	-0.3	0.35 x V _{CCIO}	0.65 x V _{CCIO}	V _{CCIO} + 0.3	0.25 x V _{CCIO}	0.75 x V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 x V _{CCIO}	0.65 x V _{CCIO}	V _{CCIO} + 0.3	0.25 x V _{CCIO}	0.75 x V _{CCIO}	2	-2

Table 2-15. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria V Devices—Preliminary

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 x V _{CCIO}	0.5 x V _{CCIO}	0.51 x V _{CCIO}	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 x V _{CCIO}	0.5 x V _{CCIO}	0.51 x V _{CCIO}	0.49 x V _{CCIO}	0.5 x V _{CCIO}	0.51 x V _{CCIO}
SSTL 135 Class I, II	1.283	1.35	1.418	0.49 x V _{CCIO}	0.5 x V _{CCIO}	0.51 x V _{CCIO}	0.49 x V _{CCIO}	0.5 x V _{CCIO}	0.51 x V _{CCIO}
SSTL 125 Class I, II	1.19	1.25	1.26	0.49 x V _{CCIO}	0.5 x V _{CCIO}	0.51 x V _{CCIO}	0.49 x V _{CCIO}	0.5 x V _{CCIO}	0.51 x V _{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V _{CCIO} /2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V _{CCIO} /2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 x V _{CCIO}	0.5 x V _{CCIO}	0.53 x V _{CCIO}	—	V _{CCIO} /2	—
HSUL-12	1.14	1.2	1.3	0.49 x V _{CCIO}	0.5 x V _{CCIO}	0.51 x V _{CCIO}	—	—	—

Table 2-16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria V Devices—Preliminary (Part 1 of 2)

I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{ol} (mA)	I _{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} - 0.31	V _{REF} + 0.31	V _{TT} - 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} - 0.31	V _{REF} + 0.31	V _{TT} - 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} - 0.25	V _{REF} + 0.25	V _{TT} - 0.603	V _{TT} + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} - 0.25	V _{REF} + 0.25	0.28	V _{CCIO} - 0.28	13.4	-13.4
SSTL-15 Class I	—	V _{REF} - 0.1	V _{REF} + 0.1	—	V _{REF} - 0.175	V _{REF} + 0.175	0.2 x V _{CCIO}	0.8 x V _{CCIO}	8	-8
SSTL-15 Class II	—	V _{REF} - 0.1	V _{REF} + 0.1	—	V _{REF} - 0.175	V _{REF} + 0.175	0.2 x V _{CCIO}	0.8 x V _{CCIO}	16	-16

Table 2-16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria V Devices—Preliminary (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OI} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL 135	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	TBD (1)	TBD (1)	TBD (1)	TBD (1)
SSTL 125	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	TBD (1)	TBD (1)	TBD (1)	TBD (1)
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	TBD (1)	TBD (1)

Note to Table 2-16:

(1) Pending silicon characterization.

Table 2-17. Differential SSTL I/O Standards for Arria V Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	-0.2	-0.15	—	0.15	-0.35	0.35	—	$V_{CCIO}/2$	—
SSTL 135	1.283	1.35	1.45	0.2	-0.2	$V_{REF} - 0.135$	$V_{CCIO}/2$	$V_{REF} + 0.135$	TBD (1)	TBD (1)	$V_{REF} - 0.15$	—	$V_{REF} + 0.15$
SSTL 125	1.19	1.25	1.31	TBD (1)	—	TBD (1)	$V_{CCIO}/2$	TBD (1)	TBD (1)	—	TBD (1)	TBD (1)	TBD (1)

Note to Table 2-17:

(1) Pending silicon characterization.

Table 2-18. Differential HSTL I/O Standards for Arria V Devices—Preliminary

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	—	0.5 x V _{CCIO}	—	0.4 x V _{CCIO}	0.5 x V _{CCIO}	0.6 x V _{CCIO}	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 x V _{CCIO} - 0.12	0.5 x V _{CCIO}	0.5 x V _{CCIO} + 0.12	0.4 x V _{CCIO}	0.5 x V _{CCIO}	0.6 x V _{CCIO}	0.44	0.44

Table 2-19. Differential I/O Standard Specifications for Arria V Devices—Preliminary ⁽¹⁾


I/O Standard	V _{CCIO} (V)			V _{ID} (mV)			V _{ICM(DC)} (V)		V _{OD} (V) ⁽²⁾			V _{OCM} (V) ⁽²⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
PCML	⁽³⁾													
2.5 V LVDS	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	1.55	0.247	—	0.6	1.125	1.25	1.375
RSDS (HIO)	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—


Notes to Table 2-19:

- (1) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 2-14.
- (2) RL range: 90 ≤ RL ≤ 110 Ω
- (3) Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 2-20 and Table 2-21.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator (EPE) and the Quartus® II PowerPlay Power Analyzer feature.

 You typically use the interactive Excel-based EPE before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

 For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no preliminary designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 2–20 and Table 2–21 list the Arria V transceiver specifications.

Table 2–20. Transceiver Specifications for Arria V GX Devices—Preliminary ⁽¹⁾ (Part 1 of 3)

Symbol/ Description	Conditions	–4 Commercial Speed Grade			–5 Commercial/Industrial Speed Grade			–6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽²⁾ , HCSL, and LVDS										
Input frequency from REFCLK input pins	—	27	—	710	27	—	710	27	—	710	MHz
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCI Express [®] (PCIe [®])	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V _{ICM} (AC coupled)	—	1.1 ⁽³⁾			1.1 ⁽³⁾			1.1 ⁽³⁾			V
V _{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
R _{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

Table 2-20. Transceiver Specifications for Arria V GX Devices—Preliminary ⁽¹⁾ (Part 2 of 3)

Symbol/ Description	Conditions	-4 Commercial Speed Grade			-5 Commercial/Industrial Speed Grade			-6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transceiver Clocks											
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Avalon [®] -Memory-Mapped (Avalon-MM) PHY management clock frequency	< 150										MHz
Receiver											
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS										
Data rate	—	611	—	6553	611	—	6553	611	—	3125	Mbps
Absolute V _{MAX} for a receiver pin ⁽⁴⁾	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V _{MIN} for a receiver pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins ⁽⁵⁾	—	85	—	—	85	—	—	85	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PCIe (Gen1 and Gen2), GIGE, XAUI, SDI, CPRI, OBSAI	Compliant									—
Programmable ppm detector ⁽⁶⁾	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000									ppm
Run Length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization	—	—	—	4	—	—	4	—	—	4	dB

Table 2-20. Transceiver Specifications for Arria V GX Devices—Preliminary ⁽¹⁾ (Part 3 of 3)

Symbol/ Description	Conditions	-4 Commercial Speed Grade			-5 Commercial/Industrial Speed Grade			-6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
Transmitter											
Supported I/O Standards	1.5 V PCML										
Data rate	—	611	—	6553	611	—	6553	611	—	3125	Mbps
V _{OCM}	—	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Rise time ⁽⁷⁾	—	30	—	160	30	—	160	30	—	160	ps
Fall time ⁽⁷⁾	—	30	—	160	30	—	160	30	—	160	ps
CMU PLL											
Supported data range	—	611	—	6553	611	—	6553	611	—	3125	Mbps
Transceiver-FPGA Fabric Interface											
Interface speed (single-width mode)	—	25	—	156.25	25	—	156.25	25	—	156.25	MHz
Interface speed (double-width mode)	—	25	—	159.375	25	—	159.375	25	—	159.375	MHz

Notes to Table 2-20:

- (1) Speed grades shown in Table 2-20 refer to the Transceiver Speed Grade in the device ordering code. For more information about device ordering codes, refer to the *Overview for Arria V Device Family* chapter.
- (2) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
- (3) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
- (4) The device cannot tolerate prolonged operation at this absolute maximum.
- (5) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (6) The rate match FIFO supports only up to ±300 parts per million (ppm).
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Table 2-21. Transceiver Specifications for Arria V GT Devices—Preliminary ⁽¹⁾ (Part 1 of 2)

Symbol/ Description	Conditions	-5 Industrial Speed Grade			Unit
		Min	Typ	Max	
Reference Clock					
Supported I/O Standards	1.2 V PCML, 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽²⁾, HCSL, and LVDS				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V _{ICM} (AC coupled)	—	1.1 ⁽³⁾			V
V _{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	mV
R _{REF}	—	—	2000 ±1%	—	Ω
Transceiver Clocks					
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	MHz
Avalon-MM PHY management clock frequency	< 150				MHz
Receiver					
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps Transceiver)	—	611	—	6375	Mbps
Data rate (10-Gbps transceiver)	—	6.376	9.8304	10.3125	Gbps
Absolute V _{MAX} for a receiver pin ⁽⁴⁾	—	—	—	1.2	V
Absolute V _{MIN} for a receiver pin	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	—	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins ⁽⁵⁾	—	85	—	—	mV
Differential on-chip termination resistors	85-Ω setting	85			Ω
	100-Ω setting	100			Ω
	120-Ω setting	120			Ω
	150-Ω setting	150			Ω

Table 2-21. Transceiver Specifications for Arria V GT Devices—Preliminary ⁽¹⁾ (Part 2 of 2)

Symbol/ Description	Conditions	-5 Industrial Speed Grade			Unit
		Min	Typ	Max	
Differential and common mode return loss	PCIe (Gen1 and Gen2), GIGE, XAUI, SDI, CPRI, OBSAI, SFI	Compliant			—
Programmable ppm detector ⁽⁶⁾	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000			ppm
Run Length	—	—	—	200	UI
Programmable equalization	—	—	—	4	dB
Programmable DC gain	DC Gain Setting = 0	—	0	—	dB
	DC Gain Setting = 1	—	3	—	dB
Transmitter					
Supported I/O Standards	1.5 V PCML				
Data rate (6-Gbps transceiver)	—	611	—	6375	Mbps
Data rate (10-Gbps transceiver)	—	6.376	9.8304	10.3125	Gbps
V _{OCM}	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Rise time ⁽⁷⁾	—	30	—	160	ps
Fall time ⁽⁷⁾	—	30	—	160	ps
CMU PLL					
Supported data range	—	0.611	—	10.3125	Gbps
Transceiver-FPGA Fabric Interface					
Interface speed (80-bit mode)	—	25	—	159.375	MHz
Interface speed (single-width mode)	—	25	—	156.25	MHz
Interface speed (double-width mode)	—	25	—	159.375	MHz

Notes to Table 2-21:

- (1) Speed grades shown in Table 2-21 refer to the Transceiver Speed Grade in the device ordering code. For more information about device ordering codes, refer to the *Overview for Arria V Device Family* chapter.
- (2) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
- (3) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
- (4) The device cannot tolerate prolonged operation at this absolute maximum.
- (5) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (6) The rate match FIFO supports only up to ±300 ppm.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Table 2-22 and Table 2-23 list the transceiver block jitter specification for Arria V devices.

Table 2-22. Transceiver Block Jitter Specification for Arria V GX Devices—Preliminary (Part 1 of 4)

Symbol/ Description	Conditions	-4 Commercial Speed Grade			-5 Commercial/ Industrial Speed Grade			-6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Transmit Jitter Generation ⁽¹⁾											
Total Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
CPRI Receiver Jitter Tolerance ⁽¹⁾											
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.65			> 0.65			> 0.65			UI
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.55			> 0.55			> 0.55			UI
OBSAI Transmit Jitter Generation ⁽²⁾											
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI

Table 2-22. Transceiver Block Jitter Specification for Arria V GX Devices—Preliminary (Part 2 of 4)

Symbol/ Description	Conditions	-4 Commercial Speed Grade			-5 Commercial/ Industrial Speed Grade			-6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance ⁽²⁾											
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			> 0.55			UI
Sinusoidal Jitter tolerance at 768 Mbps	Jitter Frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 460 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
Sinusoidal Jitter tolerance at 1536 Mbps	Jitter Frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 921.6 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
Sinusoidal Jitter tolerance at 3072 Mbps	Jitter Frequency = 21.8 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
Serial RapidIO® (SRIO) Transmit Jitter Generation ⁽³⁾											
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI

Table 2-22. Transceiver Block Jitter Specification for Arria V GX Devices—Preliminary (Part 3 of 4)

Symbol/ Description	Conditions	-4 Commercial Speed Grade			-5 Commercial/ Industrial Speed Grade			-6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SRIO Receiver Jitter Tolerance ⁽³⁾											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation ⁽⁴⁾											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance ⁽⁴⁾											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI

Table 2-22. Transceiver Block Jitter Specification for Arria V GX Devices—Preliminary (Part 4 of 4)

Symbol/ Description	Conditions	-4 Commercial Speed Grade			-5 Commercial/ Industrial Speed Grade			-6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HiGig Transmit Jitter Generation ⁽⁵⁾											
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	—	—	—	UI

Notes to Table 2-22:

- (1) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
- (2) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.
- (3) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
- (4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (5) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.

Table 2-23. Transceiver Block Jitter Specification for Arria V GT Devices—Preliminary (Part 1 of 4)

Symbol/ Description	Conditions	-5 Industrial Speed Grade			Unit
		Min	Typ	Max	
SFI Transmit Jitter Generation ⁽¹⁾					
Deterministic Jitter	Data Rate = 9.8304, 10.3125 Gbps	—	—	0.1	UI
Total Jitter	Pattern = PRBS31	—	—	0.28	UI
SFI Receive Jitter Tolerance ⁽¹⁾					
99% Jitter Tolerance	Data Rate = 9.8304, 10.3125 Gbps	>0.42			UI
Total Jitter	Pattern = PRBS31	>0.70			UI
CPRI Transmit Jitter Generation ⁽²⁾					
Total Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.279	—
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.35	—
Deterministic Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.17	—

Table 2-23. Transceiver Block Jitter Specification for Arria V GT Devices—Preliminary (Part 2 of 4)

Symbol/ Description	Conditions	-5 Industrial Speed Grade			Unit
		Min	Typ	Max	
CPRI Receive Jitter Generation ⁽²⁾					
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.66			> 0.66
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.4			> 0.4
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.65			> 0.65
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.37			> 0.37
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.55			> 0.55
OBSAI Transmit Jitter Generation ⁽³⁾					
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	—	—	0.35	—
Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	—	—	0.17	—
OBSAI Receiver Jitter Tolerance ⁽³⁾					
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55
Sinusoidal Jitter tolerance at 768 Mbps	Jitter Frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5
	Jitter Frequency = 460 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1
Sinusoidal Jitter tolerance at 1536 Mbps	Jitter Frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5
	Jitter Frequency = 921.6 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1

Table 2-23. Transceiver Block Jitter Specification for Arria V GT Devices—Preliminary (Part 3 of 4)

Symbol/ Description	Conditions	-5 Industrial Speed Grade			Unit
		Min	Typ	Max	
Sinusoidal jitter tolerance at 3072 Mbps	Jitter Frequency = 21.8 KHz Pattern = CJPAT	> 8.5			> 8.5
	Jitter Frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1
SRIO Transmit Jitter Generation ⁽⁴⁾					
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	UI
SRIO Receiver Jitter Tolerance ⁽⁴⁾					
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			UI
GIGE Transmit Jitter Generation ⁽⁵⁾					
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	UI
GIGE Receiver Jitter Tolerance ⁽⁵⁾					
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			UI

Table 2-23. Transceiver Block Jitter Specification for Arria V GT Devices—Preliminary (Part 4 of 4)

Symbol/ Description	Conditions	-5 Industrial Speed Grade			Unit
		Min	Typ	Max	
HiGig Transmit Jitter Generation ⁽⁶⁾					
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	UI

Notes to Table 2-23:

- (1) The jitter numbers for SFI are compliant to SFF-8431 Specification.
- (2) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
- (3) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.
- (4) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
- (5) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (6) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks and temperature sensing diode specifications.

Clock Tree Specifications

Table 2-24 lists the clock tree specifications for Arria V devices.

Table 2-24. Clock Tree Performance for Arria V Devices—Preliminary

Symbol	Performance			Unit
	-C4 Speed Grade	-C5, I5 Speed Grade	-C6 Speed Grade	
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 2-25 lists the Arria V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

Table 2-25. PLL Specifications for Arria V Devices—Preliminary ⁽¹⁾ (Part 1 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f _{IN}	Input clock frequency (-4 speed grade)	5	—	670 ⁽²⁾	MHz
	Input clock frequency (-5 speed grade)	5	—	622 ⁽²⁾	MHz
	Input clock frequency (-6 speed grade)	5	—	500 ⁽²⁾	MHz
f _{INPFD}	Integer input clock frequency to the PFD	5	—	325	MHz
f _{FINPFD}	Fractional input clock frequency to the PFD	50	—	TBD ⁽¹⁾	MHz

Table 2-25. PLL Specifications for Arria V Devices—Preliminary ⁽¹⁾ (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO}	PLL VCO operating range (–4 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–5 speed grade)	600	—	1400	MHz
	PLL VCO operating range (–6 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (–4 speed grade)	—	—	500 ⁽³⁾	MHz
	Output frequency for internal global or regional clock (–5 speed grade)	—	—	500 ⁽³⁾	MHz
	Output frequency for internal global or regional clock (–6 speed grade)	—	—	400 ⁽³⁾	MHz
f_{OUT_EXT}	Output frequency for external clock output (–4 speed grade)	—	—	670 ⁽³⁾	MHz
	Output frequency for external clock output (–5 speed grade)	—	—	622 ⁽³⁾	MHz
	Output frequency for external clock output (–6 speed grade)	—	—	500 ⁽³⁾	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	—	TBD ⁽¹⁾	—
$t_{DYCONFIGCLK}$	Dynamic Configuration Clock	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of $areset$	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth ⁽⁸⁾	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the $areset$ signal	10	—	—	ns
t_{INCCJ} ^{(4), (5)}	Input clock cycle-to-cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($F_{REF} < 100$ MHz)	—	—	+750	ps (p-p)
t_{OUTPJ_DC} ⁽⁶⁾	Period jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	TBD ⁽¹⁾	ps (p-p)
	Period jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	TBD ⁽¹⁾	mUI (p-p)
t_{OUTCCJ_DC} ⁽⁶⁾	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	TBD ⁽¹⁾	ps (p-p)
	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	TBD ⁽¹⁾	mUI (p-p)
t_{OUTPJ_IO} ^{(6), (9)}	Period Jitter for clock output on the regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	TBD ⁽¹⁾	ps (p-p)
	Period Jitter for clock output on the regular I/O ($F_{OUT} < 100$ MHz)	—	—	TBD ⁽¹⁾	mUI (p-p)
t_{OUTCCJ_IO} ^{(6), (9)}	Cycle-to-cycle jitter for clock output on the regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	TBD ⁽¹⁾	ps (p-p)
	Cycle-to-cycle jitter for clock output on the regular I/O ($F_{OUT} < 100$ MHz)	—	—	TBD ⁽¹⁾	mUI (p-p)

Table 2-25. PLL Specifications for Arria V Devices—Preliminary ⁽¹⁾ (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{OUTPJ_DC_F}}$	Period jitter for dedicated clock output in fractional mode	—	—	TBD ⁽¹⁾	—
$t_{\text{OUTCGJ_DC_F}}$	Cycle-to-cycle jitter for dedicated clock output in fractional mode	—	—	TBD ⁽¹⁾	—
$t_{\text{OUTPJ_IO_F}}$	Period Jitter for clock output on the regular I/O in fractional mode	—	—	TBD ⁽¹⁾	—
$t_{\text{OUTCGJ_IO_F}}$	Cycle-to-cycle jitter for clock output on the regular I/O in fractional mode	—	—	TBD ⁽¹⁾	—
$t_{\text{CASC_OUTPJ_DC}}$ ^{(6), (7)}	Period jitter for dedicated clock output in cascaded PLLs ($F_{\text{OUT}} \geq 100$ MHz)	—	—	TBD ⁽¹⁾	ps (p-p)
	Period jitter for dedicated clock output in cascaded PLLs ($F_{\text{OUT}} < 100$ MHz)	—	—	TBD ⁽¹⁾	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μ s	—	—	± 10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	24	—	bits
k_{VALUE}	Numerator of Fraction	TBD ⁽¹⁾	8388608	TBD ⁽¹⁾	—
f_{RES}	Resolution of VCO frequency ($f_{\text{INPFD}} = 100$ MHz)	—	5.96	—	Hz

Notes to Table 2-25:

- (1) Pending silicon characterization.
- (2) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (3) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.
- (4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (5) F_{REF} is f_{IN}/N when $N = 1$.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404 % confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in [Table 2-33 on page 2-34](#).
- (7) The cascaded PLL specification is only applicable with the following conditions:
 - a. Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
 - b. Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$
- (8) High bandwidth PLL settings are not supported in external feedback mode.
- (9) External memory interface clock output jitter specifications use a different measurement method, which are available in [Table 2-33 on page 2-34](#).

DSP Block Specifications

Table 2-26 lists the Arria V DSP block performance specifications.

Table 2-26. DSP Block Performance Specifications for Arria V Devices—Preliminary

Mode	Performance			Unit
	-C4 Speed Grade	-C5, I5 Speed Grade	-C6 Speed Grade	
Modes using One DSP Block				
Independent 9 x 9 Multiplication	370	310	220	MHz
Independent 18 x 19 Multiplication	370	310	220	MHz
Independent 18 x 18 Multiplication	370	310	220	MHz
Independent 27 x 27 Multiplication	310	250	200	MHz
Independent 18 x 25 Multiplication	370	310	220	MHz
Independent 20 x 24 Multiplication	370	310	220	MHz
Two 18 x 19 Multiplier Adder Mode	370	310	220	MHz
18 x 18 Multiplier Added Summed with 36-bit Input	370	310	220	MHz
Modes using Two DSP Blocks				
Complex 18 x 19 multiplication	370	310	220	MHz
Two 27 x 27 Multiplier Adder	310	250	200	MHz
Four 18 x 19 Multiplier Adder	370	310	220	MHz

Memory Block Specifications

Table 2-27 lists the Arria V memory block specifications.

Table 2-27. Memory Block Performance Specifications for Arria V Devices—Preliminary^{(1), (2)} (Part 1 of 2)

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	C4 Speed Grade	C5,I5 Speed Grade	C6 Speed Grade	
MLAB	Single port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz
	ROM, all supported width	—	—	500	450	400	MHz

Table 2-27. Memory Block Performance Specifications for Arria V Devices—Preliminary^{(1), (2)} (Part 2 of 2)

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	C4 Speed Grade	C5,I5 Speed Grade	C6 Speed Grade	
M10K Block	Single-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	315	275	240	MHz
	True dual port, all supported widths	0	1	400	350	285	MHz
	ROM, all supported widths	0	1	400	350	285	MHz
	Min Pulse Width (clock high time)	—	—	1,275	1,360	1,445	ps
	Min Pulse Width (clock low time)	—	—	850	1,060	1,175	ps

Notes to Table 2-27:

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX} .

Temperature Sensing Diode Specifications

Table 2-28 lists the specifications for the Arria V internal temperature sensing diode.

Table 2-28. Internal Temperature Sensing Diode Specifications for Arria V Devices—Preliminary

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40 to 100°C	±8°C	No	Frequency: 1 MHz	< 100 ms	8 bits	8 bits

Periphery Performance

This section describes periphery performance and the high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. GPIO standards such as 3.3-, 2.5-, 1.8-, and 1.5-V **LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2 **LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.



Actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 2-29 lists high-speed I/O timing for Arria V devices.

Table 2-29. High-Speed I/O Specifications for Arria V Devices—Preliminary^{(1), (2), (3)} (Part 1 of 3)

Symbol	Conditions	-4 Speed Grade			-5 Speed Grade			-6 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_in}}$ (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 ⁽⁵⁾	5	—	625	5	—	625	5	—	TBD	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single Ended I/O Standards ⁽⁴⁾	Clock boost factor W = 1 to 40 ⁽⁵⁾	5	—	625	5	—	625	5	—	TBD	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single Ended I/O Standards ⁽³⁾	Clock boost factor W = 1 to 40 ⁽⁵⁾	5	—	TBD	5	—	TBD	5	—	TBD	MHz
$f_{\text{HCLK_OUT}}$ (output clock frequency)	—	5	—	625 ⁽⁶⁾	5	—	625 ⁽⁶⁾	5	—	TBD ⁽⁶⁾	MHz
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10	⁽⁷⁾	—	1250	⁽⁷⁾	—	1250	⁽⁷⁾	—	1050	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	⁽⁷⁾	—	⁽⁷⁾	⁽⁷⁾	—	⁽⁷⁾	⁽⁷⁾	—	⁽⁷⁾	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) ⁽⁸⁾	SERDES factor J = 4 to 10	⁽⁷⁾	—	TBD	⁽⁷⁾	—	TBD	⁽⁷⁾	—	TBD	Mbps
$t_{\text{x Jitter}}$ - True Differential I/O Standards	Total Jitter for Data Rate, 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate, < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

Table 2-29. High-Speed I/O Specifications for Arria V Devices—Preliminary^{(1), (2), (3)} (Part 2 of 3)

Symbol	Conditions	-4 Speed Grade			-5 Speed Grade			-6 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _x Jitter - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate, 600 Mbps – 1.25 Gbps	—	—	TBD	—	—	TBD	—	—	TBD	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	TBD	—	—	TBD	—	—	TBD	UI
t _{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t _{RISE} & t _{FALL}	True Differential I/O Standards	—	—	200	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver											
True Differential I/O Standards - f _{HSDRDPA} (data rate)	SERDES factor J = 3 to 10	—	—	1250	—	—	1250	—	—	1050	Mbps
f _{HSDR} (data rate)	SERDES factor J = 3 to 10	(7)	—	(9)	(7)	—	(9)	(7)	—	(9)	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	(7)	—	(7)	(7)	—	(7)	(7)	—	(7)	Mbps
DPA Mode											
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode											
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	± ppm

Table 2-29. High-Speed I/O Specifications for Arria V Devices—Preliminary (1), (2), (3) (Part 3 of 3)

Symbol	Conditions	-4 Speed Grade			-5 Speed Grade			-6 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Non DPA Mode											
Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

Notes to Table 2-29:

- (1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.
- (2) When J = 1 or 2, bypass the SERDES block.
- (3) This applies to LVDS source synchronous mode only.
- (4) This applies to DPA and soft-CDR modes only.
- (5) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.
- (6) This is achieved by using the LVDS clock network.
- (7) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
- (8) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.
- (9) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Figure 2-1 shows the DPA lock time specifications with the DPA PLL calibration option enabled.

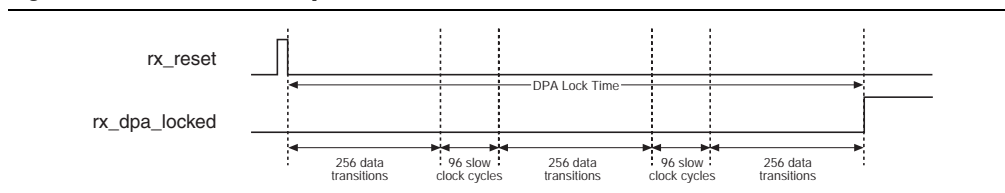
Figure 2-1. DPA Lock Time Specification with DPA PLL Calibration Enabled

Table 2-30 lists the DPA lock time specifications for Arria V devices.

Table 2-30. DPA Lock Time Specifications for Arria V Devices—Preliminary (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (4)	Maximum
SPI-4	000000000111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 2-30:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grades.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 2-2 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.25 Gbps.

Figure 2-2. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

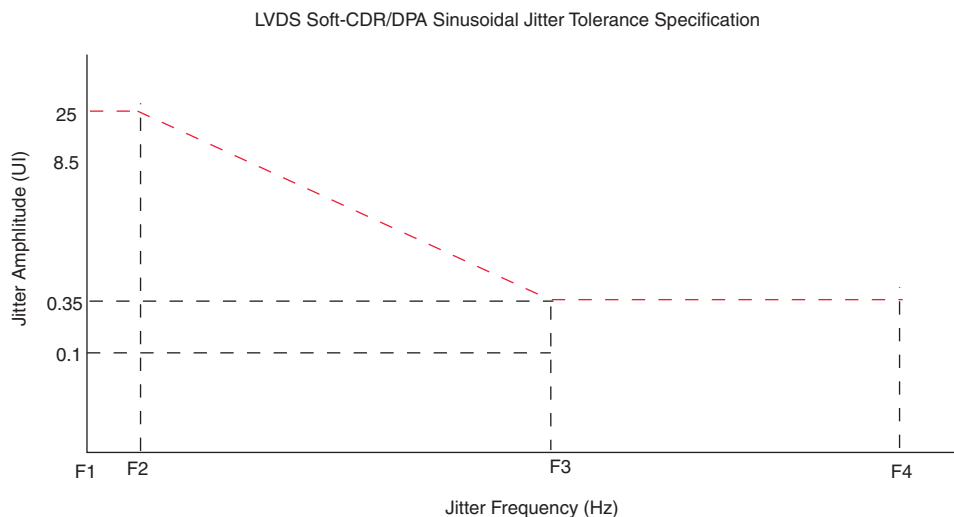


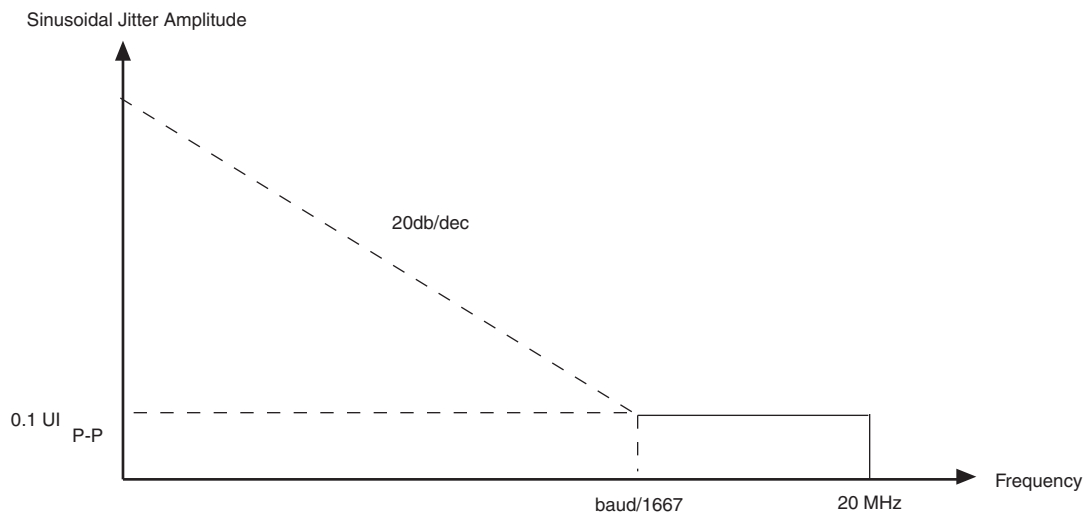
Table 2-31 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.25 Gbps.

Table 2-31. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps—Preliminary

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 2-3 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate less than 1.25 Gbps.

Figure 2-3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DQS Logic Block and Memory Output Clock Jitter Specifications

Table 2-32 lists the DQS phase shift error for Arria V devices.

Table 2-32. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V Devices—Preliminary ^{(1), (2)}

Number of DQS Delay Buffer	-C4 Speed Grade	-C5, I5 Speed Grade	-C6 Speed Grade	Unit
2	57	58	74	ps

Notes to Table 2-32:

- (1) The numbers are preliminary pending silicon characterization.
- (2) This error specification is the absolute maximum and minimum error. For example, skew on two DQS delay buffers in a -4 speed grade is 58 ps or ± 29 ps.

Table 2-33 lists the memory output clock jitter specifications for Arria V devices.

Table 2-33. Memory Output Clock Jitter Specification for Arria V Devices—Preliminary ⁽¹⁾ (Part 1 of 2)

Parameter	Clock Network	Symbol	-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	Regional	$t_{JIT(per)}$	-50	50	-55	55	-55	55	ps
Cycle-to-cycle period jitter	Regional	$t_{JIT(cc)}$	-100	100	-110	110	-110	110	ps
Duty cycle jitter	Regional	$t_{JIT(duty)}$	-50	50	-82.5	82.5	-82.5	82.5	ps
Clock period jitter	Global	$t_{JIT(per)}$	-75	75	-82.5	82.5	-82.5	82.5	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-150	150	-165	165	-165	165	ps

Table 2-33. Memory Output Clock Jitter Specification for Arria V Devices—Preliminary ⁽¹⁾ (Part 2 of 2)

Parameter	Clock Network	Symbol	-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
Duty cycle jitter	Global	$t_{JIT(duty)}$	-75	75	-90	90	-90	90	ps

Note to Table 2-33:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

OCT Calibration Block Specifications

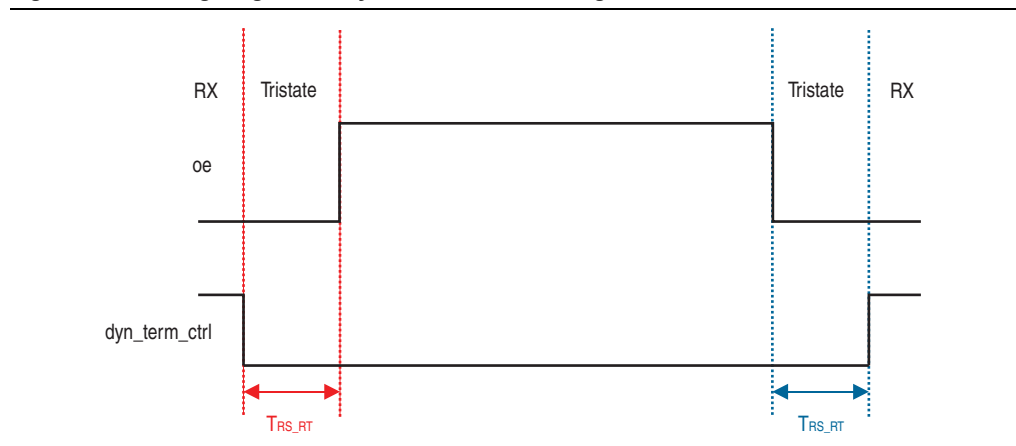
Table 2-34 lists the OCT calibration block specifications for Arria V devices.

Table 2-34. OCT Calibration Block Specifications for Arria V Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT / R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 2-4 shows the T_{RS_RT} for `dyn_term_ctrl` and `oe` signals.

Figure 2-4. Timing Diagram for `dyn_term_ctrl` and `oe` Signals



Duty Cycle Distortion (DCD) Specifications

Table 2–35 lists the worst-case DCD for Arria V devices.

Table 2–35. Worst-Case DCD on Arria V I/O Pins—Preliminary

Symbol	–C4 Speed Grade		–C5,I5 Speed Grade		–C6 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Configuration Specification

This section provides configuration specifications and timing for Arria V devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

POR Specifications

Table 2–36 lists the specifications for fast and standard POR for Arria V devices.

Table 2–36. Fast and Standard POR Delay Specification for Arria V Devices ⁽¹⁾

POR Delay	Minimum (ms)	Maximum (ms)
Fast ⁽²⁾	4	12
Standard ⁽³⁾	100	300

Notes to Table 2–36:

- (1) Select the POR delay based on the MSEL setting as described in the “Configuration Schemes for Arria V Devices” table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.
- (2) When the PORSEL signal is **high**, the device is in fast POR delay.
- (3) When the PORSEL signal is **low**, the device is in standard POR delay.

JTAG Configuration Timing

Table 2–37 lists the JTAG timing parameters and values for Arria V devices.

Table 2–37. JTAG Timing Parameters and Values for Arria V Devices—Preliminary (Part 1 of 2)

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30	—	ns
t _{JCH}	TCK clock high time	14	—	ns
t _{JCL}	TCK clock low time	14	—	ns
t _{JPSU (TDI)}	TDI JTAG port setup time	1	—	ns

Table 2-37. JTAG Timing Parameters and Values for Arria V Devices—Preliminary (Part 2 of 2)

Symbol	Description	Min	Max	Unit
$t_{JPSU(TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Note to Table 2-37:

- (1) A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, $t_{JPCO} = 12$ ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

FPP Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Arria V devices.

DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Table 2-38 lists the DCLK-to-DATA[] ratio for each combination.

Table 2-38. DCLK-to-DATA[] Ratio for Arria V Devices ⁽¹⁾

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4

Note to Table 2-38:

- (1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP x16 where the r is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

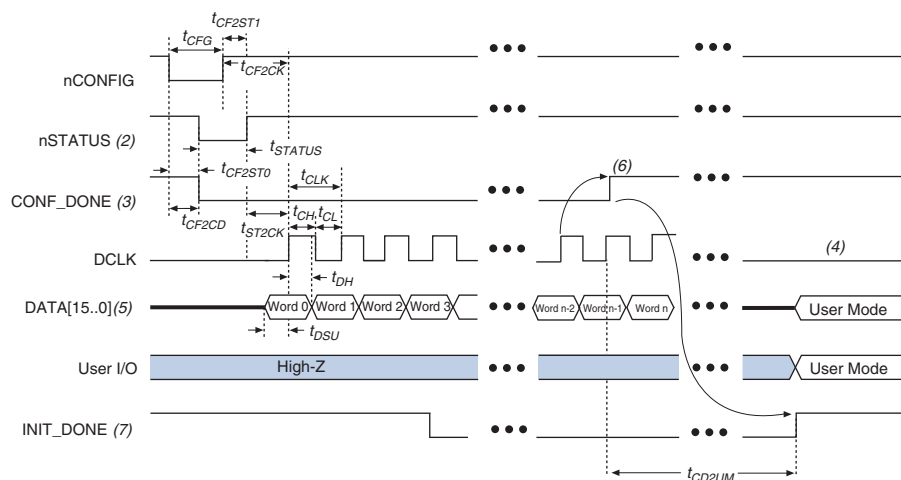
FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2-5 shows the timing waveform for a FPP configuration when using a MAX[®] II device as an external host. This timing waveform shows timing when the DCLK-to-DATA[] ratio is 1.



When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP x8 and FPP x16. For the respective DCLK-to-DATA[] ratio, refer to Table 2-38.

Figure 2-5. DCLK-to-DATA[] FPP Configuration Timing Waveform When the Ratio is 1 ⁽¹⁾



Notes to Figure 2-5:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power up, the Arria V device holds nSTATUS low for the time of the POR delay.
- (3) After power up, before and during configuration, CONF_DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) For FPP x16, use DATA [15..0]. For FPP x8, use DATA [7..0]. DATA [15..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (6) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high when the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-39 lists the timing parameters for Arria V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 2-39. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is 1—Preliminary ⁽¹⁾ (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1506 ⁽²⁾	μ s

Table 2-39. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is 1—Preliminary ⁽¹⁾ (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽³⁾	μ s
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	μ s
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	ns
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	ns
t_{CLK}	DCLK period	$1/f_{MAX}$	—	ns
f_{MAX}	DCLK frequency (FPP x8/ x16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽⁴⁾	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times$ maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

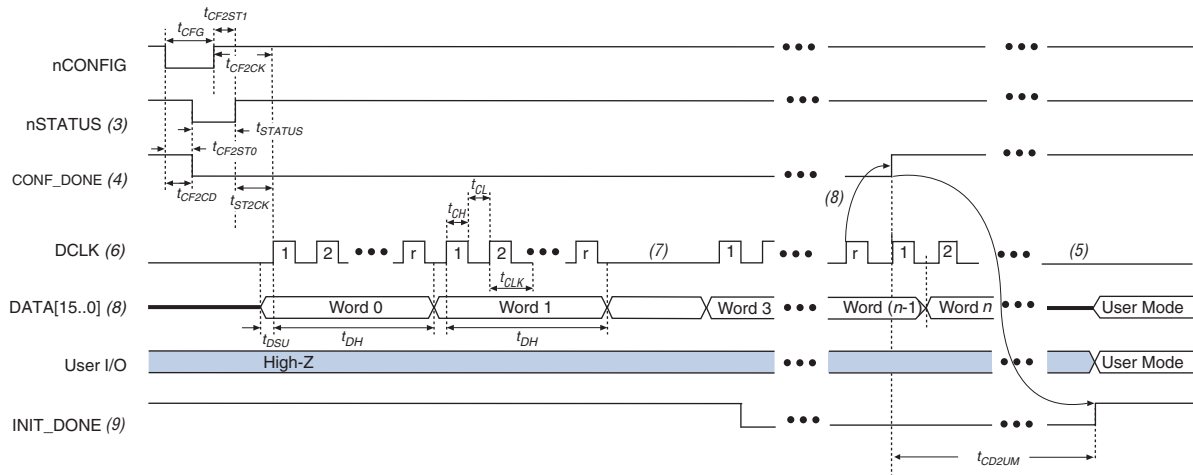
Notes to Table 2-39:

- (1) Use these timing parameters when the DCLK-to-DATA[] ratio is 1. To find the DCLK-to-DATA[] ratio for your system, refer Table 2-38 on page 2-37.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.
- (3) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2-6 shows the timing waveform for a FPP configuration when using a MAX II device or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Figure 2-6. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)



Notes to Figure 2-6:

- (1) To find the DCLK-to-DATA [] ratio for your system, refer [Table 2-38 on page 2-37](#).
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power up, the Arria V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA [] ratio. For the DCLK-to-DATA [] ratio based on the decompression and the design security feature enable settings, refer to [Table 2-38 on page 2-37](#).
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA [15..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high after the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2–40 lists the timing parameters for Arria V devices when the DCLK-to-DATA [] ratio is more than 1.

Table 2–40. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is >1—Preliminary⁽¹⁾

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1506 ⁽²⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽³⁾	μ s
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	μ s
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA [] hold time after rising edge on DCLK	$3 \times 1/f_{DCLK}$	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	ns
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	ns
t_{CLK}	DCLK period	$1/f_{MAX}$	—	ns
f_{MAX}	DCLK frequency (FPP x8/ x16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽⁴⁾	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times$ maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

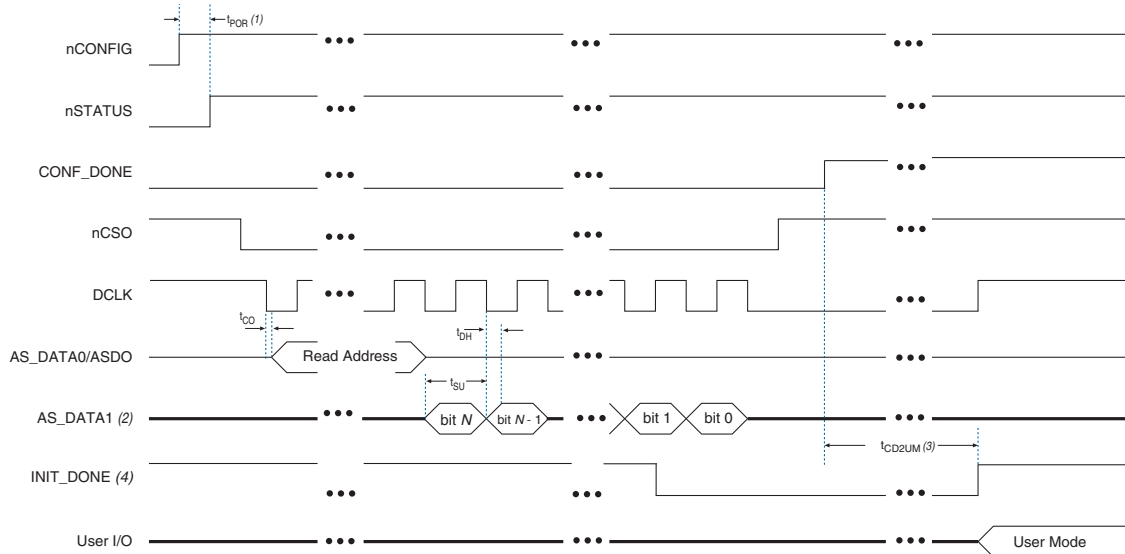
Notes to Table 2–40:

- (1) Use these timing parameters when you use decompression and the design security features.
- (2) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

AS Configuration Timing

Figure 2-7 shows the timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Figure 2-7. AS Configuration Timing



Notes to Figure 2-7:

- (1) The AS scheme supports standard and fast POR delay (t_{POR}). For t_{POR} delay information, refer to the “POR Delay Specification” section in the *Configuration, Design Security, and remote System Upgrades in Arria V Devices* chapter.
- (2) If you are using AS x4 mode, this signal represents the AS_DATA [3 . . 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (3) The initialization clock can be from the internal oscillator or CLKUSR pin.
- (4) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-41 lists the timing parameters for AS x1 and AS x4 configurations in Arria V devices.

Table 2-41. AS Timing Parameters for AS x1 and x4 Configurations in Arria V Devices—Preliminary (1), (2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	4	μ s
t_{SU}	Data setup time before the rising edge on DCLK	1.5	—	ns
t_{H}	Data hold time after the rising edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 2-41:

- (1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (2) The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 2-43 on page 2-44.

Table 2-42 lists the internal clock frequency specification for the AS configuration scheme.

Table 2-42. DCLK Frequency Specification in the AS Configuration Scheme—Preliminary^{(1), (2)}

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

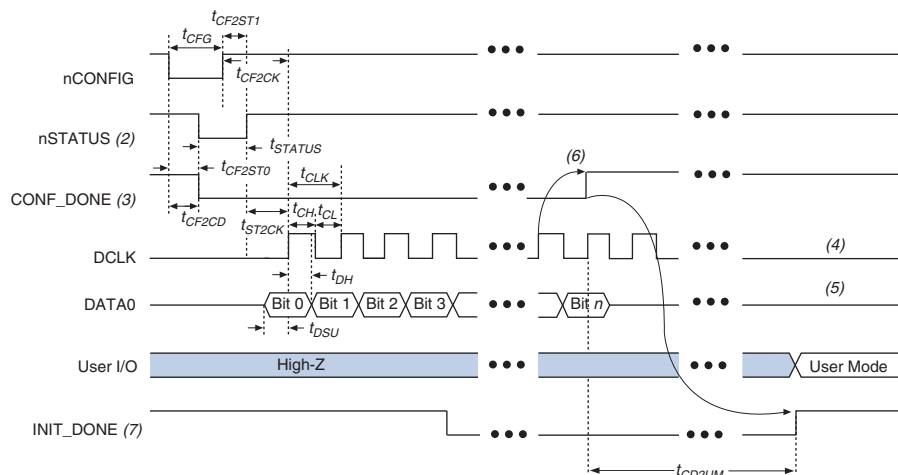
Notes to Table 2-42:

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

PS Configuration Timing

Figure 2-8 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device or microprocessor as an external host.

Figure 2-8. PS Configuration Timing Waveform⁽¹⁾



Notes to Figure 2-8:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power up, the Arria V device holds nSTATUS low for the time of the POR delay.
- (3) After power up, before and during configuration, CONF_DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high after the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-43 lists the PS timing parameter for Arria V devices.

Table 2-43. PS Timing Parameters for Arria V Devices—Preliminary

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1506 ⁽¹⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽²⁾	μ s
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	μ s
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	ns
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	ns
t_{CLK}	DCLK period	$1/f_{MAX}$	—	ns
f_{MAX}	DCLK frequency	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 2-43:

- (1) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (2) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.
- (3) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Remote System Upgrades Circuitry Timing Specification

Table 2-44 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 2-44. Remote System Upgrade Circuitry Timing Specification

Parameter	Minimum	Maximum	Unit
$t_{\text{MAX_RU_CLK}}$ ⁽¹⁾	—	40	MHz
$t_{\text{RU_nCONFIG}}$ ⁽²⁾	250	—	ns
$t_{\text{RU_nRSTIMER}}$ ⁽³⁾	250	—	ns

Notes to Table 2-44:

- (1) This clock is user-supplied to the remote system upgrade circuitry. If you are using the ALTREMOTE_UPDATE megafunction, the clock user-supplied to the ALTREMOTE_UPDATE megafunction must meet this specification.
- (2) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the “Remote System Upgrade State Machine” section in the *Device Interfaces and Integration Basics for Arria V Devices* chapter.
- (3) This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the “User Watchdog Timer” section in the *Device Interfaces and Integration Basics for Arria V Devices* chapter.

User Watchdog Internal Oscillator Frequency Specification

Table 2-45 lists the frequency specifications for the user watchdog internal oscillator.

Table 2-45. User Watchdog Internal Oscillator Frequency Specifications—Preliminary

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.



You can download the Excel-based I/O Timing spreadsheet from the [Arria V Devices Literature](#) webpage.

Programmable IOE Delay

Table 2-46 lists the Arria V IOE programmable delay settings.

Table 2-46. IOE Programmable Delay for Arria V Devices ⁽¹⁾

Parameter	Available Settings	Minimum Offset	Fast Model		Slow Model			Unit
			Industrial	Commercial	C4	C5, I5	C6	
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Note to Table 2-46:

(1) Pending the Quartus II software extraction.

Programmable Output Buffer Delay

Table 2-47 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 2-47. Programmable Output Buffer Delay—Preliminary ^{(1), (2)}

Symbol	Parameter	Typical	Unit
D _{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Notes to Table 2-47:

- (1) Pending the Quartus II software extraction.
- (2) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 2-48 lists the glossary for this chapter.

Table 2-48. Glossary Table (Part 1 of 4)

Letter	Subject	Definitions
A		
B		
C		
D	Differential I/O Standards	<p><i>Receiver Input Waveforms</i></p> <p><i>Transmitter Output Waveforms</i></p>
E		
F	f_{HSCLK}	Left/right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{\text{HSDR}} = 1/\text{TUI}$), non-DPA.
	f_{HSDRDPA}	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{\text{HSDRDPA}} = 1/\text{TUI}$), DPA.
G		
H		
I		

Table 2-48. Glossary Table (Part 2 of 4)

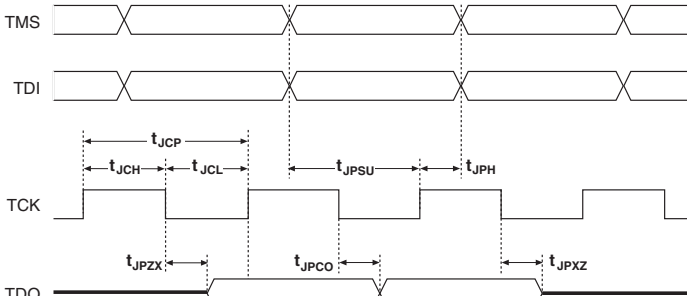
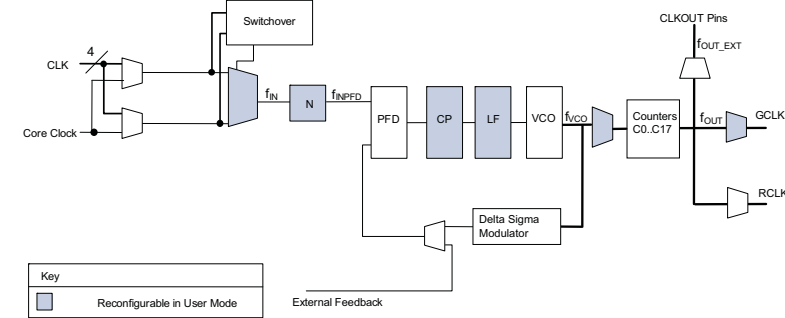
Letter	Subject	Definitions
J	J	High-speed I/O block—Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	<p>JTAG Timing Specifications:</p> 
K L M N O	—	—
P	PLL Specifications	<p>Diagram of PLL Specifications (1)</p>  <p>Note: (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p>
Q	—	—
R	R _L	Receiver differential input discrete resistor (external to the Arria V device).

Table 2-48. Glossary Table (Part 3 of 4)

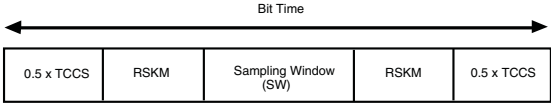
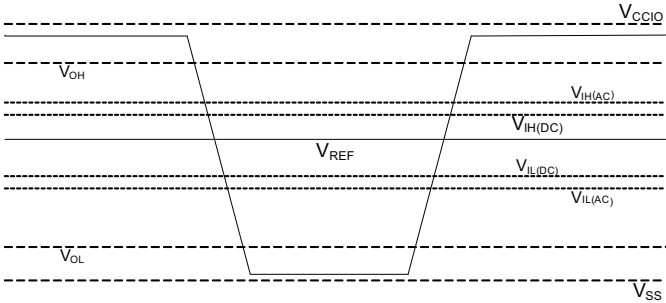
Letter	Subject	Definitions
S	Sampling window (SW)	<p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:</p> 
	Single-ended voltage referenced I/O standard	<p>The JEDEC standard for the SSTI and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p> 
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{C0} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under SW in this table).
	t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock. Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80–20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
	t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)	
U	—	—

Table 2–48. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC Common mode input voltage.
	V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
V_{OX}	Output differential cross point voltage	
W	W	High-speed I/O block—Clock Boost Factor
X, Y, Z	—	—

Document Revision History

Table 2–49 lists the revision history for this chapter.

Table 2–49. Document Revision History

Date	Version	Changes
November, 2011	1.1	<ul style="list-style-type: none"> ■ Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36. ■ Added Table 2–5. ■ Added Figure 2–4.
August 2011	1.0	Initial release.