Arria V GX, GT, SX, and ST Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in –C4(fastest), –C5, and –C6 speed grades. Industrial grade devices are offered in the –I3 and –I5 speed grades.

For more information about the densities and packages of devices in the Arria V family, refer to the *Arria V Device Overview*.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

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Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

CAUTION Conditions outside the range listed in Table 1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1. Absolute Maximum Ratings for Arria V Devices—*Preliminary*

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	–0.50	1.35	V
V_{CCP}	Periphery circuitry, PCIe® hard IP block, and transceiver physical coding sublayer (PCS) power supply	–0.50	1.35	V
V_{CCPGM}	Configuration pins power supply	–0.50	3.75	V
V_{CCAUX}	Auxiliary supply	–0.50	3.75	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.50	3.75	V
V_{CCPD}	I/O pre-driver power supply	–0.50	3.75	V
V_{CCIO}	I/O power supply	–0.50	3.90	V
V_{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	–0.50	1.80	V
V_{CCA_FPLL}	PLL analog power supply	–0.50	3.75	V
V_{CCA_GXB}	Transceiver high voltage power	–0.50	3.75	V
V_{CCH_GXB}	Transmitter output buffer power	–0.50	1.80	V
V_{CCR_GXB}	Receiver power	–0.50	1.35	V
V_{CCT_GXB}	Transmitter power	–0.50	1.35	V
V_{CCL_GXB}	Clock network power	–0.50	1.35	V
V_I	DC input voltage	–0.50	3.70	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.50	1.35	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.50	3.75	V
V_{CCIO_HPS}	HPS I/O power supply	–0.50	3.90	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	–0.50	3.75	V
V_{CCPLL_HPS}	HPS PLL analog power supply	–0.50	3.75	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (No bias)	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in Table 2 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 3.95 V can only be at 3.95 V for ~5% over the lifetime of the device; for a device lifetime of 10 years, this amounts to half a year.

Table 2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Table 2. Maximum Allowed Overshoot During Transitions for Arria V Devices—*Preliminary*

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Table 3 lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 3. Recommended Operating Conditions for Arria V Devices—*Preliminary* (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCP}	Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCPGM}	Configuration pins (3.3 V) power supply	—	3.135	3.3	3.465	V
	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCAUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCBAT} (1)	Battery back-up power supply (For design security volatile key register)	—	1.2	1.5	3.0	V
V_{CCPD} (2)	I/O pre-driver (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.418	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.425	1.5	1.575	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C

Table 3. Recommended Operating Conditions for Arria V Devices—*Preliminary* (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
t_{RAMP} (3)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Notes to Table 3:

(1) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} stays low.

(2) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

(3) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

Table 4 lists recommended operating conditions for Arria V transceiver power supplies.

Table 4. Transceiver Power Supply Operating Conditions for Arria V GX and GT Devices—*Preliminary*

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_GXBL}	Transceiver high voltage power (left side)	2.375	2.500	2.625	V
V_{CCA_GXBR}	Transceiver high voltage power (right side)				
V_{CCR_GXBL}	All GX speed grades—receiver power (left side)	1.08/1.12	1.1/1.15 (1)	1.14/1.18	V
V_{CCR_GXBR}	All GX speed grades—receiver power (right side)				
V_{CCR_GXBL}	All GT speed grades—receiver power (left side)	1.17	1.20	1.23	V
V_{CCR_GXBR}	All GT speed grades—receiver power (right side)				
V_{CCT_GXBL}	All GX speed grades—transmitter power (left side)	1.08/1.12	1.1/1.15 (1)	1.14/1.18	V
V_{CCT_GXBR}	All GX speed grades—transmitter power (right side)				
V_{CCT_GXBL}	All GT speed grades—transmitter power (left side)	1.17	1.20	1.23	V
V_{CCT_GXBR}	All GT speed grades—transmitter power (right side)				
V_{CCH_GXBL}	Transmitter output buffer power (left side)	1.425	1.500	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power (right side)				
V_{CCL_GXBL}	All GX speed grades—clock network power (left side)	1.08/1.12	1.1/1.15 (1)	1.14/1.18	V
V_{CCL_GXBR}	All GX speed grades—clock network power (right side)				
V_{CCL_GXBL}	All GT speed grades—clock network power (left side)	1.17	1.20	1.23	V
V_{CCL_GXBR}	All GT speed grades—clock network power (right side)				

Note to Table 4:

(1) For data rate <=3.2 Gbps, connect $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, or $V_{CCL\_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, or $V_{CCL\_GXBL/R}$ to a 1.15-V power supply. For details, refer to the *Arria V Device Family Pin Connection Guidelines*.

Table 5 lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) FPGA with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus.

Table 5. HPS Power Supply Operating Conditions for Arria V SX and ST Devices (1)—*Preliminary*

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CC_HPS}	HPS Core voltage and periphery circuitry power supply	1.07	1.1	1.13	V
V_{CCPD_HPS}	HPS I/O pre-driver (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O pre-driver (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O pre-driver (2.5 V) power supply	2.375	2.5	2.625	V
V_{CCIO_HPS}	HPS I/O buffers (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O buffers (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O buffers (2.5 V) power supply	2.375	2.5	2.625	V
	HPS I/O buffers (1.8 V) power supply	1.71	1.8	1.89	V
	HPS I/O buffers (1.5 V) power supply	1.425	1.5	1.575	V
	HPS I/O buffers (1.2 V) power supply	1.14	1.2	1.26	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins (3.3 V) power supply	3.135	3.3	3.465	V
	HPS reset and clock input pins (3.0 V) power supply	2.85	3.0	3.15	V
	HPS reset and clock input pins (2.5 V) power supply	2.375	2.5	2.625	V
	HPS reset and clock input pins (1.8 V) power supply	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	2.375	2.5	2.625	V
$V_{CC\_AUX\_SHARED}$	HPS and FPGA shared auxiliary power supply	2.375	2.5	2.625	V

Note to Table 5:

(1) Refer to Table 3 for the steady-state voltage values expected from the FPGA portion of the Arria V system-on-a-chip (SoC) FPGAs.

DC Characteristics

This section lists the following specifications:

- Supply Current and Power Consumption
- I/O Pin Leakage Current
- Bus Hold Specifications
- OCT Specifications
- Pin Capacitance
- Hot Socketing

Supply Current and Power Consumption

Standby current is the current drawn from the respective power rails used for power budgeting.

Altera offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Quartus® II PowerPlay Power Analyzer feature.

Use the Excel-based Early Power Estimator (EPE) before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 6 lists the Arria V I/O pin leakage current specifications.

Table 6. I/O Pin Leakage Current for Arria V Devices—*Preliminary*

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 7 lists the Arria V device bus hold specifications.

Table 7. Bus Hold Parameters for Arria V Devices (1)—*Preliminary*

Parameter	Symbol	Conditions	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max.)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min.)	–8	—	–12	—	–30	—	–50	—	–70	—	-70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-125	—	-175	—	-200	—	-300	—	-500	—	-500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 7:

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

OCT Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 8 lists the Arria V OCT termination calibration accuracy specifications.

Table 8. OCT Calibration Accuracy Specifications for Arria V Devices (1)—*Preliminary*

Symbol	Description	Conditions (V)	Calibration Accuracy			Unit
			I3, C4	I5, C5	C6	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

Note to Table 8:

(1) OCT calibration accuracy is valid at the time of calibration only.

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 9 lists the Arria V OCT without calibration resistance tolerance to PVT changes.

Table 9. OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices—*Preliminary*

Symbol	Description	Conditions (V)	Resistance Tolerance			Unit
			I3, C4	I5, C5	C6	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0 and 2.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5	±25	±40	±40	%

Use Table 10 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration (1), (2), (3), (4), (5), (6)—*Preliminary*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T\rangle \pm \langle \frac{dR}{dV} \times \Delta V\rangle\right)$$

Notes to Equation 1:

(1) The R_{OCT} value calculated from Equation 1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 10 lists OCT variation with temperature and voltage after power-up calibration.

Table 10. OCT Variation after Power-Up Calibration for Arria V Devices (1)—*Preliminary*

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation of voltage without recalibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation of temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Note to Table 10:

(1) Valid for a V_{CCIO} range of ±5% and temperature range of 0° to 85°C.

Pin Capacitance

Table 11 lists the Arria V pin capacitance.

Table 11. Pin Capacitance for Arria V Devices

Symbol	Description	Value	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	5.5	pF
C_{IOLR}	Input capacitance on left/right I/O pins	5.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	5.5	pF
C_{IOVREF}	Input capacitance on V_{REF} pins	48	pF

Hot Socketing

Table 12 lists the hot socketing specifications for Arria V devices.

Table 12. Hot Socketing Specifications for Arria V Devices—*Preliminary*

Symbol	Description	Maximum
$I_{IOPIN (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR-TX (DC)}$	DC current per transceiver transmitter (TX) pin	100 mA
$I_{XCVR-RX (DC)}$	DC current per transceiver receiver (RX) pin	50 mA

Note to Table 12:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 13 lists the weak pull-up resistor values for Arria V devices.

Table 13. Internal Weak Pull-Up Resistor Values for Arria V Devices (1), (2)—*Preliminary*

Symbol	Description	Conditions (V) (3)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.3 ±5%	25	kΩ
		V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Notes to Table 13:

(1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG `TCK` pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(4) Valid with ±10% tolerances to cover changes over PVT.

I/O Standard Specifications

Table 14 through Table 19 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria V devices.

For an explanation of terms used in Table 14 through Table 19, refer to "Glossary" on page 1–58.

Table 14. Single-Ended I/O Standards for Arria V Devices—*Preliminary* (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (1) (mA)	I_{OH} (1) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
3.0-V PCI	2.85	3	3.15	—	0.3 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2

Table 14. Single-Ended I/O Standards for Arria V Devices—*Preliminary* (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (1) (mA)	I_{OH} (1) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.2 V	1.14	1.2	1.26	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2

Note to Table 14:

(1) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **SSTL15CI** specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the handbook.

Table 15. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria V Devices—*Preliminary*

I/O Standard	V_{CCIO}(V)			V_{REF}(V)			V_{TT}(V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 x V_{CCIO}	0.5 x V_{CCIO}	0.53 x V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	—	—	—

Table 16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria V Devices—*Preliminary* (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (1) (mA)	I_{oh} (1) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} –0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} –0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	8	–8

Table 16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria V Devices—*Preliminary* (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} *(1)* (mA)	I_{oh} *(1)* (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 x V_{CCIO}	0.8 x V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 x V_{CCIO}	0.8 x V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 x V_{CCIO}	0.9 x V_{CCIO}	—	—

Note to Table 16:

(1) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **SSTL15CI** specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the handbook.

Table 17. Differential SSTL I/O Standards for Arria V Devices —*Preliminary*

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.2	—	V_{CCIO}/2 + 0.2	0.62	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.15	—	V_{CCIO}/2 + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.125	—	V_{CCIO}/2 + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	–0.2	–0.15	—	0.15	2($V_{IH(AC)}$ – V_{REF})	2($V_{IL(AC)}$ – V_{REF})	—	V_{CCIO}/2	—
SSTL-135	1.283	1.35	1.45	0.18	–0.18	– 0.15	V_{CCIO}/2	0.15	2($V_{IH(AC)}$ – V_{REF})	2($V_{IL(AC)}$ – V_{REF})	—	V_{CCIO}/2	—
SSTL-125	1.19	1.25	1.31	0.18	–0.18	– 0.15	V_{CCIO}/2	0.15	2($V_{IH(AC)}$ – V_{REF})	2($V_{IL(AC)}$ – V_{REF})	—	V_{CCIO}/2	—

Table 18. Differential HSTL I/O Standards for Arria V Devices—*Preliminary*

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 x V_{CCIO}	—	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 x V_{CCIO} – 0.12	0.5 x V_{CCIO}	0.5 x V_{CCIO} +0.12	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}	0.44	0.44

Table 19. Differential I/O Standard Specifications for Arria V Devices—*Preliminary*

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) *(1)*			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	*(3)*														
2.5 V LVDS *(4)*	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	<700 Mbps	1.80	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	>700 Mbps	1.55						
RSDS (HIO) *(5)*	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) *(6)*	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4
LVPECL *(7)*	2.375	2.5	2.625	300	—	—	0.60	<700 Mbps	1.80	—	—	—	—	—	—
							1.00	>700 Mbps	1.60						

Notes to Table 19:

(1) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(2) RL range: $90 \leq RL \leq 110\ \Omega$

(3) Transmitter, receiver, and input reference clock pins of high-speed transceivers use the **PCML** I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 20 and Table 21.

(4) For optimized **LVDS** receiver performance, the receiver voltage input range must be within 1.0V to 1.6V for data rates above 700 Mbps and 0 V to 1.85 V for data rates below 700 Mbps.

(5) For optimized **RSDS** receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

(6) For optimized **Mini-LVDS** receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.

(7) For optimized **LVPECL** receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks for commercial grade devices.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 20 and Table 21 list the Arria V transceiver specifications.

Table 20. Transceiver Specifications for Arria V GX Devices (1)—*Preliminary* (Part 1 of 3)

Symbol/ Description	Conditions	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	**1.2 V PCML, 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL** (3), **HCSL**, and **LVDS**							
Input frequency from REFCLK input pins	—	27	—	710	27	—	710	MHz
Duty cycle	—	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	Not available for **HCSL** clock standard	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.1/1.5 (4)	—	—	1.1/1.5 (4)	—	V
V_{ICM} (DC coupled)	**HCSL** I/O standard for the PCIe reference clock	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (2)	10 Hz	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	dBc/Hz
	≥1 MHz	—	—	-130	—	—	-130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

Table 20. Transceiver Specifications for Arria V GX Devices (1)—*Preliminary* (Part 2 of 3)

Symbol/ Description	Conditions	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Transceiver Clocks								
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	125	75	—	125	MHz
Receiver								
Supported I/O Standards	**1.5 V PCML**, **2.5 V PCML**, **LVPECL**, and **LVDS**							
Data rate	—	611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin (5)	—	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins (6)	—	85	—	—	85	—	—	mV
V_{ICM} (AC coupled)	—	—	800	—	—	800	—	mV
V_{ICM} (DC coupled)	≤ 3.2 Gbps (7)	670	700	730	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	Ω
t_{LTR} (8)	—	—	—	10	—	—	10	µs
t_{LTD} (9)	—	4	—	—	4	—	—	µs
t_{LTD_manual} (10)	—	4	—	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (11)	—	15	—	—	15	—	—	µs
Programmable ppm detector (12)	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000						ppm
Run Length	—	—	—	200	—	—	200	UI
Programmable equalization (AC) and DC gain	—	Refer to Figure 1 and Figure 2						dB

Table 20. Transceiver Specifications for Arria V GX Devices (1)—*Preliminary* (Part 3 of 3)

Symbol/ Description	Conditions	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter								
Supported I/O standards	**1.5 V PCML**							
Data rate	—	611	—	6553.6	611	—	3125	Mbps
V_{OCM} (AC coupled)	—	—	650	—	—	650	—	mV
V_{OCM} (DC coupled)	≤ 3.2 Gbps (7)	670	700	730	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	Ω
Rise time (13)	—	30	—	160	30	—	160	ps
Fall time (13)	—	30	—	160	30	—	160	ps
CMU PLL								
Supported data range	—	611	—	6553.6	611	—	3125	Mbps
fPLL supported data range	—	611	—	3125	611	—	3125	Mbps
Transceiver-FPGA Fabric Interface								
Interface speed (single-width mode)	—	25	—	187.5	25	—	187.5	MHz
Interface speed (double-width mode)	—	25	—	163.84	25	—	163.84	MHz

Notes to Table 20:

(1) Speed grades shown in Table 20 refer to the Transceiver Speed Grade in the device ordering code. For more information about device ordering codes, refer to the *Arria V Device Overview*.

(2) The transmitter `REFCLK` phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) -12, equivalent to 14 sigma.

(3) Differential **LVPECL** signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(4) For data rate <=3.2 Gbps, connect $V_{CCR\_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR\_GXBL/R}$ to a 1.15-V power supply. For details, refer to the *Arria V Device Family Pin Connection Guidelines*.

(5) The device cannot tolerate prolonged operation at this absolute maximum.

(6) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(7) For standard protocol compliance, use AC coupling.

(8) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(9) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(10) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(11) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(12) The rate match FIFO supports only up to ±300 parts per million (ppm).

(13) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Table 21. Transceiver Specifications for Arria V GT Devices (1)—*Preliminary* (Part 1 of 3)

Symbol/ Description	Conditions	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Reference Clock					
Supported I/O Standards	**1.2 V PCML**, **1.4 V PCML**, **1.5 V PCML**, **2.5 V PCML**, **Differential LVPECL** (3), **HCSL**, and **LVDS**				
Input frequency from `REFCLK` input pins	—	27	—	710	MHz
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.2	—	V
V_{ICM} (DC coupled)	**HCSL** I/O standard for the PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (2)	10 Hz	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	dBc/Hz
	≥1 MHz	—	—	-130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	Ω
Transceiver Clocks					
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	125	MHz
Receiver					
Supported I/O Standards	**1.5 V PCML**, **2.5 V PCML**, **LVPECL**, and **LVDS**				
Data rate (6-Gbps Transceiver)	—	611	—	6553.6	Mbps
Data rate (10-Gbps transceiver)	—	0.611	—	10.3125	Gbps
Absolute V_{MAX} for a receiver pin (4)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	V

Table 21. Transceiver Specifications for Arria V GT Devices (1)—*Preliminary* (Part 2 of 3)

Symbol/ Description	Conditions	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Minimum differential eye opening at the receiver serial input pins (5)	—	85	—	—	mV
V_{ICM} (AC coupled)	—	—	800	—	mV
V_{ICM} (DC coupled)	$\leq$ 3.2 Gbps (6)	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	85			Ω
	100-Ω setting	100			Ω
	120-Ω setting	120			Ω
	150-Ω setting	150			Ω
t_{LTR} (7)	—	—	—	10	µs
t_{LTD} (8)	—	4	—	—	µs
t_{LTD_manual} (9)	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (10)	—	15	—	—	µs
Programmable ppm detector (11)	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000			ppm
Run Length	—	—	—	200	UI
Programmable equalization (AC) and DC gain	—	Refer to Figure 1 and Figure 2			
Transmitter					
Supported I/O Standards	**1.5 V PCML**				
Data rate (6-Gbps transceiver)	—	611	—	6553.6	Mbps
Data rate (10-Gbps transceiver)	—	0.611	—	10.3125	Gbps
V_{OCM} (AC coupled)	—	—	650	—	mV
V_{OCM} (DC coupled)	$\leq$3.2 Gbps (6)	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Rise time (12)	—	30	—	160	ps
Fall time (12)	—	30	—	160	ps
CMU PLL					
Supported data range	—	0.611	—	10.3125	Gbps
fPLL supported data range	—	611	—	3125	Mbps

Table 21. Transceiver Specifications for Arria V GT Devices (1)—*Preliminary* (Part 3 of 3)

Symbol/ Description	Conditions	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transceiver-FPGA Fabric Interface					
Interface speed (PMA direct mode)	—	50	—	161.13	MHz
Interface speed (single-width mode)	—	25	—	187.5	MHz
Interface speed (double-width mode)	—	25	—	163.84	MHz

Notes to Table 21:

(1) Speed grades shown in Table 21 refer to the Transceiver Speed Grade in the device ordering code. For more information about device ordering codes, refer to the *Arria V Device Overview*.

(2) The transmitter `REFCLK` phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) -12, equivalent to 14 sigma.

(3) Differential **LVPECL** signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(4) The device cannot tolerate prolonged operation at this absolute maximum.

(5) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(6) For standard protocol compliance, use AC coupling.

(7) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(8) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(9) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(10) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(11) The rate match FIFO supports only up to ±300 ppm.

(12) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Figure 1 shows the continuous time-linear equalizer (CTLE) response for Arria V devices with data rates > 3.25 Gbps.

Figure 1. CTLE Response for Arria V Devices with Data Rates > 3.25 Gbps

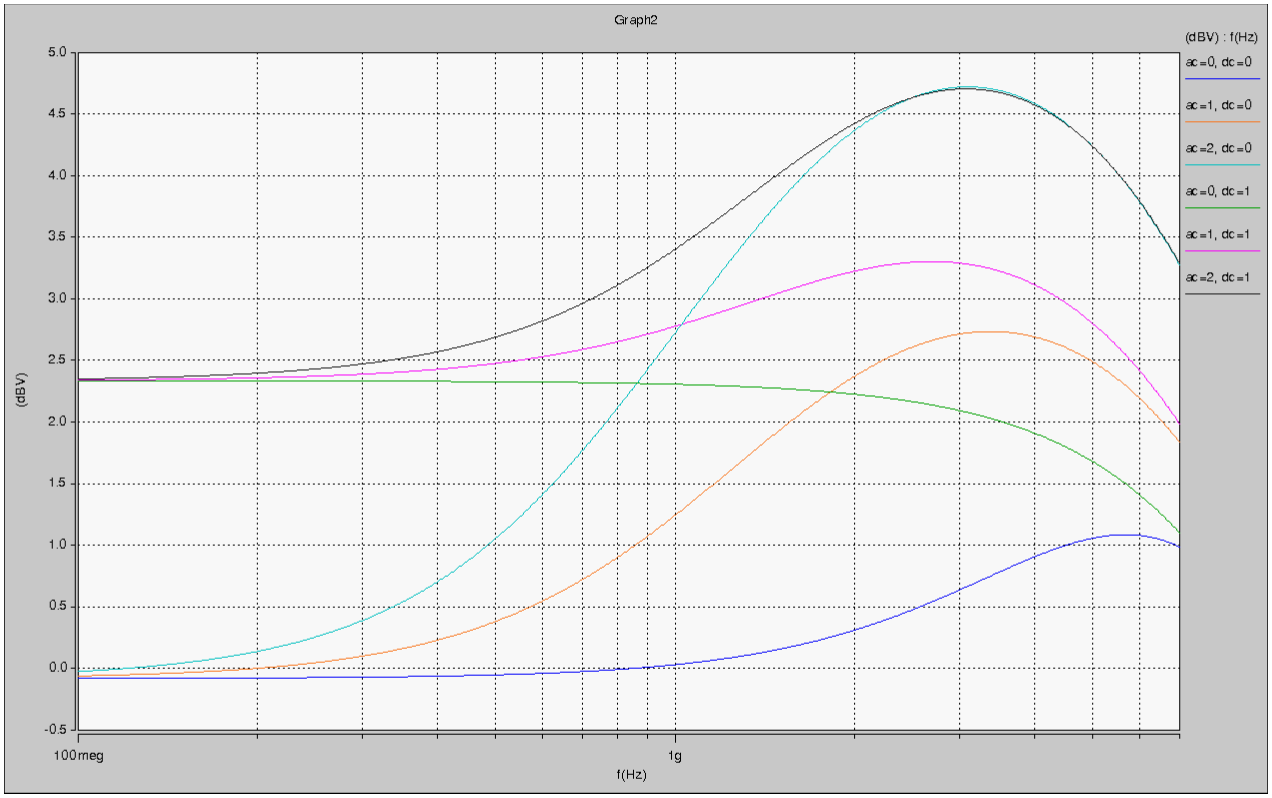


Figure 2 shows the CTLE response for Arria V devices with data rates ≤3.25 Gbps.

Figure 2. CTLE Response for Arria V Devices with Data Rates ≤3.25 Gbps

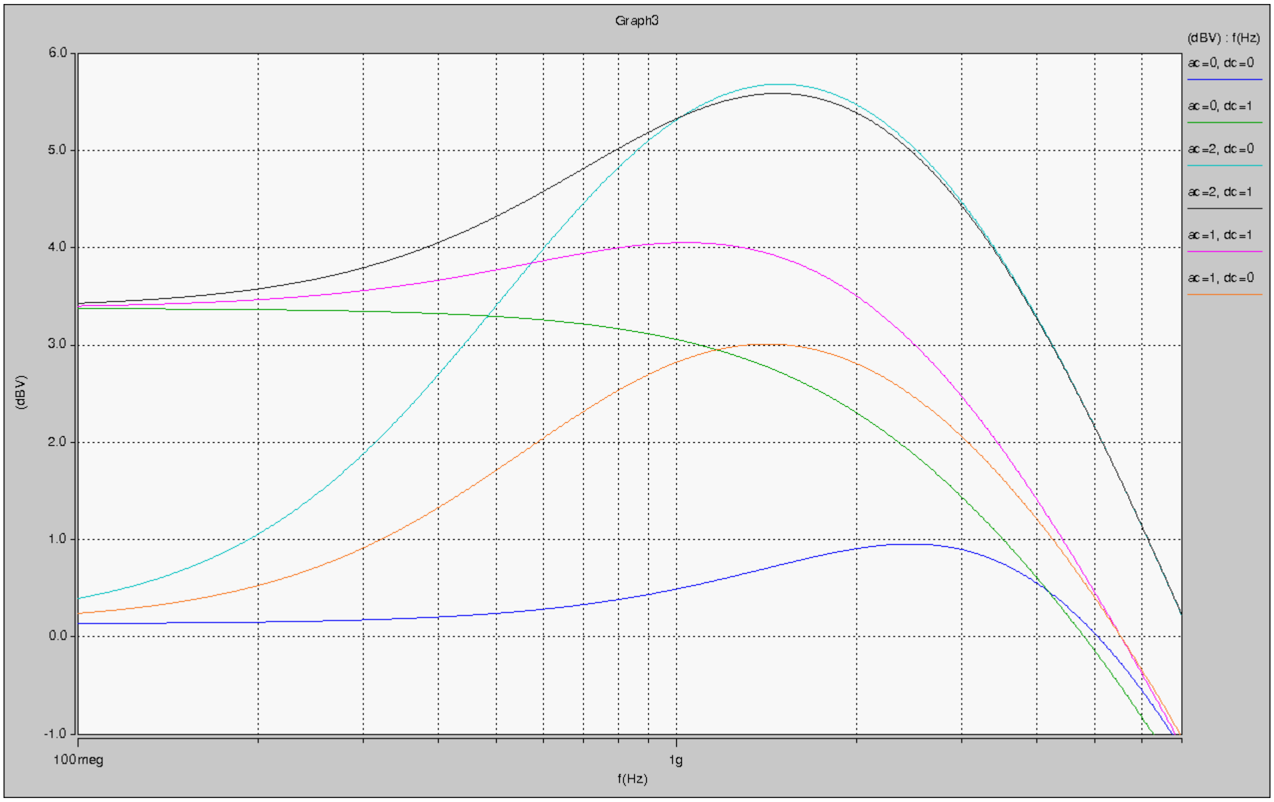


Table 22 lists the TX V_{OD} settings for Arria V transceiver channels.

Table 22. Typical TX V_{OD} Setting for Arria V Transceiver Channels = 100 Ω—*Preliminary*

Symbol	V_{OD} Setting (1)	V_{OD} Value (mV)	V_{OD} Setting (1)	V_{OD} Value (mV)
V_{OD} differential peak to peak typical	0	0	32	640
	1	20	33	660
	2	40	34	680
	3	60	35	700
	4	80	36	720
	5	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Note to Table 22:

(1) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

Table 23 lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- low-frequency data pattern—five 1s and five 0s
- data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

Table 23. Transmitter Pre-Emphasis Levels for Arria V Devices (1), (2), (3), (4)—*Preliminary* (Part 1 of 2)

Quartus II 1st Post Tap Pre-Emphasis Setting	Quartus II V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	—	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	—	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	—	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	—	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	—	7.92	4.86	4	3.38	2.87	2.46	dB
10	—	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB

Table 23. Transmitter Pre-Emphasis Levels for Arria V Devices (1), (2), (3), (4)—*Preliminary* (Part 2 of 2)

Quartus II 1st Post Tap Pre-Emphasis Setting	Quartus II V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Notes to Table 23:

(1) The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$
$|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$
$|C|$ = 1st post tap pre-emphasis setting

(2) $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.

(3) $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

(4) For example, when V_{OD} = 800 mV, the corresponding V_{OD} value setting is 40.
To check the validity of the 1st post tap pre-emphasis setting = 2
$|B| + |C| \leq 60 \longrightarrow 40 + 2 = 42$
$|B| - |C| > 5 \longrightarrow 40 - 2 = 38$
$(V_{MAX}/V_{MIN} - 1)\% < 600\% \longrightarrow (42/38 - 1)\% = 10.52\%$
Therefore, the 1st post tap pre-emphasis setting = 2 is a valid condition.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks and temperature sensing diode specifications.

Clock Tree Specifications

Table 24 lists the clock tree specifications for Arria V devices.

Table 24. Clock Tree Performance for Arria V Devices—*Preliminary*

Performance				Unit
Symbol	–I3, –C4 Speed Grade	–I5, –C5 Speed Grade	–C6 Speed Grade	
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 25 lists the Arria V PLL specifications when operating in both the commercial junction temperature range (0° C to 85° C for –C4, –C5, and –C6) and the industrial junction temperature range(0° C to 100° C for –I3 and -40° C to 100° C for –I5).

Table 25. PLL Specifications for Arria V Devices (1)—*Preliminary* (Part 1 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–3 speed grade)	5	—	670 (2)	MHz
	Input clock frequency (–4 speed grade)	5	—	670 (2)	MHz
	Input clock frequency (–5 speed grade)	5	—	622 (2)	MHz
	Input clock frequency (–6 speed grade)	5	—	500 (2)	MHz
f_{INPFD}	Integer input clock frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional input clock frequency to the PFD	50	—	TBD (1)	MHz
f_{VCO} (3)	PLL VCO operating range (–3 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–4 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–5 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–6 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (–4 speed grade)	—	—	500 (4)	MHz
	Output frequency for internal global or regional clock (–5 speed grade)	—	—	500 (4)	MHz
	Output frequency for internal global or regional clock (–6 speed grade)	—	—	400 (4)	MHz
f_{OUT_EXT}	Output frequency for external clock output (–3 speed grade)	—	—	670 (4)	MHz
	Output frequency for external clock output (–4 speed grade)	—	—	670 (4)	MHz
	Output frequency for external clock output (–5 speed grade)	—	—	622 (4)	MHz
	Output frequency for external clock output (–6 speed grade)	—	—	500 (4)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns

Table 25. PLL Specifications for Arria V Devices (1)—*Preliminary* (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{DYCONFIGCLK}$	Dynamic Configuration Clock	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (9)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} (5), (6)	Input clock cycle-to-cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} (7)	Period jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTCCJ_DC} (7)	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTPJ_IO} (7), (10)	Period Jitter for clock output on the regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period Jitter for clock output on the regular I/O ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTCCJ_IO} (7), (10)	Cycle-to-cycle jitter for clock output on the regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Cycle-to-cycle jitter for clock output on the regular I/O ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
$t_{OUTPJ\_DC\_F}$	Period jitter for dedicated clock output in fractional mode	—	—	TBD (1)	—
$t_{OUTCCJ\_DC\_F}$	Cycle-to-cycle jitter for dedicated clock output in fractional mode	—	—	TBD (1)	—
$t_{OUTPJ\_IO\_F}$	Period Jitter for clock output on the regular I/O in fractional mode	—	—	TBD (1)	—
$t_{OUTCCJ\_IO\_F}$	Cycle-to-cycle jitter for clock output on the regular I/O in fractional mode	—	—	TBD (1)	—
$t_{CASC\_OUTPJ\_DC}$ (7), (8)	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	24	—	bits
k_{VALUE}	Numerator of Fraction	TBD (1)	8388608	TBD (1)	—

Table 25. PLL Specifications for Arria V Devices (1)—*Preliminary* (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{RES}	Resolution of VCO frequency (f_{INPFD} =100 MHz)	—	5.96	—	Hz

Notes to Table 25:

(1) Pending silicon characterization.

(2) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(3) The voltage-controlled oscillator (VCO) frequency reported by the Quartus II software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(4) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

(5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(6) F_{REF} is fIN/N when N = 1.

(7) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 34 on page 1–36.

(8) The cascaded PLL specification is only applicable with the following conditions:
a. Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(9) High bandwidth PLL settings are not supported in external feedback mode.

(10) External memory interface clock output jitter specifications use a different measurement method, which are available in Table 34 on page 1–36.

DSP Block Specifications

Table 26 lists the Arria V DSP block performance specifications.

Table 26. DSP Block Performance Specifications for Arria V Devices—*Preliminary*

Mode	Performance			Unit
	–I3, –C4	–I5, –C5	–C6	
Modes using One DSP Block				
Independent 9 x 9 Multiplication	370	310	220	MHz
Independent 18 x 19 Multiplication	370	310	220	MHz
Independent 18 x 25 Multiplication	370	310	220	MHz
Independent 20 x 24 Multiplication	370	310	220	MHz
Independent 27 x 27 Multiplication	310	250	200	MHz
Two 18 x 19 Multiplier Adder Mode	370	310	220	MHz
18 x 18 Multiplier Added Summed with 36-bit Input	370	310	220	MHz
Modes using Two DSP Blocks				
Complex 18 x 19 multiplication	370	310	220	MHz

Memory Block Specifications

Table 27 lists the Arria V memory block specifications.

Table 27. Memory Block Performance Specifications for Arria V Devices (1), (2)—*Preliminary*

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–I3, –C4	–I5, –C5	–C6	
MLAB	Single port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz
	ROM, all supported width	—	—	500	450	400	MHz
M10K Block	Single-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	315	275	240	MHz
	True dual port, all supported widths	0	1	400	350	285	MHz
	ROM, all supported widths	0	1	400	350	285	MHz
	Min Pulse Width (clock high time)	—	—	1,275	1,360	1,445	ps
	Min Pulse Width (clock low time)	—	—	850	1,060	1,175	ps

Notes to Table 27:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Temperature Sensing Diode Specifications

Table 28 lists the specifications for the Arria V internal temperature sensing diode.

Table 28. Internal Temperature Sensing Diode Specifications for Arria V Devices—*Preliminary*

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40 to 100°C	±8°C	No	Frequency: 1 MHz	< 100 ms	8 bits	8 bits

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 29 lists high-speed I/O timing for Arria V devices.

Table 29. High-Speed I/O Specifications for Arria V Devices (1), (2), (3)—*Preliminary* (Part 1 of 3)

Symbol	Conditions	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (6)	5	—	625	5	—	625	5	—	TBD	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (4)	Clock boost factor W = 1 to 40 (6)	5	—	625	5	—	625	5	—	TBD	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (5)	Clock boost factor W = 1 to 40 (6)	5	—	420	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	625 (7)	5	—	625 (7)	5	—	TBD (7)	MHz
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 (8)	(9)	—	1250	(9)	—	1250	(9)	—	1050	Mbps
	SERDES factor J ≥ 8 (8), (10) LVDS TX with RX DPA	(9)	—	1600 (11)	(9)	—	1500 (11)	(9)	—	1250 (11)	Mbps
	SERDES factor J = 1 to 2 Uses DDR Registers	(9)	—	(12)	(9)	—	(12)	(9)	—	(12)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate) (13)	SERDES factor J = 4 to 10	(9)	—	945	(9)	—	945	(9)	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate) (13)	SERDES factor J = 4 to 10	(9)	—	200	(9)	—	TBD	(9)	—	TBD	Mbps

Table 29. High-Speed I/O Specifications for Arria V Devices (1), (2), (3)—*Preliminary* (Part 2 of 3)

Symbol	Conditions	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate, 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate, < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate, 600 Mbps – 1.25 Gbps	—	—	TBD	—	—	TBD	—	—	TBD	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	TBD	—	—	TBD	—	—	TBD	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with One External Output Resistor Network	—	—	—	TBD	—	—	TBD	—	—	TBD	ps
t_{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards (14)	—	—	160	—	—	180	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Network	—	—	250	—	—	250	—	—	300	ps
	Emulated Differential I/O Standards with One External Output Resistor Network	—	—	TBD	—	—	TBD	—	—	TBD	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver											
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 (8)	—	—	1250	—	—	1250	—	—	1050	Mbps
	SERDES factor J ≥ 8 with DPA (8), (10), (11)	—	—	1600	—	—	1500	—	—	1250	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(9)	—	(15)	(9)	—	(15)	(9)	—	(15)	Mbps
	SERDES factor J = 1 to 2 Uses DDR Registers	(9)	—	(12)	(9)	—	(12)	(9)	—	(12)	Mbps
DPA Mode											
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode											
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	± ppm

Table 29. High-Speed I/O Specifications for Arria V Devices (1), (2), (3)—*Preliminary* (Part 3 of 3)

Symbol	Conditions	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Non DPA Mode											
Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

Notes to Table 29:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) For LVDS applications, you must use the PLLs in integer PLL mode.

(4) This applies to DPA and soft-CDR modes only.

(5) This applies to LVDS source synchronous mode only.

(6) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

(7) This is achieved by using the LVDS clock network.

(8) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(9) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(10) The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.

(11) Pending silicon characterization.

(12) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.

(13) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

(14) This applies to default pre-emphasis and V_{OD} settings only.

(15) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Figure 3 shows the DPA lock time specifications with the DPA PLL calibration option enabled.

Figure 3. DPA Lock Time Specification with DPA PLL Calibration Enabled

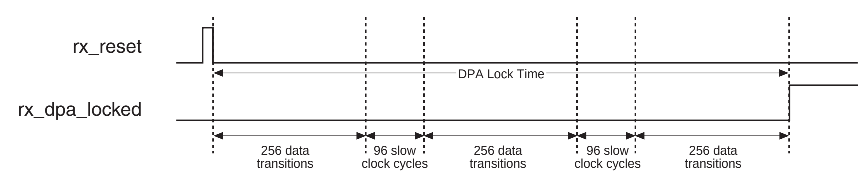


Table 30 lists the DPA lock time specifications for Arria V devices.

Table 30. DPA Lock Time Specifications for Arria V Devices (1), (2), (3)—*Preliminary*

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (4)	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 30:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grades.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 4 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.25 Gbps.

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

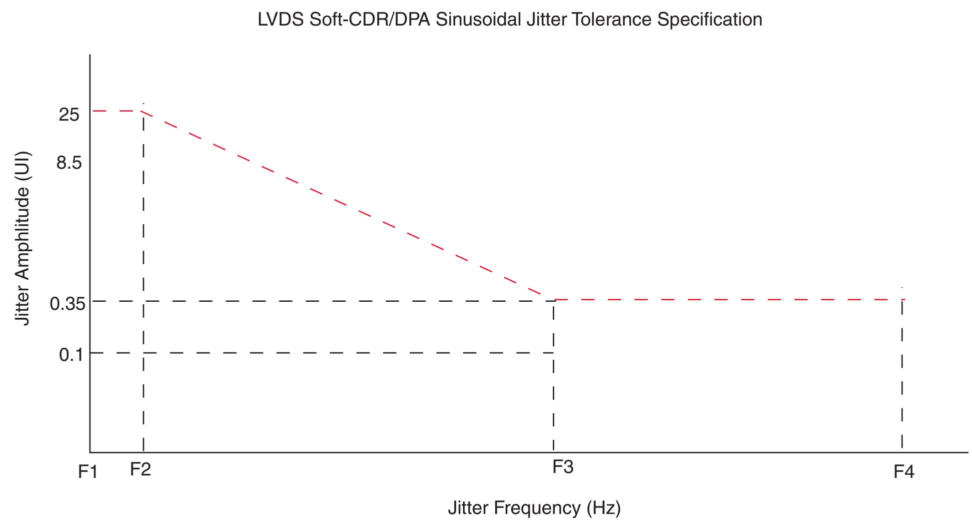


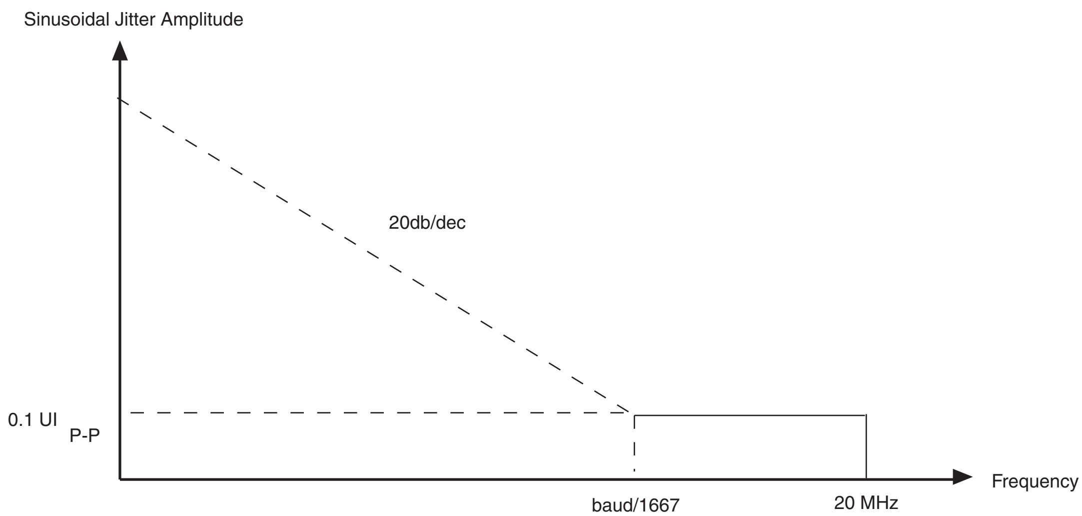
Table 31 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.25 Gbps.

Table 31. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps—*Preliminary*

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 5 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate less than 1.25 Gbps.

Figure 5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 32 lists the DLL frequency range specifications for Arria V devices.

Table 32. DLL Frequency Range Specifications for Arria V Devices

Parameter	–I3, –C4	–I5, –C5	–C6	Unit
DLL operating frequency range	200 – 667	200 – 667	200 – 667	MHz

Table 33 lists the DQS phase shift error for Arria V devices.

Table 33. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V Devices *(1)*

Number of DQS Delay Buffer	–I3, –C4	–I5, –C5	–C6	Unit
2	40	80	80	ps

Note to Table 33:

(1) This error specification is the absolute maximum and minimum error.

Table 34 lists the memory output clock jitter specifications for Arria V devices.

Table 34. Memory Output Clock Jitter Specification for Arria V Devices *(1), (2), (3)*

Parameter	Clock Network	Symbol	–I3, –C4		–I5, –C5		–C6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	–41	41	–50	50	–55	55	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	63		90		94		ps

Notes to Table 34:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

(2) Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

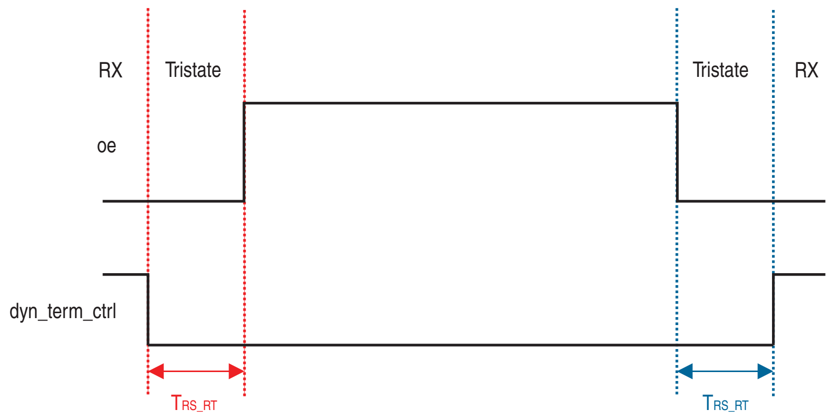
Table 35 lists the OCT calibration block specifications for Arria V devices.

Table 35. OCT Calibration Block Specifications for Arria V Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 6 shows the T_{RS_RT} for `dyn_term_ctrl` and `oe` signals.

Figure 6. Timing Diagram for dyn_term_ctrl and oe Signals



Duty Cycle Distortion (DCD) Specifications

Table 36 lists the worst-case DCD for Arria V devices.

Table 36. Worst-Case DCD on Arria V I/O Pins—*Preliminary*

Symbol	–I3, –C4		–C5,–I5		–C6		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Note to Table 36:

(1) The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

The data in Table 37 through Table 49 is preliminary and pending silicon characterization.

QSPI Timing Characteristics

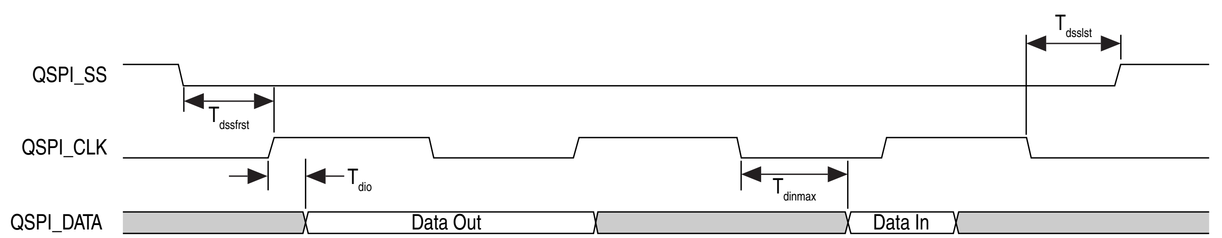
Table 37 lists the queued serial peripheral interface (QSPI) timing characteristics for Arria V devices.

Table 37. QSPI Timing Requirements for Arria V Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	CLK clock period	TBD	10	TBD	ns
$T_{dutycycle}$	QSPI_CLK duty cycle	TBD	—	TBD	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	8	—	TBD	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	8	—	TBD	ns
T_{dio}	IO Data output delay	–1	—	1	ns
T_{dinmax}	Maximum data input delay from falling edge of QSPI_CLK to data arrival at SoC	—	—	20	ns

Figure 7 shows the timing diagram for QSPI timing characteristics.

Figure 7. QSPI Timing Diagram



SPI Timing Characteristics

Table 38 lists the serial peripheral interface (SPI) master timing characteristics for Arria V devices.

Table 38. SPI Master Timing Requirements for Arria V Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	CLK clock period	TBD	16.667	TBD	ns
$T_{dutycycle}$	SPI_CLK duty cycle	TBD	—	TBD	%
$T_{dssfrst}$	Output delay SPI_SS valid before first clock edge	8	—	TBD	ns
T_{dsslst}	Output delay SPI_SS valid after last clock edge	8	—	TBD	ns
T_{dio}	Master-out slave-in (MOSI) output delay	–1	—	1	ns
T_{dinmax}	Maximum data input delay from falling edge of SPI_CLK to data arrival at SoC	—	—	500	ns

Figure 8 shows the timing diagram for SPI master timing characteristics.

Figure 8. SPI Master Timing Diagram

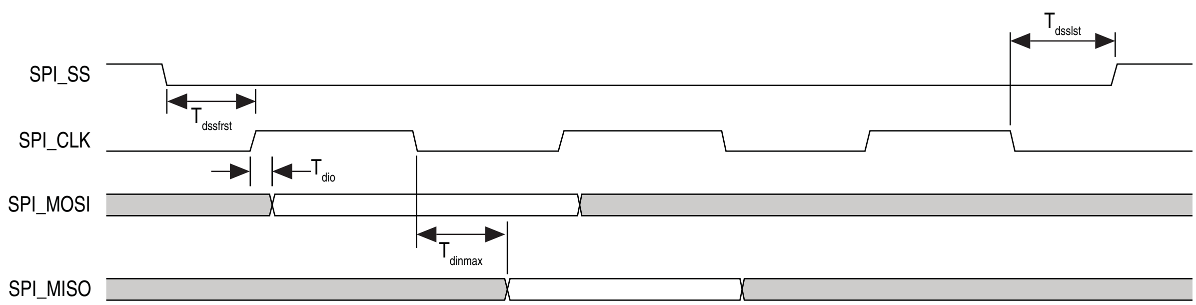


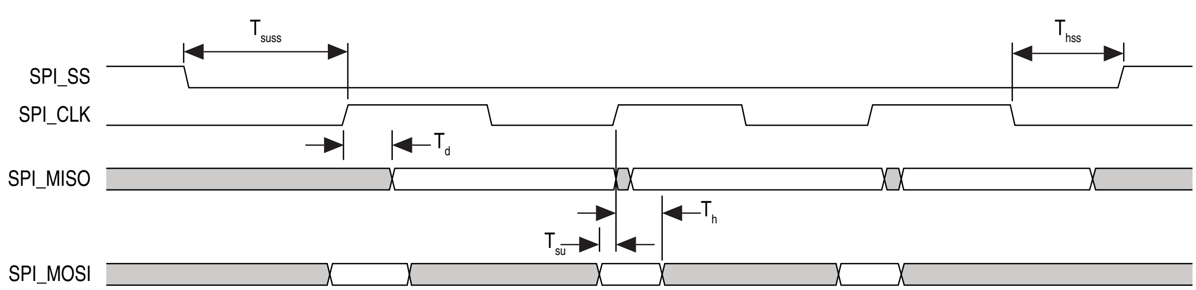
Table 39 lists the SPI slave timing characteristics for Arria V devices.

Table 39. SPI Slave Timing Requirements for Arria V Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	CLK clock period	TBD	16.67	TBD	ns
T_s	MOSI Setup time	5	—	TBD	ns
T_h	MOSI Hold time	7	—	TBD	ns
T_{suss}	Setup time SPI_SS valid before first clock edge	8	—	TBD	ns
T_{hss}	Hold time SPI_SS valid after last clock edge	8	—	TBD	ns
T_d	Master-in slave-out (MISO) output delay	TBD	—	16	ns

Figure 9 shows the timing diagram for SPI slave timing characteristics.

Figure 9. SPI Slave Timing Diagram



SD/MMC Timing Characteristics

Table 40 lists the secure digital (SD)/MultiMediaCard (MMC) timing characteristics for Arria V devices.

Table 40. SD/MMC Timing Requirements for Arria V Devices—*Preliminary* (Part 1 of 2)

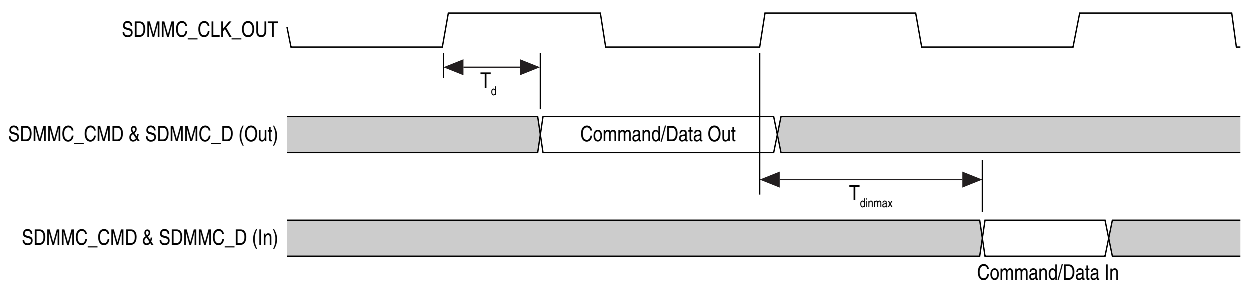
Symbol	Description	Min	Max	Unit
T_{clk}	SDMMC_CLK_OUT clock period	20	TBD	ns
$T_{dutycycle}$	SDMMC_CLK_OUT duty cycle	TBD	TBD	%

Table 40. SD/MMC Timing Requirements for Arria V Devices—*Preliminary* (Part 2 of 2)

Symbol	Description	Min	Max	Unit
T_d	SDMMC_CMD/SDMMC_D output delay	TBD	6	ns
T_{dinmax}	Maximum input delay from rising edge of SDMMC_CLK to data arrival at SoC	—	25	ns

Figure 10 shows the timing diagram for SD/MMC timing characteristics.

Figure 10. SD/MMC Timing Diagram



USB Timing Characteristics

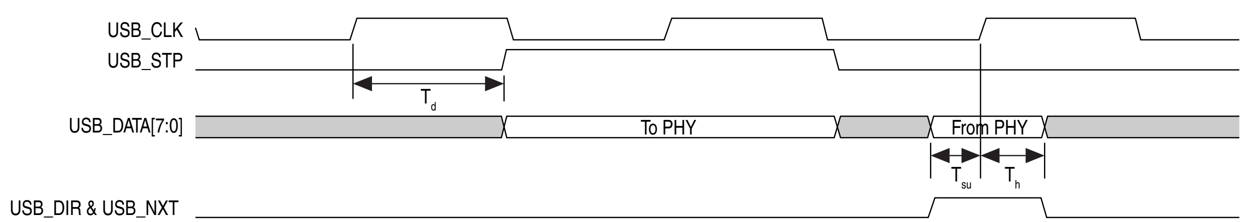
Table 41 lists the USB timing characteristics for Arria V devices.

Table 41. USB Timing Requirements for Arria V Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB CLK clock period	TBD	16.67	TBD	ns
T_d	CLK to USB_STP/USB_DATA[7:0] output delay	TBD	—	8	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	TBD	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1.5	—	TBD	ns

Figure 11 shows the timing diagram for USB timing characteristics.

Figure 11. USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 42 lists the reduced gigabit media independent interface (RGMII) TX timing characteristics for Arria V devices.

Table 42. RGMII TX Timing Requirements for Arria V Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	TBD	8	TBD	ns
T_{clk} (100Base-T)	TX_CLK clock period	TBD	40	TBD	ns
T_{clk} (10Base-T)	TX_CLK clock period	TBD	400	TBD	ns
$T_{dutycycle}$	TX_CLK duty cycle	TBD	—	TBD	%
T_d	TX_CLK to TXD/TX_CTL output data delay	–0.5	—	0.5	ns

Figure 12 shows the timing diagram for RGMII TX timing characteristics.

Figure 12. RGMII TX Timing Diagram

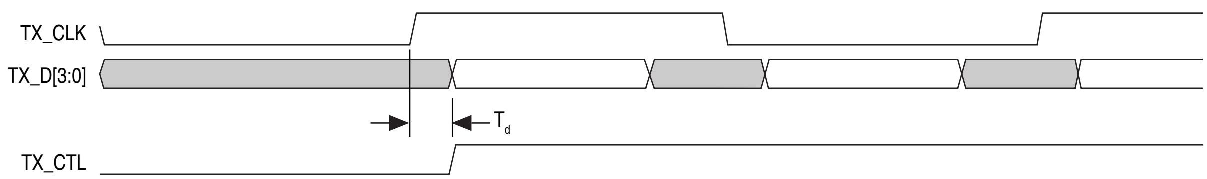


Table 43 lists the RGMII RX timing characteristics for Arria V devices.

Table 43. RGMII RX Timing Requirements for Arria V Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	TBD	8	TBD	ns
T_{clk} (100Base-T)	RX_CLK clock period	TBD	40	TBD	ns
T_{clk} (10Base-T)	RX_CLK clock period	TBD	400	TBD	ns
T_{su}	RX_D/RX_CTL setup time	1	—	TBD	ns
T_h	RX_D/RX_CTL hold time	1	—	TBD	ns

Figure 13 shows the timing diagram for RGMII RX timing characteristics.

Figure 13. RGMII RX Timing Diagram

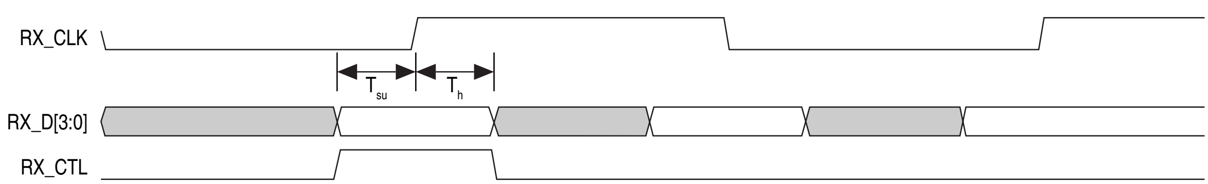


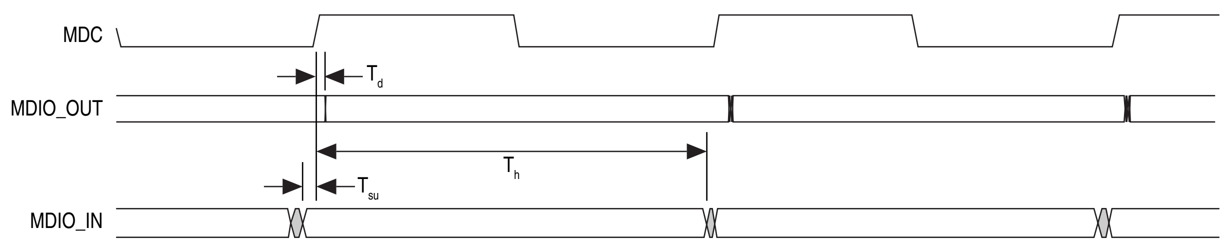
Table 44 lists the management data input/output (MDIO) timing characteristics for Arria V devices.

Table 44. MDIO Timing Requirements for Arria V Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	TBD	400	TBD	ns
T_d	MDC to MDIO output data delay	10	—	TBD	ns
T_s	Setup time for MDIO data	10	—	TBD	ns
T_h	Hold time for MDIO data	10	—	TBD	ns

Figure 14 shows the timing diagram for MDIO timing characteristics.

Figure 14. MDIO Timing Diagram



I²C Timing Characteristics

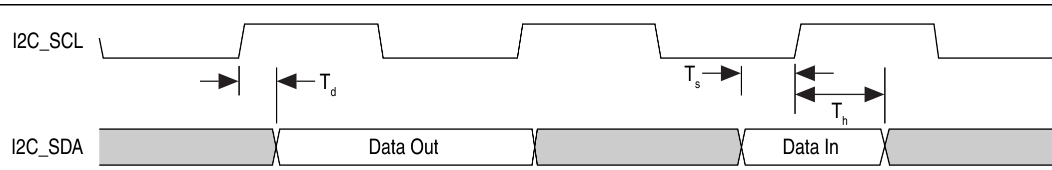
Table 45 lists the I²C timing characteristics for Arria V devices.

Table 45. I²C Timing Requirements for Arria V Devices—*Preliminary*

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	TBD	10	TBD	2.5	µs
$T_{clkhigh}$	SCL high time	4	TBD	0.6	TBD	µs
T_{clklow}	SCL low time	4.7	TBD	1.3	TBD	µs
T_s	Setup time for serial data line (SDA) data to SCL	250	TBD	100	TBD	ns
T_h	Hold time for SCL to SDA data	TBD	3.45	TBD	0.9	µs
T_d	SCL to SDA output data delay	8	TBD	8	TBD	ns

Figure 15 shows the timing diagram for MDIO timing characteristics.

Figure 15. I²C Timing Diagram



NAND Timing Characteristics

Table 46 lists the NAND timing characteristics for Arria V devices.

Table 46. NAND Timing Requirements for Arria V Devices—*Preliminary*

Symbol	Description	Min	Max	Unit
T_{wp}	Write enable pulse width	10	TBD	ns
T_{wh}	Write enable hold time	7	TBD	ns
T_{rp}	Read Enable pulse width	10	TBD	ns
T_{reh}	Read enable holdtime	7	TBD	ns
T_{clesu}	Command latch enable to write enable setup time	10	TBD	ns
T_{cleh}	Command latch enable to write enable hold time	5	TBD	ns
T_{cesu}	Chip enable to write enable setup time	15	TBD	ns
T_{ceh}	Chip enable to write enable hold time	5	TBD	ns
T_{alesu}	Address latch enable to write enable setup time	10	TBD	ns
T_{aleh}	Address latch enable to write enable hold time	5	TBD	ns
T_{dsu}	Data to write enable setup time	10	TBD	ns
T_{dh}	Data to write enable hold time	5	TBD	ns
T_{drb}	Write enable high to ready/busy low	TBD	100	ns
T_{cea}	Chip enable to data access time	TBD	25	ns
T_{rea}	Read enable to data access time	TBD	16	ns
T_{rhz}	Read enable to data high impedance	TBD	100	ns
T_{rb}	Ready to read enable low	20	TBD	ns

Figure 16 shows the timing diagram for NAND command latch timing characteristics.

Figure 16. NAND Command Latch Timing Diagram

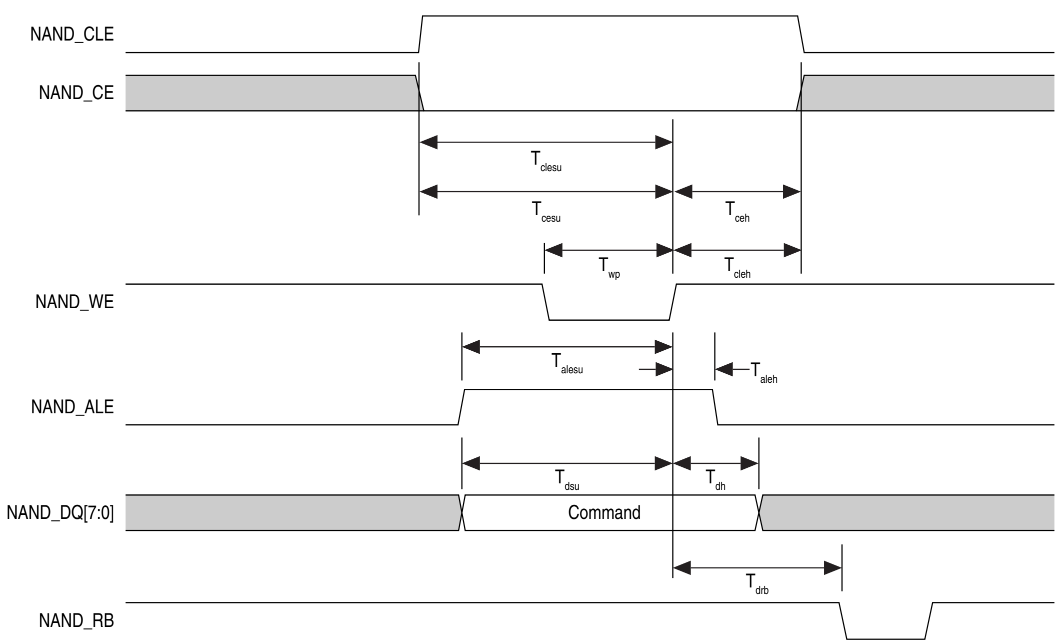


Figure 17 shows the timing diagram for NAND address latch timing characteristics.

Figure 17. NAND Address Latch Timing Diagram

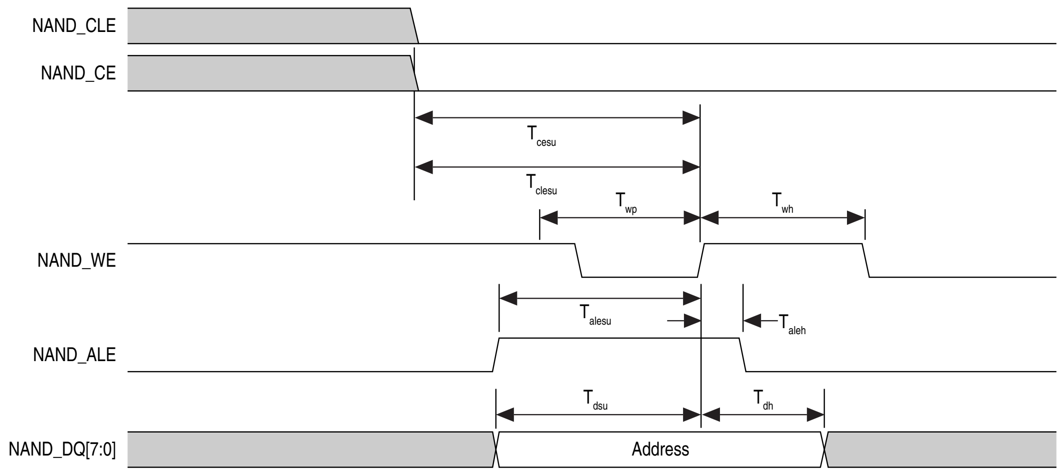


Figure 18 shows the timing diagram for NAND data write timing characteristics.

Figure 18. NAND Data Write Timing Diagram

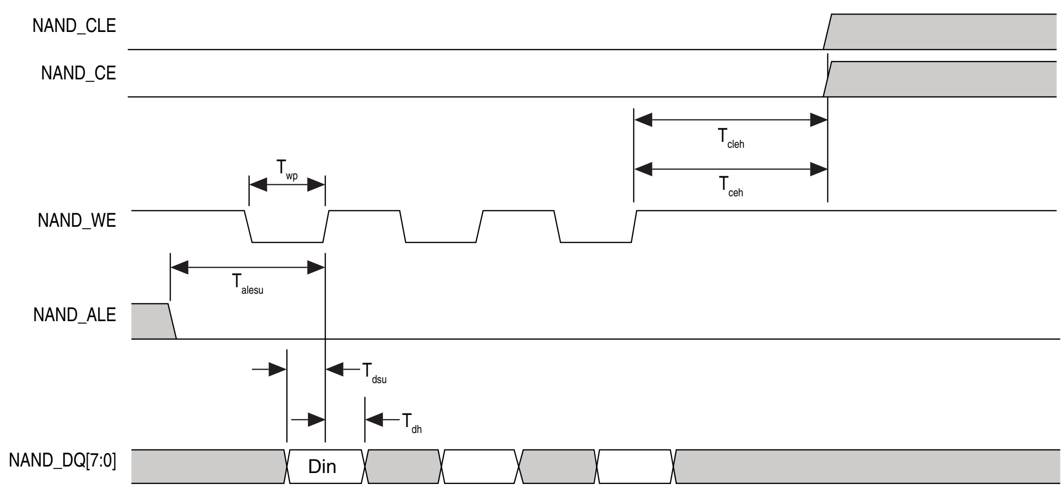
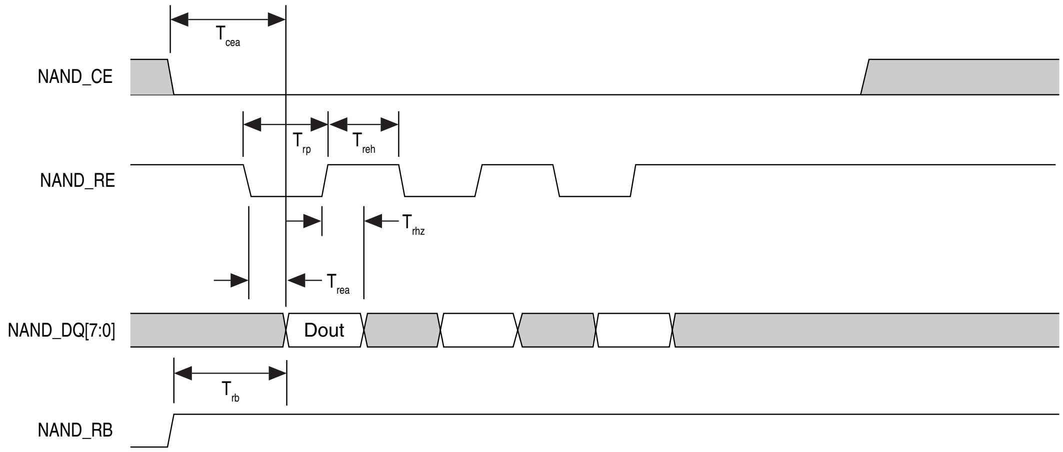


Figure 19 shows the timing diagram for NAND data read timing characteristics.

Figure 19. NAND Data Read Timing Diagram



ARM Trace Timing Characteristics

Table 47 lists the ARM trace timing characteristics for Arria V devices.

Table 47. ARM Trace Timing Requirements for Arria V Devices—*Preliminary*

Description	Min	Typ	Max	Unit
CLK clock period	TBD	8	TBD	ns
CLK maximum duty cycle	TBD	—	TBD	%
CLK to D0 –D7 output data delay	–1	—	1	ns

UART Interface

Table 48 lists the UART baud rate for Arria V devices.

Table 48. UART Baud Rate for Arria V Devices—*Preliminary*

Description	Max	Unit
Maximum baud rate	6.25M	symbols/second

GPIO Interface

Table 49 lists the general-purpose I/O (GPIO) pulse width for Arria V devices.

Table 49. GPIO Pulse Width for Arria V Devices—*Preliminary*

Description	Min	Max	Unit
Minimum detectable pulse width	40	TBD	ns

Configuration Specification

This section provides configuration specifications and timing for Arria V devices.

POR Specifications

Table 50 lists the specifications for fast and standard POR for Arria V devices.

Table 50. Fast and Standard POR Delay Specification for Arria V Devices *(1)*

POR Delay	Minimum (ms)	Maximum (ms)
Fast	4	12 *(2)*
Standard	100	300

Notes to Table 50:

(1) Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria V Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(2) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

JTAG Configuration Timing

Table 51 lists the JTAG timing parameters and values for Arria V devices.

Table 51. JTAG Timing Parameters and Values for Arria V Devices—*Preliminary*

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCP}	TCK clock period	167 *(1)*	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12 *(2)*	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 *(2)*	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 *(2)*	ns

Notes to Table 51:

(1) The minimum TCK clock period is 167 nS if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

(2) A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

FPP Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Arria V devices.

DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Table 52 lists the DCLK-to-DATA[] ratio for each combination.

Table 52. DCLK-to-DATA[] Ratio for Arria V Devices (1)

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4

Note to Table 52:

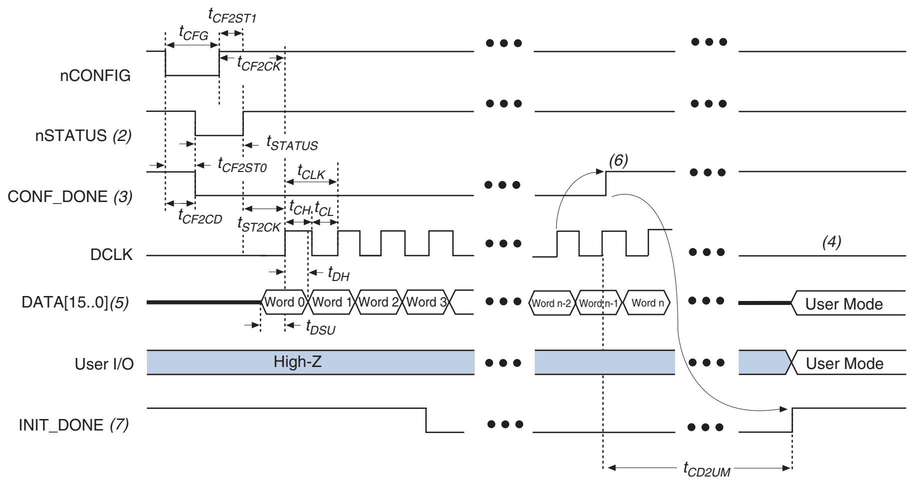
(1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP x16 where the r is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 20 shows the timing waveform for a FPP configuration when using a MAX® II device as an external host. This timing waveform shows timing when the DCLK-to-DATA[] ratio is 1.

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP x8 and FPP x16. For the respective DCLK-to-DATA[] ratio, refer to Table 52.

Figure 20. DCLK-to-DATA[] FPP Configuration Timing Waveform When the Ratio is 1 *(1)*



Notes to Figure 20:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power up, the Arria V device holds nSTATUS low for the time of the POR delay.

(3) After power up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) For FPP x16, use DATA[15..0]. For FPP x8, use DATA[7..0]. DATA[15..5] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

(6) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high when the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for Arria V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 53. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is 1 (1)—*Preliminary*

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 (2)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (3)	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP x8/ x16)	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (4)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 53:

(1) Use these timing parameters when the DCLK-to-DATA[] ratio is 1. To find the DCLK-to-DATA[] ratio for your system, refer Table 52 on page 1–47.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

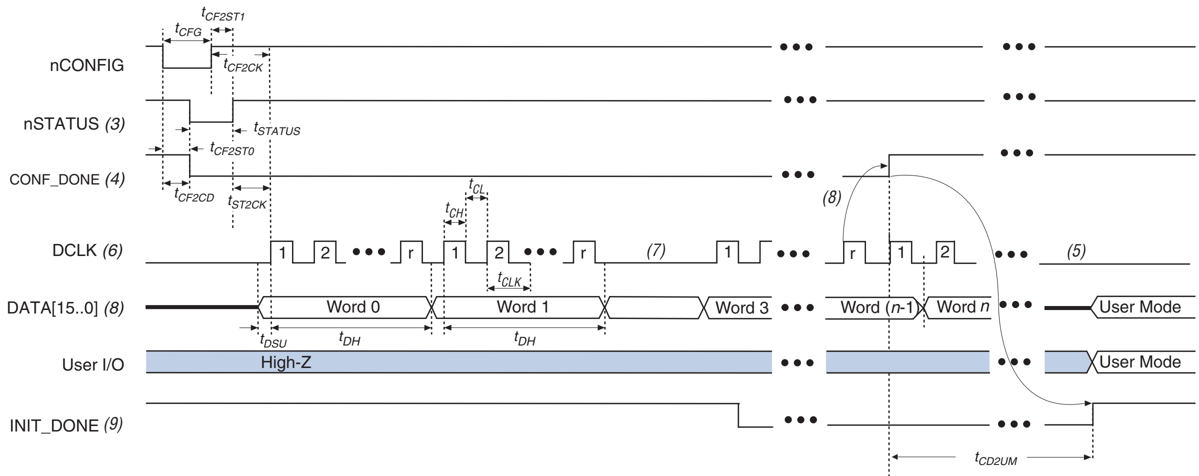
(3) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 21 shows the timing waveform for a FPP configuration when using a MAX II device or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is more than 1.

Figure 21. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 *(1), (2)*



Notes to Figure 21:

(1) To find the DCLK-to-DATA[] ratio for your system, refer Table 52 on page 1–47.

(2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(3) After power up, the Arria V device holds nSTATUS low for the time as specified by the POR delay.

(4) After power up, before and during configuration, CONF_DONE is low.

(5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 52 on page 1–47.

(7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[15..0] pins prior to sending the first DCLK rising edge.

(8) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high after the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 54 lists the timing parameters for Arria V devices when the DCLK-to-DATA[] ratio is more than 1.

Table 54. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is >1 (1)—*Preliminary*

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 (2)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (3)	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$ (4)	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP x8/ x16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (5)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 54:

(1) Use these timing parameters when you use decompression and the design security features.

(2) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

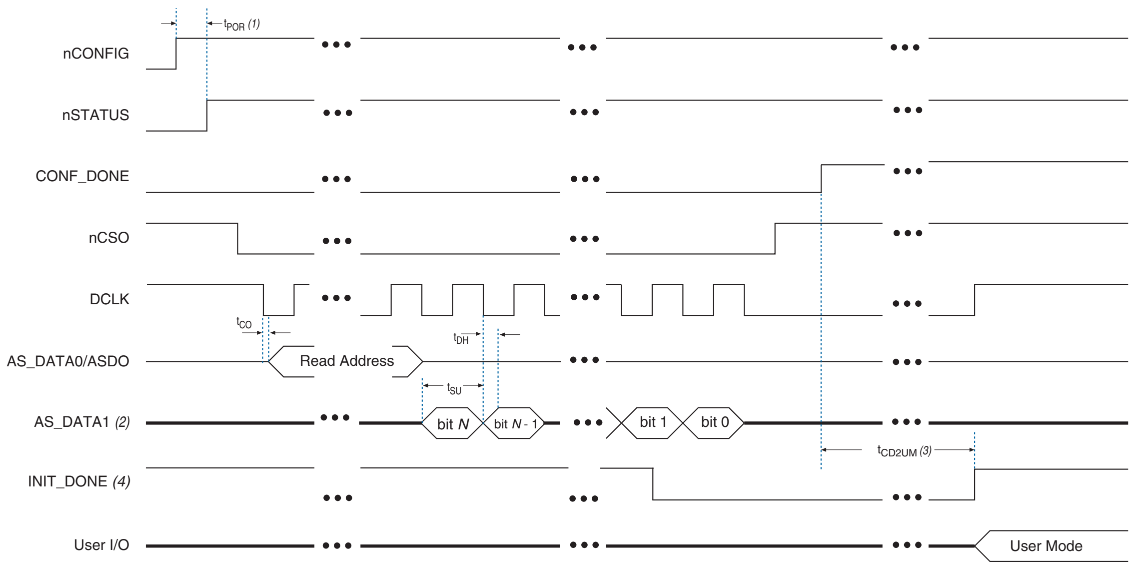
(4) N is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.

(5) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

AS Configuration Timing

Figure 22 shows the timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Figure 22. AS Configuration Timing



Notes to Figure 22:

(1) The AS scheme supports standard and fast POR delay (t_{POR}). For t_{POR} delay information, refer to the "POR Delay Specification" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(2) If you are using AS x4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.

(3) The initialization clock can be from the internal oscillator or CLKUSR pin.

(4) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 55 lists the timing parameters for AS x1 and AS x4 configurations in Arria V devices.

Table 55. AS Timing Parameters for AS x1 and x4 Configurations in Arria V Devices (1), (2)—*Preliminary*

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	4	µs
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_H	Data hold time after the falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 55:

(1) The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

(2) The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 57 on page 1–54.

Table 56 lists the internal clock frequency specification for the AS configuration scheme.

Table 56. DCLK Frequency Specification in the AS Configuration Scheme (1), (2)—*Preliminary*

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 56:

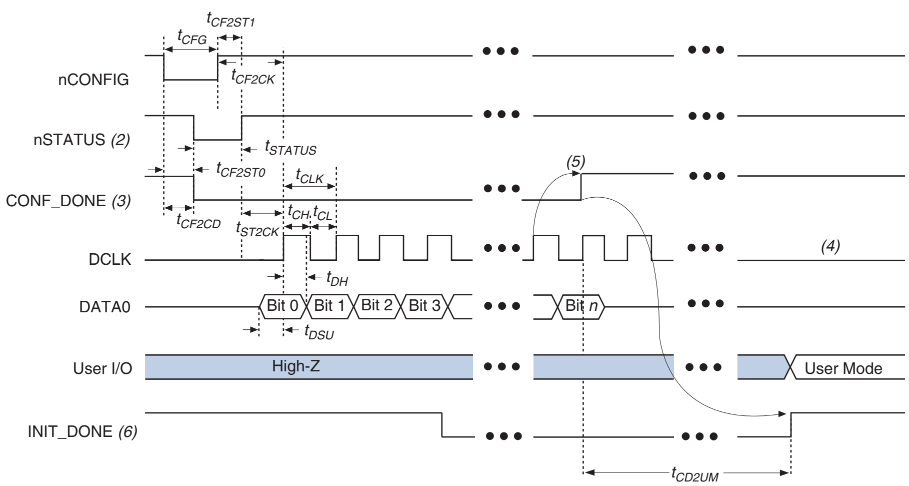
(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

PS Configuration Timing

Figure 23 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device or microprocessor as an external host.

Figure 23. PS Configuration Timing Waveform (1)



Notes to Figure 23:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power up, the Arria V device holds nSTATUS low for the time of the POR delay.

(3) After power up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high after the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(6) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 57 lists the PS timing parameter for Arria V devices.

Table 57. PS Timing Parameters for Arria V Devices—*Preliminary*

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 (1)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (2)	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (3)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 57:

(1) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

(3) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Initialization

Table 58 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency for Arria V devices.

Table 58. Initialization Clock Source Option and the Maximum Frequency for Arria V Devices

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	T_{init}
CLKUSR (1)	PS and FPP	125	
	AS	100	

Note to Table 58:

(1) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Configuration Files

Use Table 59 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (**.hex**) or tabular text file (**.ttf**) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

Table 59 lists the uncompressed raw binary file (**.rbf**) sizes for Arria V devices.

Table 59. Uncompressed .rbf Sizes for Arria V Devices (Part 1 of 2)—*Preliminary*

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V GX	A1	71,015,552	1,420,311
	A3	71,015,552	1,420,311
	A5 (1)	102,190,840	2,043,816
	A7 (1)	102,190,840	2,043,816
	B1	137,784,928	2,755,699
	B3	137,784,928	2,755,699
	B5	185,915,648	3,718,313
	B7	185,915,648	3,718,313
Arria V GT	C3	71,015,552	1,420,311
	C7 (1)	102,190,840	2,043,816
	D3	137,784,928	2,755,699
	D7	185,915,648	3,718,313
Arria V SX	B3 (1)	185, 915,648	3,718,313
	B5 (1)	185, 915,648	3,718,313

Table 59. Uncompressed .rbf Sizes for Arria V Devices (Part 2 of 2)—*Preliminary*

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V ST	D3 *(1)*	185, 915,648	3,718,313
	D5 *(1)*	185, 915,648	3,718,313

Note to Table 59:

(1) This device will be supported in a future release of the Quartus II software.

Remote System Upgrades Circuitry Timing Specification

Table 60 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 60. Remote System Upgrade Circuitry Timing Specification

Parameter	Minimum	Maximum	Unit
$t_{MAX\_RU\_CLK}$ *(1)*	—	40	MHz
$t_{RU\_nCONFIG}$ *(2)*	250	—	ns
$t_{RU\_nRSTIMER}$ *(3)*	250	—	ns

Notes to Table 60:

(1) This clock is user-supplied to the remote system upgrade circuitry. If you are using the ALTREMOTE_UPDATE megafunction, the clock user-supplied to the ALTREMOTE_UPDATE megafunction must meet this specification.

(2) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(3) This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

User Watchdog Internal Oscillator Frequency Specification

Table 61 lists the frequency specifications for the user watchdog internal oscillator.

Table 61. User Watchdog Internal Oscillator Frequency Specifications—*Preliminary*

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

You can download the Excel-based I/O Timing spreadsheet from the Arria V Devices Documentation webpage.

Programmable IOE Delay

Table 62 lists the Arria V I/O element (IOE) programmable delay settings.

Table 62. IOE Programmable Delay for Arria V Devices

Parameter	Available Settings	Minimum Offset	Fast Model		Slow Model					Unit
			Industrial	Commercial	–I3	–C4	–I5	–C5	–C6	
D1	31	0	0.474	0.474	0.832	0.865	0.969	1.002	1.141	ns
D3	7	0	1.633	1.632	2.869	2.982	3.343	3.458	3.936	ns
D4	31	0	0.473	0.473	0.832	0.865	0.969	1.003	1.142	ns
D5	31	0	0.473	0.473	0.832	0.865	0.970	1.004	1.142	ns

Programmable Output Buffer Delay

Table 63 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 63. Programmable Output Buffer Delay (1), (2)—*Preliminary*

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Notes to Table 63:

(1) Pending the Quartus II software extraction.

(2) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 64 lists the glossary for this datasheet.

Table 64. Glossary Table (Part 1 of 4)

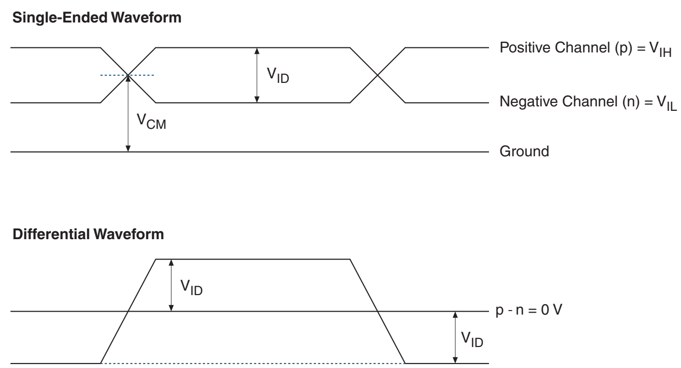
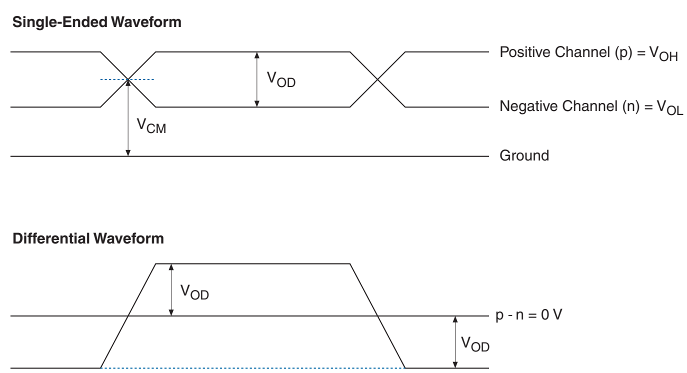
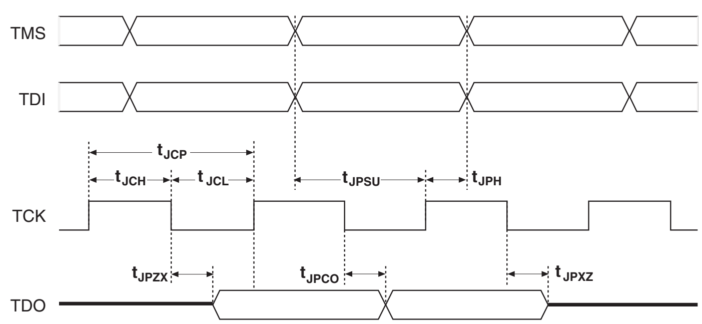
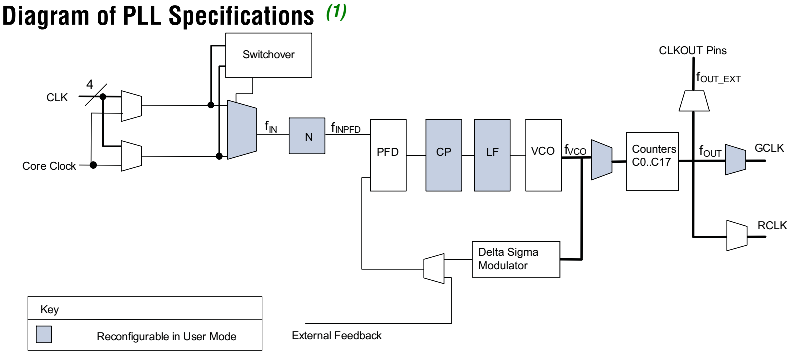
Letter	Subject	Definitions
A B C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms*  *Transmitter Output Waveforms* 
E	—	—
F	f_{HSCLK}	Left/right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G H I	—	—

Table 64. Glossary Table (Part 2 of 4)

<table>
<tr><th>Letter</th><th>Subject</th><th>Definitions</th></tr>
<tr><td rowspan="2">J</td><td>J</td><td>High-speed I/O block—Deserialization factor (width of parallel data bus).</td></tr>
<tr><td>JTAG Timing Specifications</td><td>JTAG Timing Specifications:

</td></tr>
<tr><td>K
L
M
N
O</td><td>—</td><td>—</td></tr>
<tr><td rowspan="2">P</td><td>PLL Specifications</td><td>Diagram of PLL Specifications (1)


Note:
(1) <code>Core Clock</code> can only be fed by dedicated clock input pins or PLL outputs.</td></tr>
<tr><td>Preliminary</td><td>Some tables show the designation as “Preliminary”. Preliminary characteristics are created using simulation results, process data, and other known parameters.

Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no preliminary designations on finalized tables.</td></tr>
<tr><td>Q</td><td>—</td><td>—</td></tr>
<tr><td>R</td><td>R_L</td><td>Receiver differential input discrete resistor (external to the Arria V device).</td></tr>
</table>

Table 64. Glossary Table (Part 3 of 4)

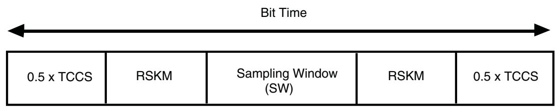
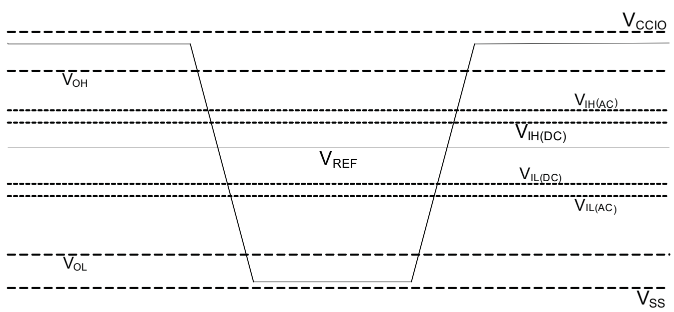
Letter	Subject	Definitions
S	**Sampling window (SW)**	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
	Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **SW** in this table).
	t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock. **Timing Unit Interval (TUI)** The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80–20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
	t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
	t_{RISE}	Signal low-to-high transition time (20–80%)
U	—	—

Table 64. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC Common mode input voltage.
	V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—Clock Boost Factor
X, Y, Z	—	—

Document Revision History

Table 65 lists the revision history for this document.

Table 65. Document Revision History

Date	Version	Changes

November 2012	3.0	■ Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 55, Table 56, and Table 59.
		■ Removed table: Transceiver Block Jitter Specifications for Arria V Devices.
		■ Added HPS information:
		  ■ Added "HPS Specifications" section.
		  ■ Added Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, and Table 49.
		  ■ Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.
		  ■ Updated Table 3 and Table 5.

October 2012	2.4	■ Updated Arria V GX $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ minimum and maximum values, and data rate in Table 4. ■ Added receiver VICM (AC coupled) and VICM (DC coupled) values, and transmitter VOCM (AC coupled) and VOCM (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	■ Updated the SERDES factor condition in Table 30.
July 2012	2.2	■ Updated the maximum voltage for V_I (DC input voltage) in Table 1. ■ Updated Table 20 to include the Arria V GX -I3 speed grade. ■ Updated the minimum value of the `fixedclk` clock frequency in Table 20 and Table 21. ■ Updated the SERDES factor condition in Table 30. ■ Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ values in Table 4.
June 2012	2.0	Updated for the Quartus II software v12.0 release: ■ Restructured document. ■ Updated "Supply Current and Power Consumption" section. ■ Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52. ■ Added Table 22, Table 23, and Table 33. ■ Added Figure 1–1 and Figure 1–2. ■ Added "Initialization" and "Configuration Files" sections.
February 2012	1.3	■ Updated Table 2–1. ■ Updated Transceiver-FPGA Fabric Interface rows in Table 2–20. ■ Updated V_{CCP} description.
December 2011	1.2	■ Updated Table 2–1 and Table 2–3.
November 2011	1.1	■ Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36. ■ Added Table 2–5. ■ Added Figure 2–4.
August 2011	1.0	Initial release.