Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Disclaimer

© 2017 Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Megacore, NIOS, Quartus Prime and Stratix words and logos are trademarks of Intel Corporation in the US and/or other countries. Other marks and brands may be claimed as the property of others. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

These pin connection guidelines, and your use thereof, are subject to and governed by Intel's terms and conditions below. By using these pin connection guidelines, you indicate your acceptance of all such terms and conditions. If you do not agree with such terms and conditions, you may not use the pin connection guidelines, and you are required to promptly and irrevocably destroy the pin connection guidelines and any copies or portions thereof in your possession or under your control.

Terms and Conditions:

1. These pin connection guidelines are provided as examples only, and should not be deemed to be technical specifications or recommendations. The use of the pin connection guidelines for any particular design should be verified for device operation with the applicable datasheet and Intel.
2. Subject to these terms and conditions, Intel grants to you the use of these pin connection guidelines as examples of possible pin connections of an Intel programmable logic device-based design. You may not use these pin connection guidelines for any other purpose except as expressly permitted in these terms and conditions. Intel does not recommend, suggest, or require that these pin connection guidelines be used in conjunction or combination with any other software or product, and makes no representations, warranties or guaranties, implied or express as well as any warranties arising from course of performance, course of dealing, or usage in trade including but not limited to the accuracy, completeness or genuineness thereof.
3. Intel will not be liable for any lost revenue, lost profits, or other consequential, indirect, or special damages caused by your use of these pin connection guidelines even if advised of the possibility of such damages occurring.
4. This agreement shall be governed in all respects by the laws of the State of Delaware, without regard to conflict of law or choice of law principles. You agree to submit to the exclusive jurisdiction of the federal and state courts in the State of Delaware for the resolution of any dispute or claim arising out of or relating to these terms of use.

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V GT and GX Pin Connection Guidelines

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins			
CLK[0:23][p:n]	I/O, Clock	Dedicated positive and negative clock input pins that can also be used for data inputs. OCT Rd is supported on these pins. When you use the single-ended I/O standard, only the CLK[0:23]p pins serve as the dedicated input pins to the PLL.	When you do not use these pins, Altera recommends tying them to GND or leaving them unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. You can reserve them as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUT0, FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUTp, FPLL_[BL,BC,BR,TL,TC,TR]_FB0	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended clock output pins , one differential clock output pair or single ended feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. You can reserve them as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUT1, FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUTn	I/O, Clock		
FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUT2, FPLL_[BL,BC,BR,TL,TC,TR]_FBp, FPLL_[BL,BC,BR,TL,TC,TR]_FB1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs, differential external feedback input pin or single ended feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. You can reserve them as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUT3, FPLL_[BL,BC,BR,TL,TC,TR]_FBn	I/O, Clock		

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Dedicated Configuration/JTAG Pins			
MSEL[0:4]	Input	Use these pins to set the configuration scheme and POR delay. These pins have an internal 25-kΩ pull-down that is always active.	When you use these pins, tie them directly to VCCPGM or GND to get the combination for the configuration scheme as specified in the "Configuration, Design Security, and Remote System Upgrades in Arria V Devices" chapter in the Arria V Handbook. These pins are not used in the JTAG configuration scheme. Tie the MSEL pins to GND if you are using the JTAG configuration scheme. Use only MSEL pin settings defined in the "Configuration, Design Security, and Remote System Upgrades in Arria V Devices" chapter.
AS_DATA0 / ASDO / DATA[0]	Bidirectional	In a passive serial (PS) or fast passive parallel (FPP) configuration scheme, DATA[0] is a dedicated input data pin. In an active serial (AS) x1 and AS x4 configuration schemes, AS_DATA0 and ASDO are dedicated bidirectional data pins.	When you do not use this pin, Altera recommends leaving the pin unconnected.
AS_DATA[1:3] / DATA[1:3]	Bidirectional	In an AS configuration scheme, AS_DATA[1:3] pins are used. In an FPP x8 or FPP x16 configuration scheme, the DATA[1:3] pins are used.	When you do not use this pin, Altera recommends leaving the pin unconnected.
nCSO/ DATA[4]	Bidirectional	In an AS configuration scheme, the nCSO pin is used. nCSO drives the control signal from the Arria V device to the EPCS or EPCQ device in the AS configuration scheme. In an FPP configuration scheme, the DATA4 pin is used.	When you are not programming the device in the AS configuration scheme, the nCSO pin is not used. When you do not use this pin as an output pin, Altera recommends leaving the pin unconnected.

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
nCE	Input	nCE is an active-low chip enable pin. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In a multi-device configuration, the nCE pin of the first device is tied low while its nCEO pin drives the nCE pin of the next device in the chain. In a single-device configuration and JTAG programming, connect the nCE pin to GND.
nCONFIG	Input	Pulling this pin low during configuration and user mode causes the Arria V device to lose its configuration data, enter a reset state, and tri-states all I/O pins. A low-to-high logic initiates a reconfiguration.	When you use the nCONFIG pin in a passive configuration scheme, connect the pin directly to the configuration controller. When you use the nCONFIG pin in an AS configuration scheme, connect the pin through a 10-kΩ resistor tied to VCCPGM. When you do not use the nCONFIG pin, connect the pin directly or through a 10-kΩ resistor to VCCPGM. During JTAG programming, the nCONFIG status is ignored.
CONF_DONE	Bidirectional (open-drain)	As a status output, the CONF_DONE pin drives low before and during configuration. After all configuration data is received without error and the initialization cycle starts, the CONF_DONE pin is released. As a status input, the CONF_DONE pin goes high after all data is received. Then the device initializes and enters user mode. This pin is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistor to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host.
nCEO	I/O, Output (open-drain)	Dual-purpose open-drain output pin. This pin drives low when device configuration completes.	During multi-device configuration, this pin feeds the nCE pin of the next device in the chain. If this pin is not feeding the nCE pin of the next device, you can use this pin as a regular I/O pin. In a single-device configuration, use this pin as a regular I/O pin. During single-device configuration, you may leave this pin floating. Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
nSTATUS	Bidirectional (open-drain)	The Arria V device drives the nSTATUS pin low immediately after power-up and releases it after the Arria V device exits power-on reset (POR). As a status output, the nSTATUS pin is pulled low to indicate an error during configuration. As a status input, the device enters an error state when the nSTATUS pin is driven low by an external source during configuration or initialization. This pin is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistor to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host.
TCK	Input	JTAG test clock input pin that clock input to the boundary-scan testing (BST) circuitry. Some operations occur at the rising edge, while others occur at the falling edge.It is expected that the clock input waveform has a nominal 50% duty cycle.This pin has an internal 25-kΩ pull-down that is always active.	Connect this pin to a 1-kΩ pull-down resistor to GND.
TMS	Input	JTAG test mode select input pin that provides the control signal to determine the transitions of the test access port (TAP) controller state machine. The TMS pin is evaluated on the rising edge of the TCK pin. Transitions in the state machine occur on the falling edge of the TCK after the signal is applied to the TMS pin. This pin has an internal 25-kΩ pull-up that is always active.	Connect this pin through a 1-kΩ - 10-kΩ pull-up resistor to the VCCPD in the dedicated I/O bank which the JTAG pin resides. If the JTAG connections are not used, connect the TMS pin to VCCPD using a 1-kΩ resistor.

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
TDI	Input	JTAG test data input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of the TCK pin. This pin has an internal 25-kΩ pull-up that is always active.	Connect this pin through a 1-kΩ - 10-kΩ pull-up resistor to the VCCPD in the dedicated I/O bank which the JTAG pin resides. If the JTAG connections are not used, connect the TDI pin to VCCPD using a 1-kΩ resistor.
TDO	Output	JTAG test data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of the TCK pin. This pin is tri-stated if the data is not being shifted out of the device.	To disable the JTAG circuitry, leave the TDO pin unconnected. In cases where the TDO pin uses VCCPD = 2.5 V to drive a 3.3 V JTAG interface, there may be leakage current in the TDI input buffer of the interfacing devices. You may use an external pull-up resistor tied to 3.3 V on their TDI pin to eliminate the leakage current if needed.
Optional/Dual-Purpose Configuration Pins			
DCLK	Input (PS, FPP) Output (AS)	Dedicated bidirectional clock pin. In the PS and FPP configuration schemes, the DCLK pin is the clock input used to clock configuration data from an external source into the Arria V device. In the AS configuration scheme, the DCLK pin is an output clock to clock the EPCS or EPCQ device.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	I/O, Output(open-drain)	Optional output pin. This pin is an open-drain output pin by default and requires a 10-kΩ pull-up resistor. Active high signal indicates that the error detection circuitry has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuitry is enabled.	When you use the dedicated CRC_ERROR pin configured as an open-drain output, connect this pin through an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated CRC_ERROR configured as an open-drain output, and when this pin is not used as an I/O pin, connect this pin as defined in the Quartus II software.
DEV_CLRn	I/O, Input	Optional input pin that allows you to override all clears on all the device registers. When this pin is driven low, all registers are cleared. When this pin is driven high (VCCPGM), all registers behave as programmed.	When you do not use the dedicated input DEV_CLRn pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin to GND.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
DEV_OE	I/O, Input	Optional input pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated. When this pin is driven high (VCCPGM), all I/O pins behave as programmed.	When you do not use the dedicated input DEV_OE pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin to GND.
DATA[5:15]	I/O, Input	Dual-purpose configuration data input pins. These pins are required for the FPP configuration scheme. Use DATA [5:7] pins for FPP x8, DATA [5:15] pins for FPP x16. You can use the pins that are not required for configuration as regular I/O pins.	When you do not use the DATA[5:15] input pins, and when these pins are not used as I/O pins, Altera recommends leaving these pins unconnected.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as an INIT_DONE pin in the Quartus II software. When this pin is enabled, a transition from low to high on the pin indicates that the device has entered user mode. If the INIT_DONE output pin option is enabled in the Quartus II software, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	When you use the dedicated INIT_DONE pin configured as an open-drain output pin, connect this pin through an external 10-kΩ pull-up resistor to VCCPGM. In Active Serial (AS) multi-device configuration mode, Altera recommends that the INIT_DONE output pin option is enabled in the Quartus II software for devices in the configuration chain. Do not tie INIT_DONE pins together between master and slave devices. Monitor the INIT_DONE status for each device to ensure successful transition into user-mode. When you do not use the dedicated INIT_DONE pin configured as open-drain output pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin as defined in the Quartus II software.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	When you do not use the CLKUSR pin as a configuration clock input pin, and when the pin is not used as an I/O pin, Altera recommends setting these pins “as output driving ground” and connecting this pin to GND. You can do so using the Pin Planner in the Quartus II software by finding the pin, right click “Reserve Pins” then select “As output driving ground”.
CvP_CONFDONE	I/O, Output(open-drain)	The CVP_CONFDONE pin is driven low during configuration. When Configuration via Protocol (CvP) is complete, this signal is released and is pulled high by an external pull-up resistor. Status of this pin is only valid if the CONF_DONE pin is high.	When you use the dedicated CvP_CONFDONE pin configured as an open-drain output pin, connect this pin through an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated CvP_CONFDONE pin configured as open-drain output pin, and when this pin is not used as an I/O pin, Altera recommendsconnecting this pin as defined in the Quartus II software.
nPERST[L0,R0]	I/O, Input	Dedicated fundamental reset pins. These pins are only available when you use them together with the PCI Express® (PCIe®) hard IP. When these pins are low, the transceivers are in reset. When these pins are high, the transceivers are out of reset. When these pins are not used as the fundamental reset, these pins may be used as user I/O pins.	Connect these pins as defined in the Quartus II software. This pin may be driven by 3.3V regardless of the VCCIO voltage level of the bank without a level translator as long as the input signal meets the LVTTL VIH/VIL specification and the overshoot specifications for 100% operation as listed in the device datasheet. Only one nPERST pin is used per PCIe hard IP. The Arria V GT and GX devices always have two two pins listed, even if the specific component might have 0 or 1 PCIe hard IP. nPERSTL0 = Bottom left PCIe hard IP & CvP nPERSTR0 = Bottom right PCIe hard IP (When available) For maximum compatibility, Altera recommends using the nPERSTL0 first, as this is the only location that supports CvP configuration scheme. Assuming you are using the bottom left PCIe hard IP, connect nPERST from your PCIe slot directly to nPERSTL0.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Partial Reconfiguration Pins			
PR_REQUEST	I/O, Input	Partial reconfiguration request pin. Drive this pin high to start partial reconfiguration. Drive this pin low to end reconfiguration. This pin can only be used in partial reconfiguration using the external host mode in the FPP x16 configuration scheme.	When you do not use the dedicated input PR_REQUEST pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin to GND.
PR_READY	I/O, Output or Output (open-drain)	The partial reconfiguration ready pin is driven low until the device is ready to begin partial reconfiguration. When the device is ready to start reconfiguration, this signal is released and is pulled high by an external pull-up resistor.	When you use the dedicated PR_READY pin configured as an open-drain output pin, connect this pin through an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated PR_READY pin configured as an open-drain output pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin as defined in the Quartus II software.
PR_ERROR	I/O, Output or Output (open-drain)	The partial reconfiguration error pin is driven low during partial reconfiguration unless the device detects an error. If an error is detected, this signal is released and pulled high by an external pull-up resistor.	When you use the dedicated PR_ERROR pin configured as an open-drain output pin, connect this pin through an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated PR_ERROR pin configured as an open-drain output pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin as defined in the Quartus II software.
PR_DONE	I/O, Output or Output(open-drain)	The partial reconfiguration done pin is driven low until the partial reconfiguration is complete. When the reconfiguration is complete, this signal is released and is pulled high by an external pull-up resistor.	When you use the dedicated PR_DONE pin configured as an open-drain output pin, connect this pin through an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated PR_DONE pin configured as an open-drain output pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin as defined in the Quartus II software.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Differential I/O Pins			
DIFFIO_RX_[B,T][#:#]p, DIFFIO_RX_[B,T][#:#]n	I/O, RX channel	These are true LVDS receiver channels on column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. OCT Rd is supported on all DIFFIO_RX pins and when VCCPD is 2.5V.	Connect unused pins as defined in the Quartus II software.
DIFFIO_TX_[B,T][#:#]p, DIFFIO_TX_[B,T][#:#]n	I/O, TX channel	These are true LVDS transmitter channels on column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Quartus II software.
DIFFOUT_[B,T,R][#:#]p, DIFFOUT_[B,T,R][#:#]n	I/O, TX channel	These are emulated LVDS output channels. All the user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. External resistor network is needed for emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins	Connect unused pins as defined in the Quartus II software. See Note 11.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
External Memory Interface Pins			
DQS[#][B,T,R]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in the Quartus II software.
DQSn[#][B,T,R]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Quartus II software.
DQ[#][B,T,R]	I/O, bidirectional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in the Quartus II software.
CQ[#][B,T,R]/CQn[#][B,T,R]	I/O, Input	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Connect unused pins as defined in the Quartus II software.
QK[#][B,T,R]	I/O, Input	Optional data strobe signal for use in RLDRAM II.	Connect unused pins as defined in the Quartus II software.
QKn[#][B,T,R]	I/O, Input	Optional complementary data strobe signal for use in RLDRAM II.	Connect unused pins as defined in the Quartus II software.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Hard Memory PHY Pins			
[B,T]_DQS_[#]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	If you use hard memory PHY, connection to memory device DQS pin must start from [B,T]_DQS_0 pin. For details, refer to the specific device pinout file. Connect unused pins as defined in the Quartus II software.
[B,T]_DQS#_[#]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	If you use hard memory PHY, connection to memory device DQSn pin must start from [B,T]_DQS#_0 pin. For details, refer to the specific device pinout file. Connect unused pins as defined in the Quartus II software.
[B,T]_DQ_[#]	I/O, bidirectional	Optional data signal for use in external memory interfacing. Use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	If you use hard memory PHY, connection to memory device DQ pin must start from [B,T]_DQ_0 pin. For details, refer to the specific device pinout file. Connect unused pins as defined in the Quartus II software.
DQS[#]_[1:8]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in the Quartus II software.
DQS#[#]_[1:8]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Quartus II software.

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
DQ[#]_[1:8]_[#]	I/O, bidirectional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in the Quartus II software.
CQ[#]_[1:8]/CQ#[#]_[1:8]	I/O, Input	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Connect unused pins to the CQ/CQn pins in the Pin Planner of the Quartus II software.
QK[#]_[1:8]	I/O, Input	Optional data strobe signal for use in RLDRAM II.	Connect unused pins to the QK[#] pins in the Pin Planner of the Quartus II software. (Sbar in the Quartus II Pin Planner)
QK#[#]_[1:8]	I/O, Input	Optional complementary data strobe signal for use in RLDRAM II.	Connect unused pins to the QKn[#] pins in the Pin Planner of the Quartus II software. (S in the Quartus II Pin Planner)
DM[#]_[1:8]	I/O, Output	Optional Write Data Mask, edge-aligned to DQ during Write.	Connect unused pins as defined in the Quartus II software.
WE#_[1:8]	I/O, Output	Write enable. Write-enable input for DDR2, DDR3 SDRAM and RLDRAM II	Connect unused pins as defined in the Quartus II software.
CAS#_[1:8]	I/O, Output	Column Address Strobe for DDR2 & DDR3 SDRAM	Connect unused pins as defined in the Quartus II software.
RAS#_[1:8]	I/O, Output	Row Address Strobe for DDR2 & DDR3 SDRAM.	Connect unused pins as defined in the Quartus II software.
RPS#_[1:8]	IO, Output	Read signal to QDRII memory. Active low and reset in the inactive state	Connect unused pins as defined in the Quartus II software.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
WPS#_[1:8]	IO, Output	Write signal to QDRII memory. Active low & reset in the inactive state.	Connect unused pins as defined in the Quartus II software.
RESET#_[1:8]	IO, Output	Active low reset signal.	Connect unused pins as defined in the Quartus II software.
CK_[1:8]	IO, Output	Input clock for external memory devices	Connect unused pins as defined in the Quartus II software.
CK#_[1:8]	IO, Output	Input clock for external memory devices, inverted CK	Connect unused pins as defined in the Quartus II software.
CKE_[1:8]_[#]	IO, Output	Active low clock enable.	Connect unused pins as defined in the Quartus II software.
BA_[1:8]_[#]	IO, Output	Bank address input for DDR2, DDR3 SDRAM and RLDRAM II	Connect unused pins as defined in the Quartus II software.
A_[1:8]_[#]	IO, Output	Address input for DDR2, DDR3 SDRAM, RLDRAM II and QDRII/+ SRAM	Connect unused pins as defined in the Quartus II software.
CS#_[1:8]_[#]	IO, Output	Active low Chip Select.	Connect unused pins as defined in the Quartus II software.
CA_[1:8]_[#]	IO, Output	Command and address input for LPDDR SDRAM	Connect unused pins as defined in the Quartus II software.
REF#_[1:8]	IO, Output	Auto-refresh control input for RLDRAM II	Connect unused pins as defined in the Quartus II software.
ODT_[1:8]_[#]	IO, Output	On die termination signal to set the termination resistors to each pin.	Connect unused pins as defined in the Quartus II software.

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Reference Pins			
RREF_BR	Input	Reference resistor for right (R) side transceiver, and bottom (B) and right (R) sides PLL of the device.	If any PLL on the right and bottom sides of the device is used, or any REFCLK pin or transceiver channel on right side of the device is used, you must connect each RREF pin on that side of the device to its own individual 2.0-kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.
RREF_TL	Input	Reference resistor for left (L) side transceiver, and top (T) and left (L) sides PLL of the device.	If any PLL on the left and top sides of the device is used, or any REFCLK pin or transceiver channel on the left side of the device is used, you must connect each RREF pin on that side of the device to its own individual 2.0-kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.
RZQ_[0,1,5,6]	I/O, Input	Reference pins for I/O banks. The RZQ pins share the same VCCIO with the I/O bank where they are located. The external precision resistor must be connected to the designated pin within the bank. If not required, this pin is a regular I/O pin.	If the device does not use this dedicated input for the external precision resistor or as an I/O, Altera recommends connecting the pin to GND. If used for OCT calibration, connect the RZQ pin to GND through an external 100- or 240- reference resistor depending on the desired OCT impedance. Refer to the Arria V handbook for the OCT impedance options for the desired OCT scheme.
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, ground, or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration you may connect these pins to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Supply Pins (See Notes 4 through 7)			
VCC	Power	VCC supplies power to the core.	For the Arria V GX -C4, -C5, -I5, -C6, and Arria V GT -I5 devices, connect all VCC pins to a 1.1V low noise switching regulator. For the Arria V GX -I3, Arria V GT -I3, and Arria V SX and ST –I3 devices, connect all VCC pins to a 1.15V low noise switching regulator. You may source VCCP from the same regulator as VCC with proper isolation filters. Use Arria V Early Power Estimator to determine the current requirements for VCC and other power supplies. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, 6, and 7.
VCCP	Power	VCCP supplies power to the periphery, HIP, and PCS.	For the Arria V GX -C4, -C5, -I5, -C6, and Arria V GT -I5 devices, connect VCCP pins to a 1.1V low noise switching regulator. For the Arria V GX - I3, Arria V GT -I3, and Arria V SX and ST –I3 devices, connect all VCCP pins to a 1.15V low noise switching regulator. You may tie these pins to the same regulator as VCC with proper isolation filters. For VCC and VCCP on smaller form factor boards where board thickness and layer count are limited, for example on a PCI Express card, ensure that VCC and VCCP are isolated from each other as much as possible by placing them on separate layers as far from each other as possible. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, 6, and 7.
VCCD_FPLL	Power	PLL Digital power.	Connect all VCCD_FPLL pins to a 1.5V linear or low noise switching power supply. These pins may be tied to the same regulator as VCCH_GXB and VCCBAT. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCA_FPLL	Power	PLL Analog power.	Connect these pins to a 2.5V low noise switching power supply through a proper isolation filter. For more information, refer to the respective power supply sharing guidelines. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCC_AUX	Power	Auxiliary supply for the programmable power technology.	Connect all VCC_AUX pins to a 2.5V low noise switching power supply through a proper isolation filter. For more information, refer to the respective power supply sharing guidelines. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCCIO[3,4,5,6,7,8]	Power	These are I/O supply voltage pins for I/O banks. Each bank can support a different voltage level from 1.2V to 3.3V. Supported I/O standards are LVTTL/ LVCMOS (3.3, 3.0, 2.5, 1.8, 1.5, 1.2V), SSTL(2,18,15 Class-I/II), SSTL(135, 125), HSTL(18,15,12 Class-I/II), HSUL12, LVDS, LVPECL, PCI/PCI-X.	Connect these pins to 1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V, 3.0V, or 3.3V supplies, depending on the I/O standard connected to the specified bank. When these pins require 2.5V you may tie them to the same regulator as VCCPD and VCCPGM, but only if each of these supplies require 2.5V sources. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8.
VCCPGM	Power	Configuration pins power supply which support 1.8, 2.5, 3.0 & 3.3V	Connect these pins to either 1.8V, 2.5V, 3.0V, or 3.3V power supply. When these pins require 2.5V you may tie them to the same regulator as VCCIO and VCCPD, but only if each of these supplies require 2.5V sources. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, and 4.
VCCPD[3,4,5,6,7,8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 2.5V, 3.0 & 3.3V.	The VCCPD pins require 2.5V, 3.0V, or 3.3V power supply. When these pins have the same voltage requirements as VCCPGM and VCCIO, you may tie them to the same regulator. The voltage on VCCPD is dependent on the VCCIO voltage. When VCCIO is 3.3V, VCCPD must be 3.3V. When VCCIO is 3.0V, VCCPD must be 3.0V. When VCCIO is 2.5V or less, VCCPD must be 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCBAT	Power	Battery back-up power supply for design security volatile key register.	If you are using design security volatile key, connect this pin to a non-volatile battery power source in the range of 1.2V to 3.0V. If you are not using the volatile key, connect this pin to a 1.5V, 2.5V, or 3.0V power supply. Arria V devices will not exit POR if VCCBAT is not powered up.
GND	Ground	Device ground pins.	Connect all GND pins to the board ground plane.
VREF[#]N0	I/O, Power	Input reference voltage for each I/O bank. If a bank uses a voltage referenced I/O standard for input operation, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.	VREF pins will source current and the regulator used for VREF pins should have the capability to sink and source current. If VREF pins are not used, connect these pins to either the VCCIO in the bank in which the pin resides or GND. When VREF pins are used as I/O, they have higher capacitance than regular I/O pins which will slow the edge rates and affect I/O timing. Decoupling depends on the design decoupling requirements of the specific board. See Notes 2 and 8.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Tranceiver Pins (See Notes 4 through 10)			
VCCR_GXB[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.	For the Arria V GX -C4, -C5, -I3, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps and Arria V SX -C4, -C5, -I3, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps, connect VCCR_GXB pins to a 1.1V low noise switching regulator. For the Arria V GX -C4, -C5, -I3 and -I5 devices with transceiver data rates > 3.2Gbps and Arria V SX -C4, -C5, -I3 and -I5 devices with transceiver data rates > 3.2Gbps, connect VCCR_GXB pins to a 1.15V low noise switching regulator. For the Arria V GT and Arria V ST devices, connect VCCR_GXB pins to a 1.2V low noise switching regulator. For Arria V GX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps and Arria V SX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps, you may tie these pins to the same 1.1V regulator as VCC with a proper isolation filter. For Arria V GX -C4, -C5, and -I5 devices with transceiver data rates > 3.2Gbps, Arria V GX -I3 devices, Arria V GT devices, Arria V SX -C4, -C5, and -I5 devices with transceiver data rates > 3.2Gbps, Arria V SX -I3 devices, and Arria V ST devices, you may tie these pins to the same regulator as VCCL_GXB. Decoupling of these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 7, and 10.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCT_GXB[L,R][0..3]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.	For the Arria V GX -C4, -C5, -I3, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps and Arria V SX -C4, -C5, -I3, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps, connect VCCT_GXB pins to a 1.1V low noise switching regulator. For the Arria V GX -C4, -C5, -I3 and -I5 devices with transceiver data rates > 3.2Gbps and Arria V SX -C4, -C5, -I3 and -I5 devices with transceiver data rates > 3.2Gbps, connect VCCT_GXB pins to a 1.15V low noise switching regulator. For the Arria V GT and Arria V ST devices, connect VCCT_GXB pins to a 1.2V low noise switching regulator. For Arria V GX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps and Arria V SX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps, you may tie these pins to the same 1.1V regulator as VCC with a proper isolation filter. For Arria V GX -C4, -C5, and -I5 devices with transceiver data rates > 3.2Gbps, Arria V GX -I3 devices, Arria V GT devices, Arria V SX -C4, -C5, and -I5 devices with transceiver data rates > 3.2Gbps, Arria V SX -I3 devices, and Arria V ST devices, you may tie these pins to the same regulator as VCCR_GXB and VCCL_GXB with a proper isolation filter. Decoupling of these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 7, and 10.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCL_GXB[L,R][0..3]	Power	Analog power, transceiver clock network power, specific to the left (L) or the right (R) of the device.	For the Arria V GX -C4, -C5, -I3, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps and Arria V SX -C4, -C5, -I3, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps, connect VCCL_GXB pins to a 1.1V low noise switching regulator. For the Arria V GX -C4, -C5, -I3 and -I5 devices with transceiver data rates > 3.2Gbps and Arria V SX -C4, -C5, -I3 and -I5 devices with transceiver data rates > 3.2Gbps, connect VCCL_GXB pins to a 1.15V low noise switching regulator. For the Arria V GT and Arria V ST devices, connect VCCL_GXB pins to a 1.2V low noise switching regulator. For Arria V GX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps and Arria V SX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps, you may tie these pins to the same 1.1V regulator as VCC with a proper isolation filter. For Arria V GX -C4, -C5, and -I5 devices with transceiver data rates > 3.2Gbps, Arria V GX -I3 devices, Arria V GT devices, Arria V SX -C4, -C5, and -I5 devices with transceiver data rates > 3.2Gbps, Arria V SX -I3 devices, and Arria V ST devices, you may tie these pins to the same regulator as VCCR_GXB. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, 7, and 10.
VCCH_GXB[L,R][0..3]	Power	Analog power, transmitter output buffer power, specific to the left (L) or the right (R) of the device.	Connect VCCH_GXB to a 1.5V linear or low noise switching regulator. You may source these pins from the same regulator as VCCD_FPLL and VCCBAT. Decoupling of these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 7, and 10.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCA_GXB[L,R][0..3]	Power	Analog power, transceiver high voltage power, specific to the left (L) side or right (R) side of the device.	Connect VCCA_GXB to a 2.5V low noise switching regulator. For more information, refer to the respective power supply sharing guidelines. Decoupling of these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 7, and 10.
GXB_RX_[L,R][0:11][p,n], GXB_REFCLK_[L,R][0:11][p,n]	Input	High speed positive (p) or negative (n) differential receiver channels. High speed positive (p) or negative (n) differential reference clock Specific to the left (L) side or right (R) side of the device.	These pins are AC-coupled when used. GXB_RX pins can be DC-coupled for data rates <= 3.2Gbps and custom protocol implementation. Connect all unused pins directly to GND. Some GXB_RX pins have the 10Gbps capability in the Arria V GT device. For details, refer to the Transceiver Architecture chapter in the Arria V Device Handbook. See Note 9.
GXB_TX_[L,R][0:11][p,n]	Output	High speed positive (p) and negative (n) differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TX pins floating. Some GXB_TX pins have the 10Gbps capability in the Arria V GT device. For details, refer to the Transceiver Architecture chapter in the Arria V Device Handbook.
REFCLK[0:3][L,R]_[p:n]	Input	High speed positive (p) & negative (n) differential reference clock, specific to the left (L) side or right (R) side of the device.	In the PCI Express configuration, DC-coupling is allowed on the REFCLK if the selected REFCLK I/O standard is HCSL. These pins must be AC-coupled if the selected REFCLK I/O standard is not HCSL. See Note 9 for non-HCSL I/O standard. Connect all unused pins directly to GND.

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Notes to Arria V GT and GX Pin Connection Guidelines

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are based on the Arria V GT and GX device variants.
2. Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage droop requirements of the device/supply. Then, decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling.
3. Use the Arria V Early Power Estimator to determine the current requirements for VCC and other power supplies.
4. These supplies may share power planes across multiple Arria V devices.
5. Example 1 and Figure 1 illustrate the power supply sharing guidelines for Arria V GX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.2Gbps. Example 2 and Figure 2 illustrate the power supply sharing guidelines for Arria V GX -C4, -C5, and -I5 devices with transceiver data rates > 3.2Gbps. Example 3 and Figure 3 illustrate the power supply sharing guidelines for Arria V GX -I3 devices. Example 4 and Figure 4 illustrate the power supply sharing guidelines for Arria V GT -I3 devices. Example 5 and Figure 5 illustrate the power supply sharing guidelines for Arria V GT -I5 devices.
6. Power pins should not share breakout vias from the BGA. Each ball on the BGA must have its own dedicated breakout via. VCC and VCCP must not share breakout vias.
7. Low Noise Switching Regulator - a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response. The switching frequency range is not an Altera requirement. However, Altera does require the Line Regulation and Load Regulation meet the following specifications:
   - Line Regulation < 0.4%
   - Load Regulation < 1.2%

   You have the option to use a linear regulator depending on your design and your system’s power and thermal budget considerations.
8. The number of modular I/O banks on Arria V devices depends on the device density. For the indexes available for a specific device, refer to the I/O Bank section in the Arria V handbook.
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires that the AC-coupling capacitor is placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. All transceiver power pins on the same side of the device must be connected either to the required supply or to GND. When ALL transceiver channels on the same side are unused, you have the option to connect all of the transceiver power pins on the same side of the device to GND or to the required supply.
11. For item [#], refer to the device pin table for the pin-out mapping.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V ST and SX Pin Connection Guidelines

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Dedicated Configuration/JTAG Pins			
HPS_TDI	Input	JTAG test Data input pin for instructions as well as test and programming Data. Data is shifted in on the rising edge of the TCK pin. This pin has an internal 25-kΩ pull-up resistor that is always active.	Connect this pin through a 1-kΩ - 10-kΩ pull-up resistor to VCCPD_HPS in the dedicated I/O bank which the JTAG pin resides. To disable the JTAG circuitry, connect the TDI pin to VCCPD_HPS using a 1-kΩ resistor.
HPS_TMS	Input	JTAG test mode Select input pin that provides the control signal to determine the transitions of the test access port (TAP) controller state machine. The TMS pin is evaluated on the rising edge of the TCK pin. Therefore, you must set up the TMS pin before the rising edge of the TCK pin. Transitions in the state machine occur on the falling edge of the TCK after the signal is applied to the TMS pin. This pin has an internal 25-kΩ pull-up resistor that is always active.	Connect this pin through a 1-kΩ - 10-kΩ - pull-up resistor to the VCCPD_HPS in the dedicated I/O bank which the JTAG pin resides. To disable the JTAG circuitry, connect the TMS pin to VCCPD_HPS using a 1-kΩ resistor.
HPS_TRST	Input	Active-low input to asynchronously reset the boundary-scan circuit. This pin has an internal 25-kΩ pull-up that is always active.	Connect this pin through a 1-kΩ - 10-kΩ pull-up resistor to the VCCPD_HPS in the dedicated I/O bank which the JTAG pin resides. To disable the JTAG circuitry, connect the TRST pin to GND through a 1-kΩ pull-down resistor.
HPS_TCK	Input	JTAG test clock input pin that clock input to the boundary-scan testing (BST) circuitry. Some operations occur at the rising edge, while others occur at the falling edge. It is expected that the clock input waveform have a nominal 50% duty cycle. This pin has an internal 25-kΩ pull-down that is always active.	Connect this pin through a 1-kΩ - 10-kΩ pull-down resistor to GND.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
HPS_TDO	Output	JTAG test Data output pin for instructions as well as test and programming Data. Data is shifted out on the falling edge of the TCK pin. This pin is tri-stated if the Data is not being shifted out of the device.	To disable the JTAG circuitry, leave the HPS_TDO pin unconnected. In cases where the HPS_TDO pin uses VCCPD_HPS = 2.5 V to drive a 3.3 V JTAG interface, there may be leakage current in the HPS_TDI input buffer of the interfacing devices. An external pull-up resistor tied to 3.3 V on the HPS_TDI pin may be used to eliminate the leakage current if needed.
HPS_nRST	I/O, bidirectional	Warm reset to the HPS block. Active low input affects the system reset domains which allows debugging to operate. This pin has an internal 25-kΩ pull-up resistor that is always active.	Connect this pin through a 1-kΩ - 10-kΩ pull-up resistor to VCCRSTCLK_HPS.
HPS_nPOR	I/O, Input	Cold reset to the HPS block. Active low input that will reset all HPS logics that can be reset. Places the HPS in a default state sufficient for software to boot. This pin has an internal 25-kΩ pull-up resistor that is always active.	Connect this pin through a 1-kΩ - 10-kΩ pull-up resistor to VCCRSTCLK_HPS.
HPS_PORSEL	Input	Dedicated input that selects between a standard POR or a fast POR delay for HPS block. A logic low selects a standard POR delay setting and a logic high selects a fast POR delay setting. This pin has an internal 25-kΩ pull-down resistor that is always active.	Connect this pin directly to VCCRSTCLK_HPS or GND.
Clock Pins			
HPS_CLK1	Input, Clock	Dedicated clock input pin that drives the main PLL. This provides clocks to the MPU, L3/L4 sub-systems, debug sub-system and the Flash controllers. It can also be programmed to drive the peripheral and SDRAM PLLs.	Connect a single-ended clock source to this pin. The I/O standard of the clock source must be compatible with VCCRSTCLK_HPS. Refer to the valid frequency range of the clock source in Arria V Device Datasheet. The input clock must be present at this pin for HPS operation.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
HPS_CLK2	Input, Clock	Dedicated clock input pin that can be programmed to drive the peripheral and SDRAM PLLs.	Connect a single-ended clock source to this pin. The I/O standard of the clock source must be compatible with VCCRSTCLK_HPS. Refer to the valid frequency range of the clock source in Arria V Device Datasheet. This is an optional HPS clock input pin. When you do not use this pin, Altera recommends tying it to VCCRSTCLK_HPS.
Supply Pins (See Notes 4 through 7)			
VCC_HPS	Power	VCC_HPS supplies power to the HPS core.	Connect all VCC_HPS pins to a 1.1V low noise switching regulator for Arria V SX and ST devices except Arria V SX and ST –I3 devices. Connect all VCC_HPS pins to a 1.15V low noise switching regulator for Arria V SX and ST –I3 devices. If powering down of the FPGA fabric is not required, VCC_HPS pins may be sourced from the same regulator as VCC with a proper isolation filter. Use the Arria V Early Power Estimator to determine the current requirements for VCC_HPS and other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 6.
VCCIO[#]_HPS	Power	These are I/O supply voltage pins for I/O banks. Each bank can support a different voltage level from 1.2V to 3.3V. Supported I/O standards are LVTTL/ LVCMOS (3.3, 3.0, 2.5, 1.8, 1.5V), SSTL(18,15, 2 Class-I/II), HSTL(18,15 Class-I/II), HSUL12, LVDS, LVPECL, and PCI/PCI-X.	Connect these pins to a 1.2V, 1.5V, 1.8V, 2.5V, 3.0V, or 3.3V power supply, depending on the I/O standard required by the specified bank. When these pins have the same voltage requirements as VCCPD_HPS and VCCRSTCLK_HPS, they may be tied to the same regulator. If powering down of the FPGA fabric is not required and if these pins have the

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
			same voltage requirement as VCCIO, VCCIO_HPS pins may be sourced from the same regulator as VCCIO. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8.
VCCPLL_HPS	Power	VCCPLL_HPS supplies power to the HPS core PLLs.	Connect these pins to a 2.5V low noise switching power supply through a proper isolation filter. For more information, refer to the respective power sharing guidelines. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCCRSTCLK_HPS	Power	VCCRSTCLK_HPS supplies power to HPS clock and reset pins.	Connect these pins to either a 1.8V, 2.5V, 3.0V, or 3.3V power supply. When these pins have the same voltage requirements as VCCIO_HPS and VCCPD_HPS, they may be tied to the same regulator. If powering down of the FPGA fabric is not required and if these pins have the same voltage requirement as VCCIO, VCCPGM, and VCCPD, they may be tied to the same regulator. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, and 4.
VCC_AUX_SHARED	Power	Auxiliary supply.	VCC_AUX_SHARED must always be powered up at 2.5V for the HPS operation. Connect this pin to VCC_AUX using a proper isolation filter. For more information, refer to the respective power sharing guidelines. See Notes 2,3,4, and 7.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCPD[#]_HPS	Power	Dedicated power pins.	The VCCPD_HPS pins require 2.5V, 3.0V or 3.3V. When these pins have the same voltage requirements as VCCRSTCLK_HPS and VCCIO_HPS, they may be tied to the same regulator. The voltage on VCCPD_HPS is dependent on the VCCIO_HPS voltage. If powering down of the FPGA fabric is not required and if these pins have the same voltage requirement as VCCPD, VCCIO, and VCCPGM, they may be tied to the same regulator. When VCCIO_HPS is 3.3V, VCCPD_HPS must be 3.3V. When VCCIO_HPS is 3.0V, VCCPD_HPS must be 3.0V. When VCCIO_HPS is 2.5V or less, VCCPD_HPS must be 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8.
VREFB[#]N0_HPS	Power	Input reference voltage for each I/O bank. If a bank uses a voltage referenced I/O standard for input operation, then these pins are used as the voltage-reference pins for the bank.	VREF pins will source current and the regulator used for VREF pins should have the capability to sink and source current. If the VREF pins are not used, you should connect them to either the VCCIO in the bank in which the pin resides or GND.
Hard Memory PHY Pins			
HPS_DQ[#]	I/O, bidirectional	Optional data signal for use in external memory interfacing. Use caution when making pin assignments if you plan on migrating to a different memory interface that has a different HPS_DQ bus width. Analyze the available HPS_DQ pins across all pertinent HPS_DQS columns in the pin list.	If hard memory PHY is used, connection to memory device DQ pin must start from [B,T]_DQ_0 pin. For details, refer to the specific device pinout file. Connect unused pins as defined in the Quartus II software.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
HPS_DQS_[#]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated HPS_DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	If hard memory PHY is used, connection to memory device DQS pin must start from [B,T]_DQS_0 pin. For details, refer to the specific device pinout file. Connect unused pins as defined in the Quartus II software.
HPS_DQS#_[#]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated HPS_DQS phase shift circuitry.	If hard memory PHY is used, connection to memory device DQSn pin must start from [B,T]_DQS#_0 pin. For details, refer to the specific device pinout file. Connect unused pins as defined in the Quartus II software.
HPS_DM_[#]	I/O, Output	Optional write data mask, edge-aligned to HPS_DQ during write.	Connect unused pins as defined in the Quartus II software.
HPS_WE#	I/O, Output	Write-Enable input for DDR2 andDDR3 SDRAM.	Connect unused pins as defined in the Quartus II software.
HPS_CAS#	I/O, Output	Column address strobe for DDR2 and DDR3 SDRAM.	Connect unused pins as defined in the Quartus II software.
HPS_RAS#	I/O, Output	Row address strobe for DDR2 and DDR3 SDRAM.	Connect unused pins as defined in the Quartus II software.
HPS_RESET#	I/O, Output	Active low reset signal.	Connect unused pins as defined in the Quartus II software.
HPS_CK	I/O, Output	Output clock for external memory devices.	Connect unused pins as defined in the Quartus II software.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
HPS_CK#	I/O, Output	Output clock for external memory devices, inverted CK.	Connect unused pins as defined in the Quartus II software.
HPS_BA_[#]	I/O, Output	Bank address input for DDR2 and DDR3 SDRAM.	Connect unused pins as defined in the Quartus II software.
HPS_A_[#]	I/O, Output	Address input for DDR2 and DDR3 SDRAM.	Connect unused pins as defined in the Quartus II software.
HPS_CA_[#]	I/O, Output	Command and address inputs for LPDDR and LPDDR2 SDRAM.	Connect unused pins as defined in the Quartus II software.
HPS_CS#_[#]	I/O, Output	Active low chip Select.	Connect unused pins as defined in the Quartus II software.
HPS_ODT_[#]	I/O, Output	On-die termination signal enables and disables termination resistance internal to the external memory.	Connect unused pins as defined in the Quartus II software.
Reference Pins			
HPS_RZQ_0	I/O, Input	Reference pin for I/O banks. The HPS_RZQ_0 pins shares the same HPS_VCCIO with the I/O bank where it is located. The external precision resistor must be connected to the designated pin within the bank. If not required, these pins are regular I/O pins.	When the Arria V SoC device does not use these dedicated input pins for the external precision resistor or as I/O pins, Altera recommends connecting these pins to GND. When these pins are used for the OCT calibration, the HPS_RZQ_0 pin is connected to GND through an external 100-Ω or 240-Ω reference resistor depending on the desired OCT impedance. For the OCT impedance options for the desired OCT scheme, refer to the Arria V device handbook, I/O Features in Arria V Devices Chapter.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
General Purpose Input Pins (See Note 13)							
HPS_GPI#	Input	General purpose inputs signals in the SDRAM bank					These pins use the same VCCIO_HPS as the other HPS SDRAM pins. Connect unused pins as defined in the Quartus II software.
Peripheral Pins (See Note 12 & 13)							
		Power-up	**Function 3**	**Function 2**	**Function 1**	**Function 0**	
RGMII0_TX_CLK	I/O		RGMII0 Transmit clock			General Purpose IO Bit 0	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_TXD0	I/O		RGMII0 Transmit Data Bit 0	USB1 Data Bit 0		General Purpose IO Bit 1	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_TXD1	I/O		RGMII0 Transmit Data Bit 1	USB1 Data Bit 1		General Purpose IO Bit 2	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_TXD2	I/O		RGMII0 Transmit Data Bit 2	USB1 Data Bit 2		General Purpose IO Bit 3	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_TXD3	I/O		RGMII0 Transmit Data Bit 3	USB1 Data Bit 3		General Purpose IO Bit 4	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_RXD0	I/O		RGMII0 Receive Data Bit 0	USB1 Data Bit 4		General Purpose IO Bit 5	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_MDIO	I/O		RGMII0 Management Data IO	USB1 Data Bit 5	I2C2 Serial Data	General Purpose IO Bit 6	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_MDC	I/O		RGMII0 Management Data Clock	USB1 Data Bit 6	I2C2 Serial Clock	General Purpose IO Bit 7	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_RX_CTL	I/O		RGMII0 Receive Control	USB1 Data Bit 7		General Purpose IO Bit 8	If unused, program it in the Quartus II software as an input with a weak pull-up.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
RGMII0_TX_CTL	I/O		RGMII0 Transmit Control			General Purpose IO Bit 9	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_RX_CLK	I/O		RGMII0 Receive Clock	USB1 Clock		General Purpose IO Bit 10	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_RXD1	I/O		RGMII0 Receive Data Bit 1	USB1 Stop Data		General Purpose IO Bit 11	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_RXD2	I/O		RGMII0 Receive Data Bit 2	USB1 Direction		General Purpose IO Bit 12	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII0_RXD3	I/O		RGMII0 Receive Data Bit 3	USB1 Next Data		General Purpose IO Bit 13	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_ALE	I/O		NAND Address Latch Enable	RGMII1 Transmit clock	QSPI Slave Select 3	General Purpose IO Bit 14	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_CE	I/O		NAND Chip Enable	RGMII1 Transmit Data Bit 0	USB1 Data Bit 0	General Purpose IO Bit 15	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_CLE	I/O		NAND Command Latch Enable	RGMII1 Transmit Data Bit 1	USB1 Data Bit 1	General Purpose IO Bit 16	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_RE	I/O		NAND Read Enable	RGMII1 Transmit Data Bit 2	USB1 Data Bit 2	General Purpose IO Bit 17	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_RB	I/O		NAND Ready/Busy	RGMII1 Transmit Data Bit 3	USB1 Data Bit 3	General Purpose IO Bit 18	If used as the NAND Ready/Busy input, connect this pin through a 1-kΩ - 10-kΩ pull-up resistor to VCCPD_HPS in the dedicated I/O bank which the NAND_RB pin resides. If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_DQ0	I/O		NAND Data Bit 0	RGMII1 Receive Data		General Purpose IO	If unused, program it in the Quartus II software as an input with a weak pull-up.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
				Bit 0		Bit 19	
NAND_DQ1	I/O		NAND Data Bit 1	RGMII1 Management Data IO	I2C3 Serial Data	General Purpose IO Bit 20	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_DQ2	I/O		NAND Data Bit 2	RGMII1 Management Data clock	I2C3 Serial clock	General Purpose IO Bit 21	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_DQ3	I/O		NAND Data Bit 3	RGMII1 Receive control	USB1 Data Bit 4	General Purpose IO Bit 22	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_DQ4	I/O		NAND Data Bit 4	RGMII1 Transmit control	USB1 Data Bit 5	General Purpose IO Bit 23	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_DQ5	I/O		NAND Data Bit 5	RGMII1 Receive clock	USB1 Data Bit 6	General Purpose IO Bit 24	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_DQ6	I/O		NAND Data Bit 6	RGMII1 Receive Data Bit 1	USB1 Data Bit 7	General Purpose IO Bit 25	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_DQ7	I/O		NAND Data Bit 7	RGMII1 Receive Data Bit 2		General Purpose IO Bit 26	If unused, program it in the Quartus II software as an input with a weak pull-up.
NAND_WP	I/O		NAND Write Protect	RGMII1 Receive Data Bit 3	QSPI Slave Select 2	General Purpose IO Bit 27	If unused, program it in the Quartus II software as an input with a weak pull-up.
BOOTSEL2 (BSEL2)/ NAND_WE	I/O	BOOTSEL2 (BSEL2) During a cold reset this signal is sampled as a boot select input.	NAND Write Enable	QSPI Slave Select 1		General Purpose IO Bit 28	Connect a pull-up or pull-down resistor to VCCIO such as 4.7-kΩ - 10-kΩ to select the desired boot select values. Refer to the Booting and Configuration appendix in the Arria V Device Handbook for Boot Select values. This resistor will not interfere with the slow speed interface signals that could share this pin.
QSPI_IO0	I/O		QSPI Data IO Bit 0		USB 1 Clock	General Purpose IO	If unused, program it in the Quartus II software as an input with a weak pull-up.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
						Bit 29	
QSPI_IO1	I/O		QSPI Data IO Bit 1		USB1 Stop Data	General Purpose IO Bit 30	If unused, program it in the Quartus II software as an input with a weak pull-up.
QSPI_IO2	I/O		QSPI Data IO Bit 2		USB1 Direction	General Purpose IO Bit 31	If unused, program it in the Quartus II software as an input with a weak pull-up.
QSPI_IO3	I/O		QSPI Data IO Bit 3		USB1 Next Data	General Purpose IO Bit 32	If unused, program it in the Quartus II software as an input with a weak pull-up.
BOOTSEL1 (BSEL1)/ QSPI_SS0	I/O	BOOTSEL1 (BSEL1) During a cold reset this signal is sampled as a boot select input.	QSPI Slave Select 0			General Purpose IO Bit 33	Connect a pull-up or pull-down resistor to VCCIO such as 4.7-kΩ - 10-kΩ to select the desired boot select values. Refer to the Booting and Configuration appendix in the Arria V Device Handbook for Boot Select values. This resistor will not interfere with the slow speed interface signals that could share this pin.
QSPI_CLK	I/O		QSPI Clock			General Purpose IO Bit 34	When configured as the QSPI Clock and if single memory topology is used, connect a 50 Ω series termination resistor near this Arria V SoC FPGA device pin. For other topologies use a 25 Ω resistor. If unused, program it in the Quartus II software as an input with a weak pull-up.
QSPI_SS1	I/O		QSPI Slave Select 1			General Purpose IO Bit 35	If unused, program it in the Quartus II software as an input with a weak pull-up.
SDMMC_CMD	I/O		SDMMC Command Line	USB0 Data Bit 0		General Purpose IO Bit 36	If unused, program it in the Quartus II software as an input with a weak pull-up. If the pin is connected to a SD/MMC flash device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
SDMMC_PWREN	I/O		SDMMC Power Enable	USB0 Data Bit 1		General Purpose IO Bit 37	If unused, program it in the Quartus II software as an input with a weak pull-up.
SDMMC_D0	I/O		SDMMC Data Bit 0	USB0 Data Bit 2		General Purpose IO Bit 38	If unused, program it in the Quartus II software as an input with a weak pull-up. If the pin is connected to a SD/MMC flash device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
SDMMC_D1	I/O		SDMMC Data Bit 1	USB0 Data Bit 3		General Purpose IO Bit 39	If unused, program it in the Quartus II software as an input with a weak pull-up. If the pin is connected to a SD/MMC flash device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
SDMMC_D4	I/O		SDMMC Data Bit 4	USB0 Data Bit 4		General Purpose IO Bit 40	If unused, program it in the Quartus II software as an input with a weak pull-up. If the pin is connected to a SD/MMC flash device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
SDMMC_D5	I/O		SDMMC Data Bit 5	USB0 Data Bit 5		General Purpose IO Bit 41	If unused, program it in the Quartus II software as an input with a weak pull-up. If the pin is connected to a SD/MMC flash device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
SDMMC_D6	I/O		SDMMC Data Bit 6	USB0 Data Bit 6		General Purpose IO Bit 42	If unused, program it in the Quartus II software as an input with a weak pull-up. If the pin is connected to a SD/MMC flash device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
SDMMC_D7	I/O		SDMMC Data Bit 7	USB0 Data Bit 7		General Purpose IO Bit 43	If unused, program it in the Quartus II software as an input with a weak pull-up. If the pin is connected to a SD/MMC flash device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
HPS_GPIO44	I/O			USB0 Clock		General Purpose IO	If unused, program it in the Quartus II software as an input with a weak pull-up.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
						Bit 44	
SDMMC_CCLK_OUT	I/O		SDMMC Clock out	USB0 Stop Data		General Purpose IO Bit 45	If unused, program it in the Quartus II software as an input with a weak pull-up.
SDMMC_D2	I/O		SDMMC Data Bit 2	USB0 Direction		General Purpose IO Bit 46	If unused, program it in the Quartus II software as an input with a weak pull-up. If the pin is connected to a SD/MMC flash device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
SDMMC_D3	I/O		SDMMC Data Bit 3	USB0 Next Data		General Purpose IO Bit 47	If unused, program it in the Quartus II software as an input with a weak pull-up. If the pin is connected to a SD/MMC flash device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. See note 15.
TRACE_CLK	I/O		Trace Clock			General Purpose IO Bit 48	If unused, program it in the Quartus II software as an input with a weak pull-up.
TRACE_D0	I/O		Trace Data Bit 0	SPIS0 Clock	UART0 Receive Data	General Purpose IO Bit 49	If unused, program it in the Quartus II software as an input with a weak pull-up.
TRACE_D1	I/O		Trace Data Bit 1	SPIS0 Master Out Slave In	UART0 Transmit	General Purpose IO Bit 50	If unused, program it in the Quartus II software as an input with a weak pull-up.
TRACE_D2	I/O		Trace Data Bit 2	SPIS0 Master In Slave Out	I2C1 Serial Data	General Purpose IO Bit 51	If unused, program it in the Quartus II software as an input with a weak pull-up.
TRACE_D3	I/O		Trace Data Bit 3	SPIS0 Slave Select 0	I2C1 Serial clock	General Purpose IO Bit 52	If unused, program it in the Quartus II software as an input with a weak pull-up.
TRACE_D4	I/O		Trace Data Bit 4	SPIS1 Clock		General Purpose IO Bit 53	If unused, program it in the Quartus II software as an input with a weak pull-up.
TRACE_D5	I/O		Trace Data Bit 5	SPIS1 Master Out Slave In		General Purpose IO Bit 54	If unused, program it in the Quartus II software as an input with a weak pull-up.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
TRACE_D6	I/O		Trace Data Bit 6	SPIS1 Slave Select Input	I2C0 Serial Data	General Purpose IO Bit 55	If unused, program it in the Quartus II software as an input with a weak pull-up.
TRACE_D7	I/O		Trace Data Bit 7	SPIS1 Master In Slave Out	I2C0 Serial clock	General Purpose IO Bit 56	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIM0_CLK	I/O		SPIM0 Clock	I2C1 Serial Data	UART 0 Clear to Send	General Purpose IO Bit 57	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIM0_MOSI	I/O		SPIM0 Master Out Slave In	I2C1 Serial clock	UART0 Request to Send	General Purpose IO Bit 58	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIM0_MISO	I/O		SPIM0 Master In Slave Out		UART1 Clear to Send	General Purpose IO Bit 59	If unused, program it in the Quartus II software as an input with a weak pull-up.
BOOTSEL0 (BSEL0)/SPIM0_SS0	I/O	BOOTSEL0 (BSEL0) During a cold reset this signal is sampled as a boot select input.	SPIM0 Slave Select 0		UART1 Request to Send	General Purpose IO Bit 60	Connect a pull-up or pull-down resistor to VCCIO such as 4.7-kΩ - 10-kΩ to select the desired boot select values. Refer to the Booting and Configuration appendix in the Arria V Device Handbook for Boot Select values. This resistor will not interfere with the slow speed interface signals that could share this pin.
UART0_RX	I/O		UART0 Receive		SPIM0 Slave Select 1	General Purpose IO Bit 61	If unused, program it in the Quartus II software as an input with a weak pull-up.
CLOCKSEL1 (CSEL1)/UART0_TX	I/O	CLOCKSEL1 (CSEL1) During a cold reset this signal is sampled as a	UART0 Transmit		SPIM1 Slave Select 1	General Purpose IO Bit 62	Connect a pull-up or pull-down resistor such as 4.7-kΩ - 10-kΩ to select the desired clock select values. Refer to the Booting and Configuration appendix in the Arria V Device Handbook for Clock Select values. This resistor will not interfere with the slow speed interface

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
		clock select input.					signals that could share this pin.
I2C0_SDA	I/O		I2C0 Serial Data	UART1 Receive	SPIM1 Clock	General Purpose IO Bit 63	If unused, program it in the Quartus II software as an input with a weak pull-up.
I2C0_SCL	I/O		I2C0 Serial Clock	UART1 Transmit	SPIM1 Master Out Slave In	General Purpose IO Bit 64	If unused, program it in the Quartus II software as an input with a weak pull-up.
UART0_RX	I/O			UART0 Receive	SPIM1 Master In Slave Out	General Purpose IO Bit 65	If unused, program it in the Quartus II software as an input with a weak pull-up. See Note 14.
CLOCKSEL0 (CSEL0)/UART0_TX	I/O	CLOCKSEL0 (CSEL0) During a cold reset this signal is sampled as a clock select input.		UART0 Transmit	SPIM1 Slave Select 0	General Purpose IO Bit 66	Connect a pull-up or pull-down resistor such as 4.7-kΩ - 10-kΩ to select the desired clock select values. Refer to the Booting and Configuration appendix in the Arria V Device Handbook for Clock Select values. This resistor will not interfere with the slow speed interface signals that could share this pin. See Note 14.
RGMII1_TX_CLK	I/O		RGMII1_TX_CLK			General Purpose I/O Bit 48	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_TXD0	I/O		RGMII1_TXD0			General Purpose I/O Bit 49	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_TXD1	I/O		RGMII1_TXD1			General Purpose I/O Bit 50	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_TX_CTL	I/O		RGMII1_TX_CTL			General Purpose I/O Bit 51	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_RXD0	I/O		RGMII1_RXD0			General Purpose I/O Bit 52	If unused, program it in the Quartus II software as an input with a weak pull-up.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
RGMII1_RXD1	I/O		RGMII1_RXD1			General Purpose I/O Bit 53	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_MDIO	I/O		RGMII1_MDIO	SPIM0_CLK	SPIS0_CLK	General Purpose I/O Bit 54	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_MDC	I/O		RGMII1_MDC	SPIM0_MOSI	SPIS0_MOSI	General Purpose I/O Bit 55	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_TXD2	I/O		RGMII1_TXD2	SPIM0_MISO	SPIS0_MISO	General Purpose I/O Bit 56	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_TXD3	I/O		RGMII1_TXD3	SPIM0_SS0	SPIS0_SS0	General Purpose I/O Bit 57	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_RX_CLK	I/O		RGMII1_RX_CLK	SPIS1_CLK	SPIM1_CLK	General Purpose I/O Bit 58	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_RX_CTL	I/O		RGMII1_RX_CTL	SPIS1_MOSI	SPIM1_MOSI	General Purpose I/O Bit 59	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_RXD2	I/O		RGMII1_RXD2	SPIS1_MISO	SPIM1_MISO	General Purpose I/O Bit 60	If unused, program it in the Quartus II software as an input with a weak pull-up.
RGMII1_RXD3	I/O		RGMII1_RXD3	SPIS1_SS0	SPIM1_SS0	General Purpose I/O Bit 61	If unused, program it in the Quartus II software as an input with a weak pull-up.
UART1_RX	I/O		UART1_RX	SPIM1_SS1		General Purpose I/O Bit 62	If unused, program it in the Quartus II software as an input with a weak pull-up.
UART1_TX	I/O		UART1_TX	SPIM0_CLK		General Purpose I/O Bit 63	If unused, program it in the Quartus II software as an input with a weak pull-up.
I2C1_SDA	I/O		I2C1_SDA	SPIM0_MOSI		General Purpose I/O Bit 64	If unused, program it in the Quartus II software as an input with a weak pull-up.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V HPS Pin Name	Pin Type (1st and 2nd Function)	Pin Description					Connection Guidelines
I2C1_SCL	I/O		I2C1_SCL	SPIM0_MISO		General Purpose I/O Bit 65	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIM0_SS0	I/O			SPIM0_SS0		General Purpose I/O Bit 66	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIS0_CLK	I/O		SPIS0_CLK	SPIM_SS1		General Purpose I/O Bit 67	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIS0_MOSI	I/O		SPIS0_MOSI			General Purpose I/O Bit 68	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIS0_MISO	I/O		SPIS0_MISO			General Purpose I/O Bit 69	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIS0_SS0	I/O		SPIS0_SS0			General Purpose I/O Bit 70	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIS1_CLK	I/O		SPIS1_CLK	SPIM1_CLK		General Purpose I/O Bit 67	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIS1_MOSI	I/O		SPIS1_MOSI	SPIM1_MOSI		General Purpose I/O Bit 68	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIS1_MISO	I/O		SPIS1_MISO	SPIM1_MISO		General Purpose I/O Bit 69	If unused, program it in the Quartus II software as an input with a weak pull-up.
SPIS1_SS0	I/O		SPIS1_SS0	SPIM1_SS0		General Purpose I/O Bit 70	If unused, program it in the Quartus II software as an input with a weak pull-up.

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Notes to Arria V ST and SX Pin Connection Guidelines

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are based on the Arria V ST and SX device variants.
2. Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage droop requirements of the device or supply. Then, decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling.
3. Use the Arria V Early Power Estimator to determine the current requirements for VCC and other power supplies.
4. These supplies may share power planes across multiple Arria V devices.
5. Example 6, Figure 6, Example 7, and Figure 7 illustrate the power supply sharing guidelines for Arria V ST –I3 devices. Example 8, Figure 8, Example 9, and Figure 9 illustrate the power supply sharing guidelines for Arria V ST –I5 devices.
6. Power pins should not share breakout vias from the BGA. Each ball on the BGA must have its own dedicated breakout via. VCC and VCCP must not share breakout vias.
7. Low Noise Switching Regulator - a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response. The switching frequency range is not an Altera requirement. However, Altera does require the Line Regulation and Load Regulation meet the following specifications:
   - Line Regulation < 0.4%
   - Load Regulation < 1.2%

   You have the option to use a linear regulator depending on your design and your system’s power and thermal budget considerations.
8. The number of modular I/O banks on Arria V devices depends on the device density. For the indexes available for a specific device, refer to the I/O Bank section in the Arria V handbook.
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires that the AC-coupling capacitor is placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. All transceiver power pins on the same side of the device must be connected either to the required supply or to GND. When ALL transceiver channels on the same side are unused, you have the option to connect all of the transceiver power pins on the same side of the device to GND or to the required supply.
11. For item [#], refer to the device pin table for the pin-out mapping.
12. The peripheral pins are programmable through pin multiplexors. Each pin may have up to four functions. Configuraton of each pin is done during HPS configuration.
13. Peripheral I/O pins and GPIO pins that are configured as Loan I/O drive '1' before FPGA is being configured.
14. There are two sets of pins that are labeled UART0_RX and UART_TX. The pin mux will determine how the pins are used.
15. When using SD card, there is an existing 50-kΩ pull-up on SDMMC Data Bit 3 that can be disabled using SET_CLR_CARD_DETECT (ACMD42) command. This does not apply to eMMC flash.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V GX –C4, -C5, -I5, and –C6 <= 3.2 Gbps

Example 1. Power Supply Sharing Guidelines for Arria V GX –C4, -C5, -I5, and –C6 with Transceiver Data Rates <= 3.2 Gbps

Example Requiring 3 Power Regulators

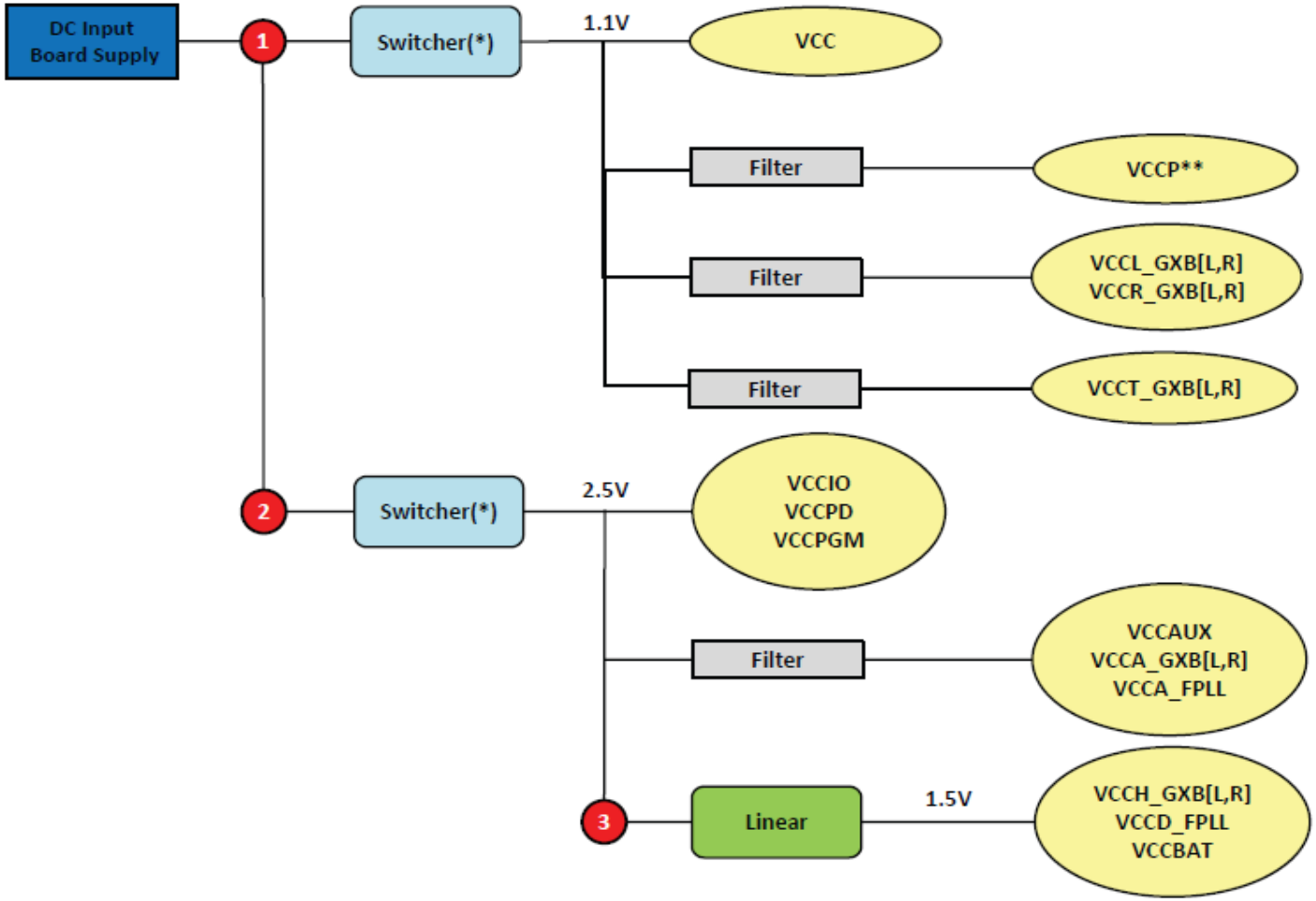
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP, VCCL_GXB, VCCR_GXB and VCCT_GXB with VCC with proper isolation filters. For all 5AGXA1, 5AGXA3, 5AGXA5, 5AGXA7, 5AGXB1 and 5AGXB3 devices excluding ES devices, VCCR_GXB, VCCT_GXB, and VCCL_GXB should be combined together and share one isolation filter.
VCCP					Isolate	
VCCL_GXB[L,R]					Isolate	
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCC_AUX		2.5			Isolate	May be able to share VCC_AUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCH_GXB[L,R]	3	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GX device is provided in Figure 1.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 1. Example Power Supply Block Diagram for Arria V GX –C4, -C5, -I5, and –C6 with Transceiver Data Rates <= 3.2 Gbps



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping VCC and VCCP power rails isolated from each and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V GX –C4, -C5, and -I5 > 3.2 Gbps

Example 2. Power Supply Sharing Guidelines for Arria V GX –C4, - C5, and –I5 with Tranceiver Data Rates > 3.2 Gbps

Example Requiring 4 Power Regulators

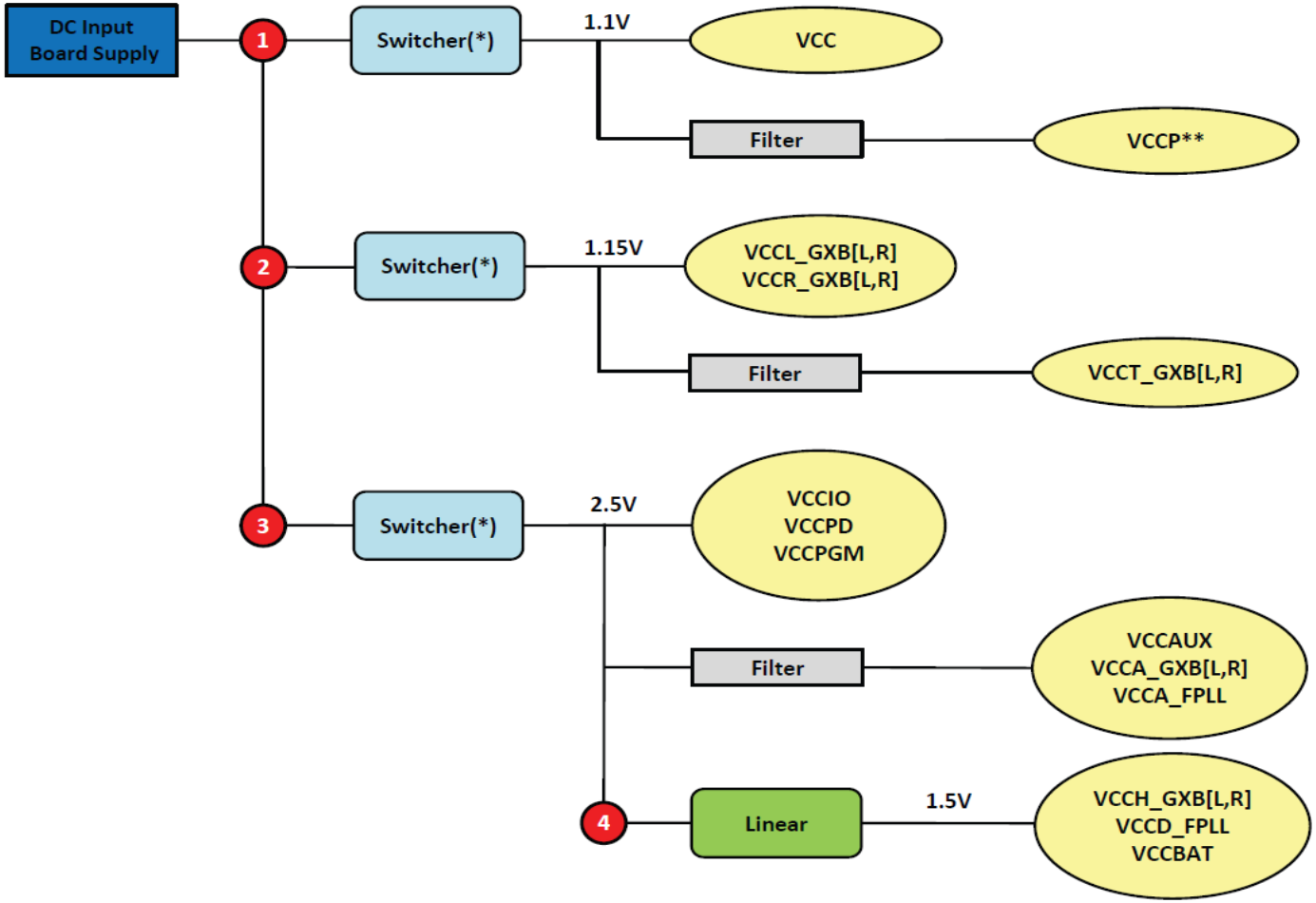
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters. For all 5AGXA1, 5AGXA3, 5AGXA5, 5AGXA7, 5AGXB1 and 5AGXB3 devices excluding ES devices, VCCR_GXB, VCCT_GXB, and VCCL_GXB should be combined together and share one isolation filter.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCC_AUX		2.5			Isolate	May be able to share VCC_AUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GX is provided in Figure 2.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 2. Example Power Supply Block Diagram for Arria V GX –C4, - C5, and –I5 with Transceiver Data Rates > 3.2 Gbps



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

** Altera recommends keeping VCC and VCCP power rails isolated from each and on separate layers of the PCB.

Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V GX –I3

Example 3. Power Supply Sharing Guidelines for Arria V GX –I3

Example Requiring 4 Power Regulators

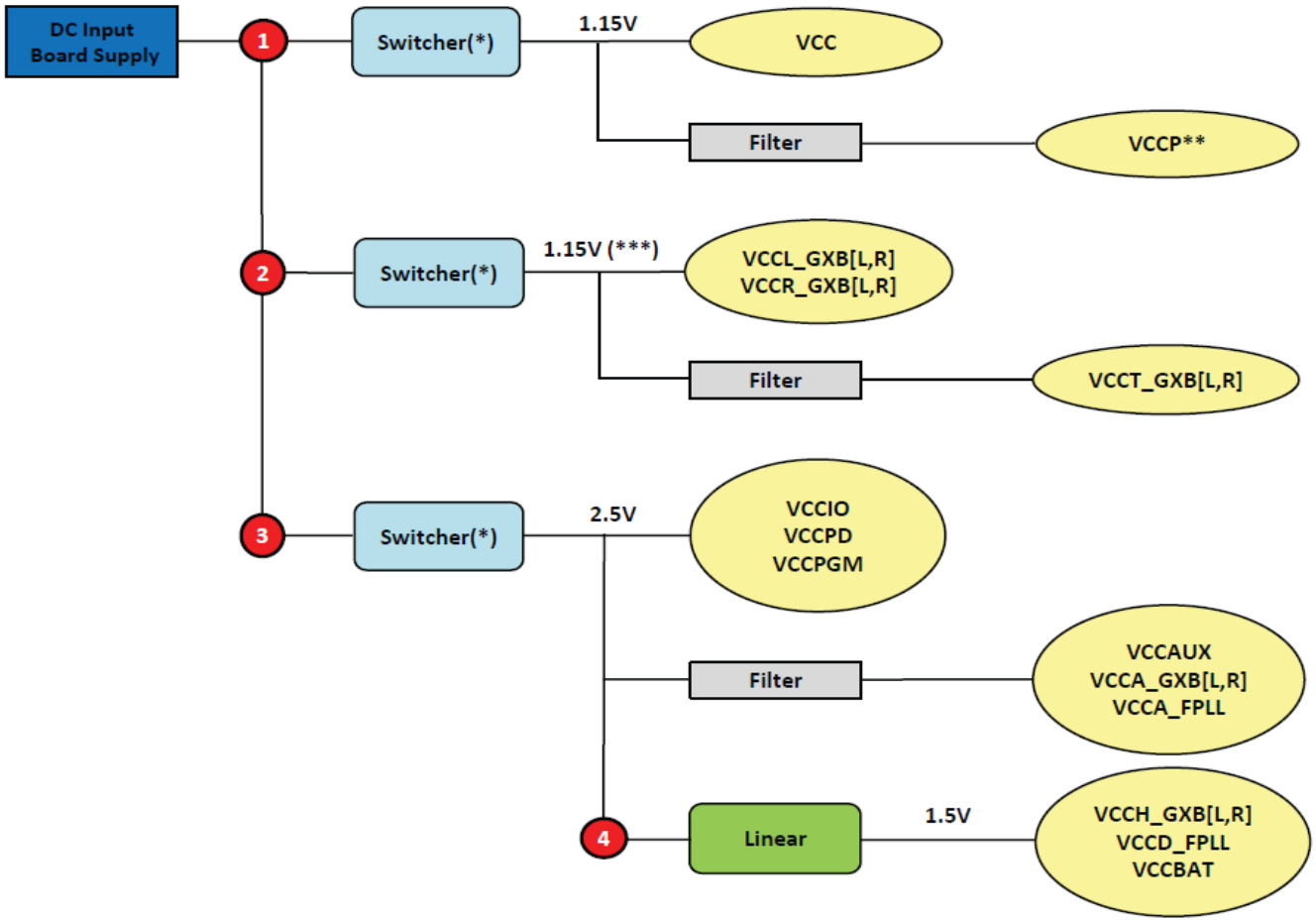
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.15 (**)	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters. For all 5AGXA1, 5AGXA3, 5AGXA5, 5AGXA7, 5AGXB1 and 5AGXB3 devices excluding ES devices, VCCR_GXB, VCCT_GXB, and VCCL_GXB should be combined together and share one isolation filter.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCC_AUX		2.5			Isolate	May be able to share VCC_AUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
(**) VCCL_GXB[L,R], VCCR_GXB[L,R], and VCCT_GXB[L,R] can be 1.1V when the transceiver data rate is <= 3.2 Gbps.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GX –I3 is provided in Figure 3.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 3. Example Power Supply Block Diagram for Arria V GX –I3



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
*** VCCL_GXB[L,R], VCCR_GXB[L,R], and VCCT_GXB[L,R] can be 1.1V when the transceiver data rate is <= 3.2Gbps.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V GT –I3

Example 4. Power Supply Sharing Guidelines for Arria V GT –I3

Example Requiring 4 Power Regulators

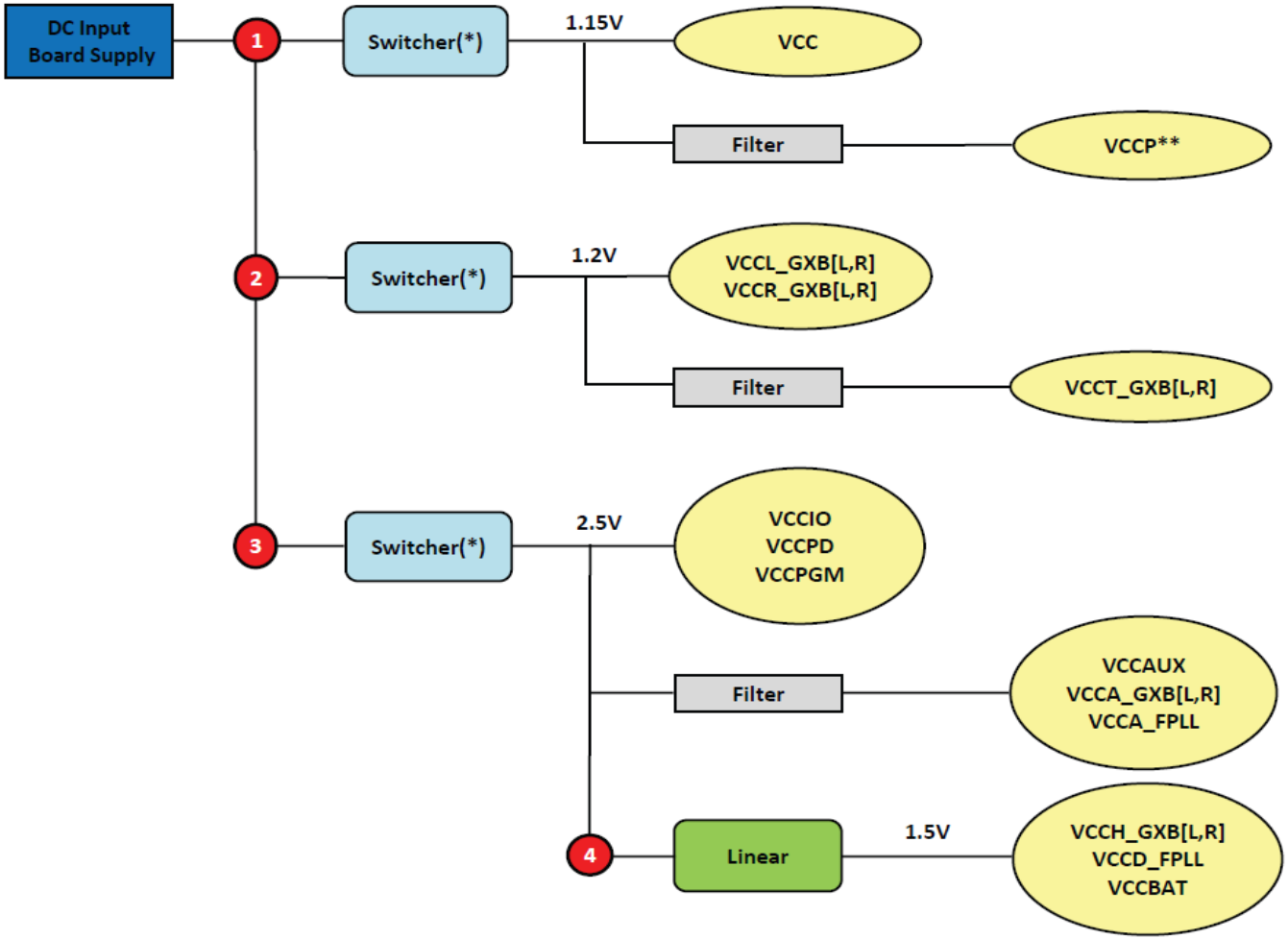
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCP	1	1.15	± 30mV	Switcher (*)	Share Isolate	May be able to share VCCP with VCC with proper isolation filters.
VCCL_GXB[L,R] VCCR_GXB[L,R] VCCT_GXB[L,R]	2	1.2	± 30mV	Switcher (*)	Share Isolate	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters. For all 5AGTD3 devices excluding ES devices, VCCR_GXB, VCCT_GXB, and VCCL_GXB should be combined together and share one isolation filter.
VCCIO VCCPD VCCPGM	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCC_AUX VCCA_GXB[L,R] VCCA_FPLL		2.5			Isolate	May be able to share VCC_AUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCH_GXB[L,R] VCCD_FPLL VCCBAT	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GT –I3 is provided in Figure 4.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 4. Example Power Supply Block Diagram for Arria V GT –I3



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V GT –I5

Example 5. Power Supply Sharing Guidelines for Arria V GT –I5

Example Requiring 4 Power Regulators

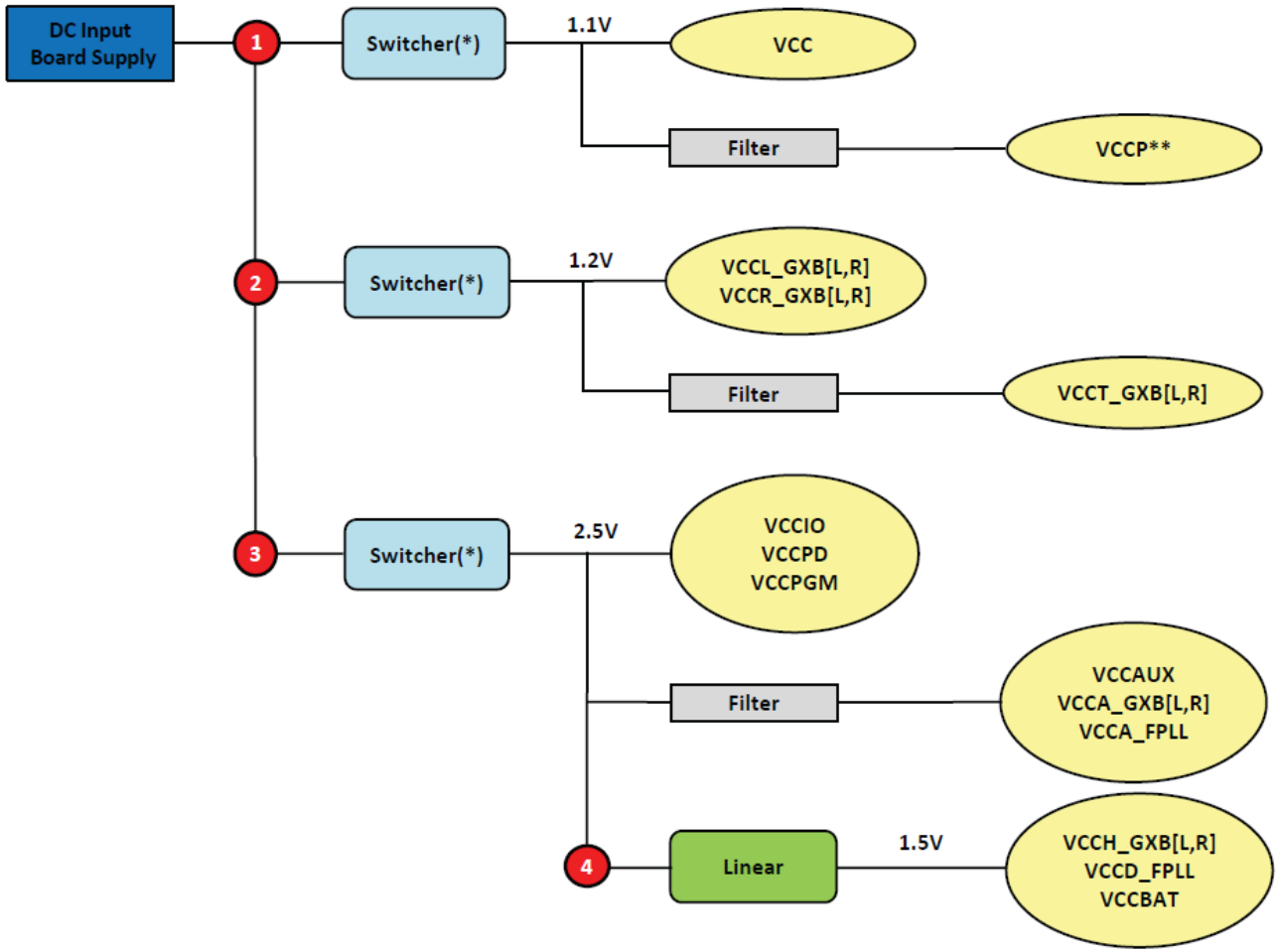
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.2	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters. For all 5AGTD3 devices excluding ES devices, VCCR_GXB, VCCT_GXB, and VCCL_GXB should be combined together and share one isolation filter.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCC_AUX		2.5			Isolate	May be able to share VCC_AUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GT –I5 is provided in Figure 5.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 5. Example Power Supply Block Diagram for Arria V GT –I5



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V ST –I3

Example 6. Power Supply Sharing Guidelines for Arria V ST –I3

Example Requiring 4 Power Regulators (FPGA & HPS Share Power)

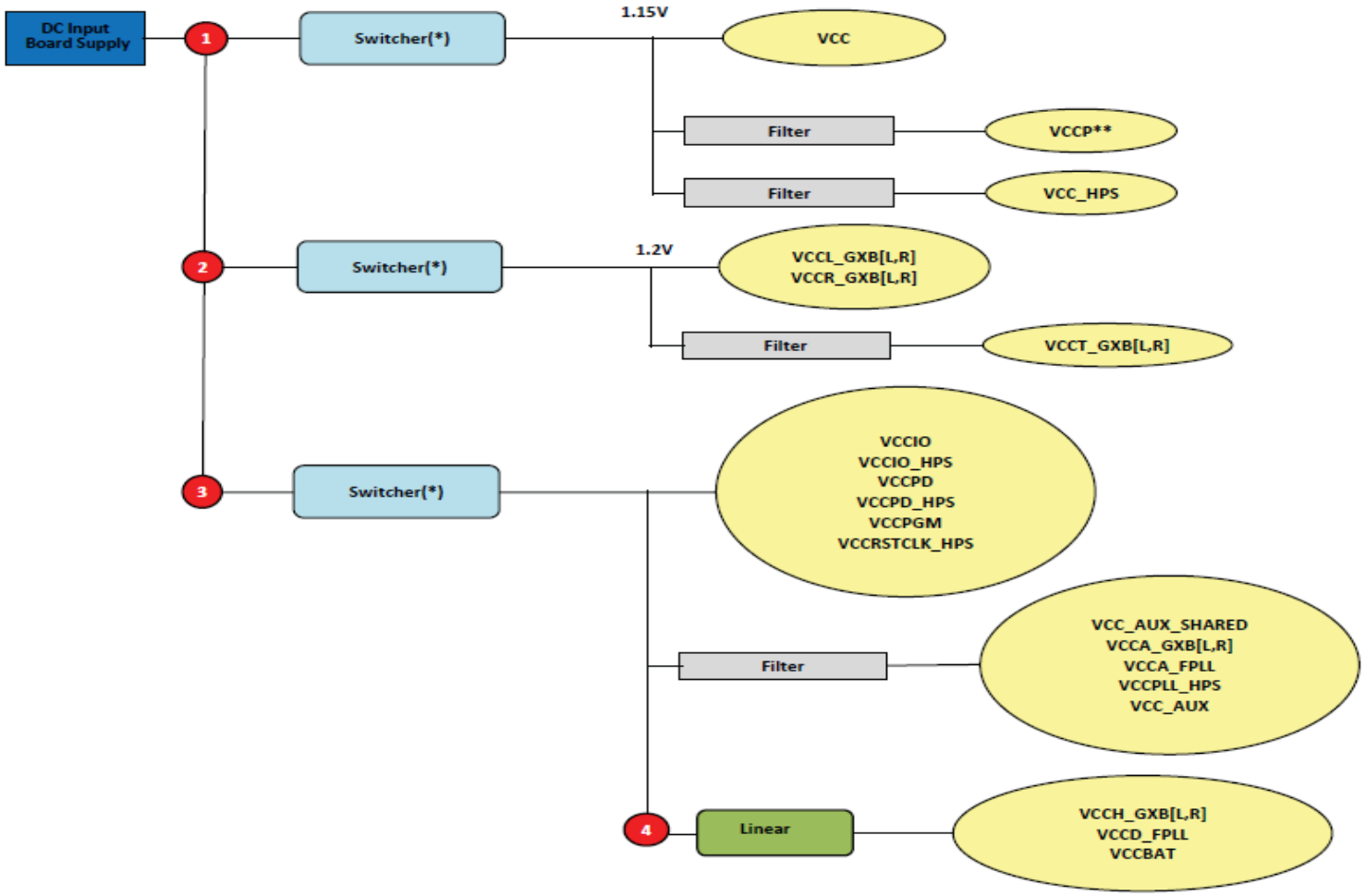
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCP with same regulator as VCC with proper isolation filters.
VCCP					Isolate	
VCC_HPS					Isolate	May be able to share VCC_HPS with same regulator as VCC with proper isolation filters.
VCCL_GXB[L,R]	2	1.2	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require the same voltage level, and when the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCIO_HPS						
VCCPD						
VCCPD_HPS						
VCCPGM						
VCCRSTCLK_HPS						
VCC_AUX_SHARED		2.5			Isolate	VCC_AUX_SHARED must always be powered up for the HPS operation. VCC_AUX must always be powered up for the PLL operation. VCCA_FPLL, VCCA_GXB and VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED, VCCA_GXB, VCCA_FPLL, VCCPLL_HPS and VCC_AUX with the same regulator as VCCIO, VCCIO_HPS, VCCPD, VCCPD_HPS, VCCPGM and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCPLL_HPS						
VCC_AUX						
VCCBAT	4	Varies	± 5%	Linear	Share if 1.5V	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices. If you use the design security feature, VCCBAT should be powered by battery with voltage range as listed in the device datasheet.
VCCH_GXB[L,R]		1.5				
VCCD_FPLL						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V ST –I3 is provided in Figure 6.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 6. Example Power Supply Block Diagram for Arria V ST –I3 (FPGA & HPS Share Power)



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.

Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V ST –I3

Example 7. Power Supply Sharing Guidelines for Arria V ST –I3

Example Requiring 6 Power Regulators (FPGA & HPS Do Not Share Power)

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.2	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCA_GXB[L,R]		2.5			Isolate	VCC_AUX must always be powered up for the PLL operation. May be able to share VCCA_GXB, VCCA_FPLL and VCC_AUX with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_FPLL						
VCC_AUX						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

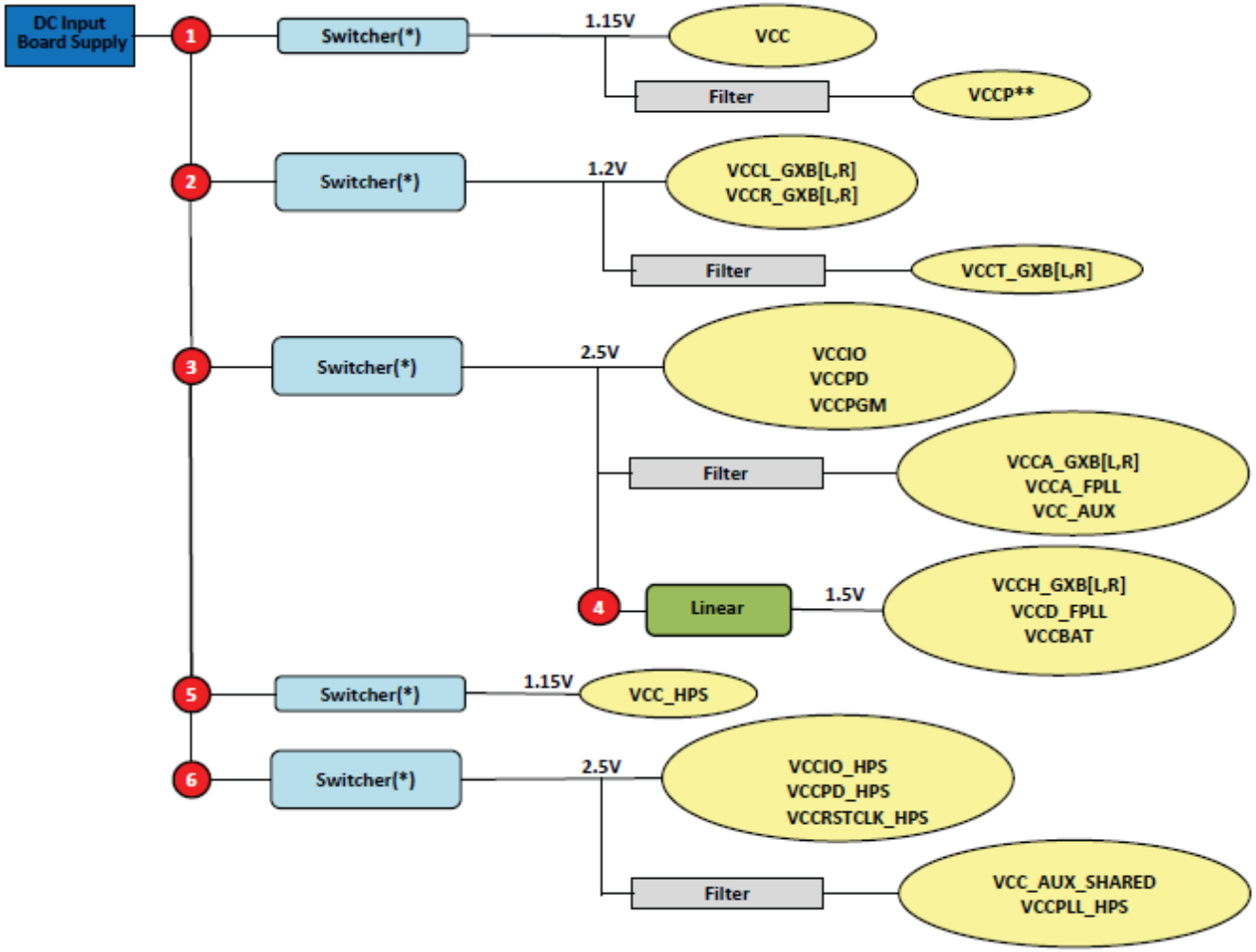
<table>
<tr><th>Power Pin Name</th><th>Regulator Count</th><th>Voltage Level (V)</th><th>Supply Tolerance</th><th>Power Source</th><th>Regulator Sharing</th><th>Notes</th></tr>
<tr><td>VCC_HPS</td><td>5</td><td>1.15</td><td>± 30mV</td><td>Switcher (*)</td><td>Isolate</td><td>Separate regulator allows the FPGA to be powered off while the HPS is powered on.
VCC_HPS should be placed at power layers nearest to the Arria V device.</td></tr>
<tr><td>VCCIO_HPS</td><td rowspan="4">6</td><td rowspan="3">Varies</td><td rowspan="4">± 5%</td><td rowspan="4">Switcher (*)</td><td rowspan="3">Share if 2.5V</td><td rowspan="3">If all of these supplies require the same voltage level, and when the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design.
Use the EPE tool to assist in determining the power required for your specific design.</td></tr>
<tr><td>VCCPD_HPS</td></tr>
<tr><td>VCCRSTCLK_HPS</td></tr>
<tr><td>VCC_AUX_SHARED</td><td rowspan="2">2.5</td><td rowspan="2">Isolate</td><td rowspan="2">VCC_AUX_SHARED must always be powered up for the HPS operation. VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED and VCCPLL_HPS with the same regulator as VCCIO_HPS, VCCPD_HPS, and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter.</td></tr>
<tr><td>VCCPLL_HPS</td></tr>
</table>

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V ST –I3 is provided in Figure 7.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 7. Example Power Supply Block Diagram for Arria V ST –I3 (FPGA & HPS Do Not Share Power)



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V ST –I5

Example 8. Power Supply Sharing Guidelines for Arria V ST –I5

Example Requiring 4 Power Regulators (FPGA & HPS Share Power)

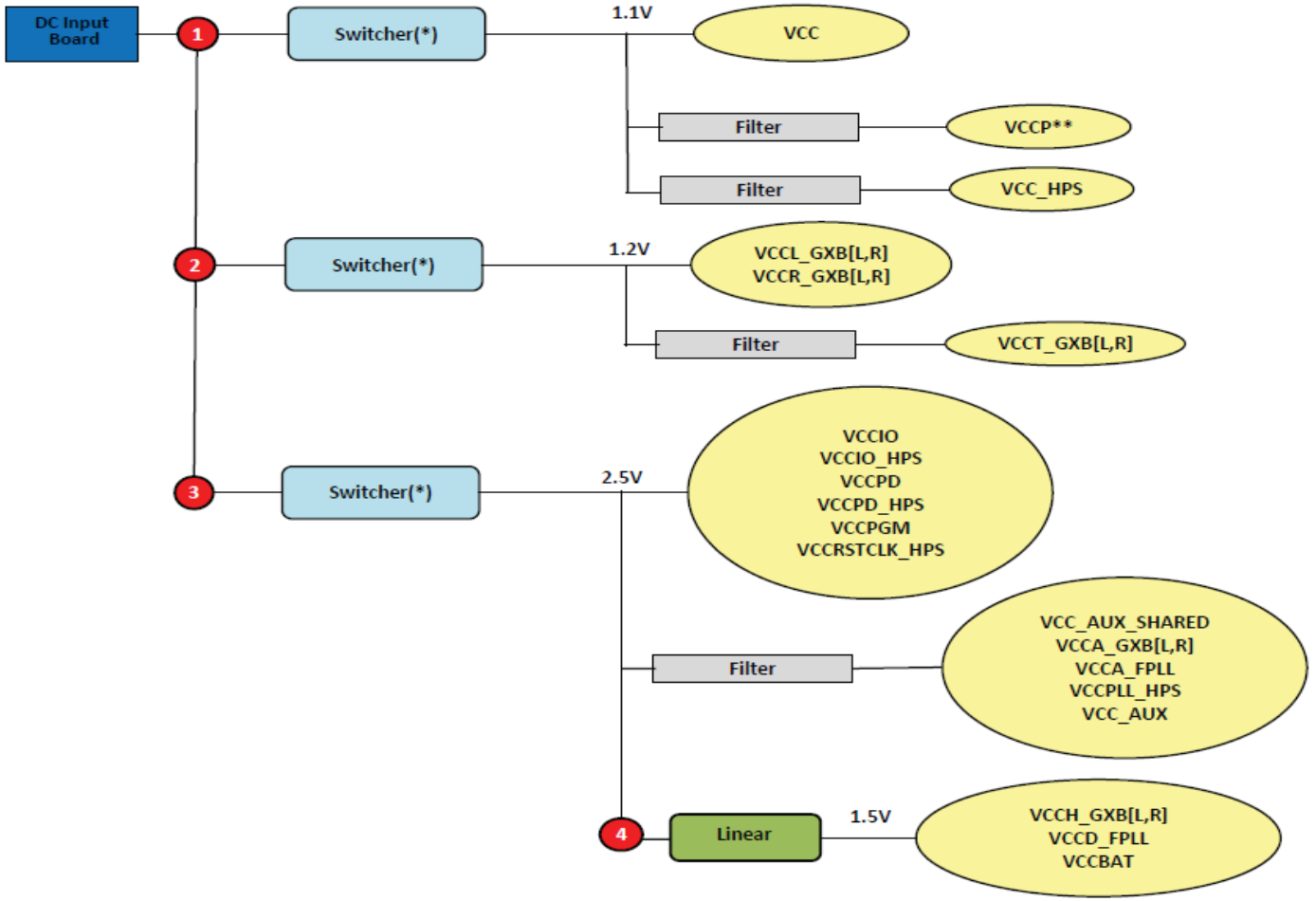
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP, VCC_HPS with same regulator as VCC with proper isolation filters.
VCCP					Isolate	
VCC_HPS					Isolate	
VCCL_GXB[L,R]	2	1.2	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require the same voltage level, and when the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCIO_HPS						
VCCPD						
VCCPD_HPS						
VCCPGM						
VCCRSTCLK_HPS						
VCC_AUX_SHARED		2.5			Isolate	VCC_AUX_SHARED must always be powered up for the HPS operation. VCC_AUX must always be powered up for the PLL operation. VCCA_FPLL, VCCA_GXB and VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED, VCCA_GXB, VCCA_FPLL, VCCPLL_HPS and VCC_AUX with the same regulator as VCCIO, VCCIO_HPS, VCCPD, VCCPD_HPS, VCCPGM and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCPLL_HPS						
VCC_AUX						
VCCBAT	4	Varies	± 5%	Linear	Share if 1.5V	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices. If you use the design security feature, VCCBAT should be powered by battery with voltage range as listed in the device datasheet.
VCCH_GXB[L,R]		1.5				
VCCD_FPLL						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V ST –I5 is provided in Figure 8.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 8. Example Power Supply Block Diagram for Arria V ST –I5 (FPGA & HPS Share Power)



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V ST –I5

Example 9. Power Supply Sharing Guidelines for Arria V ST –I5

Example Requiring 6 Power Regulators (FPGA & HPS Do Not Share Power)

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.2	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCA_GXB[L,R]		2.5			Isolate	VCC_AUX must always be powered up for the PLL operation. May be able to share VCCA_GXB, VCCA_FPLL and VCC_AUX with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_FPLL						
VCC_AUX						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						
VCC_HPS	5	1.1	± 30mV	Switcher (*)	Isolate	Separate regulator allows the FPGA to be powered off while the HPS is powered on. VCC_HPS should be placed at power layers nearest to the Arria V device.
VCCIO_HPS	6	Varies	± 5%	Switcher (*)	Share if	If all of these supplies require the same voltage level, and when the regulator selected satisfies

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

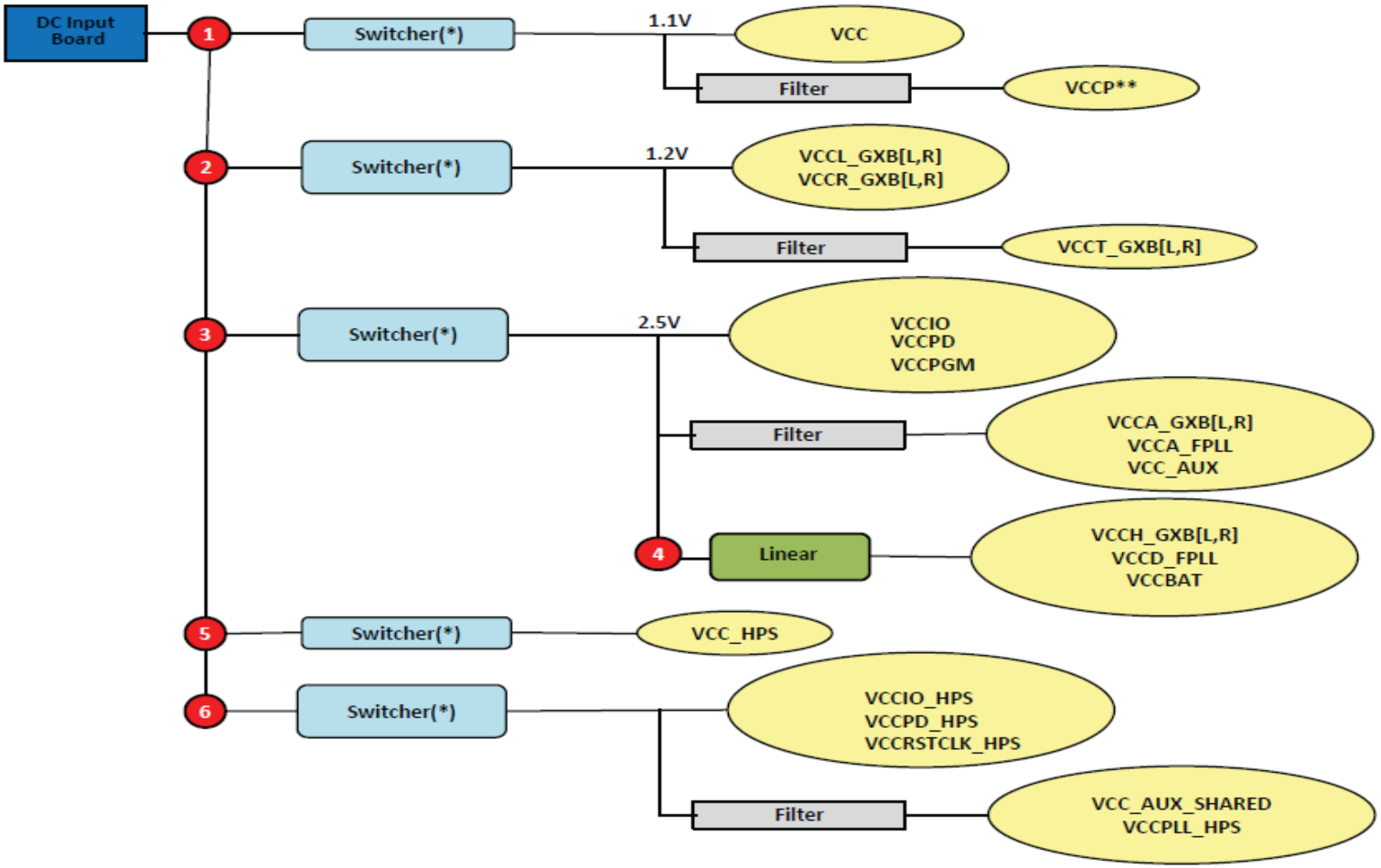
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCPD_HPS					2.5V	the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCRSTCLK_HPS						
VCC_AUX_SHARED		2.5			Isolate	VCC_AUX_SHARED must always be powered up for the HPS operation. VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED and VCCPLL_HPS with the same regulator as VCCIO_HPS, VCCPD_HPS, and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter.
VCCPLL_HPS						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V ST –I5 is provided in Figure 9.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 9. Example Power Supply Block Diagram for Arria V ST –I5 (FPGA & HPS Do Not Share Power)



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V SX –C4, C5, I5, and C6

Example 10. Power Supply Sharing Guidelines for Arria V SX –C4, C5, I5, and C6 with Transceiver Data Rate <= 3.2 Gbps

Example Requiring 4 Power Regulators (FPGA & HPS Share Power)

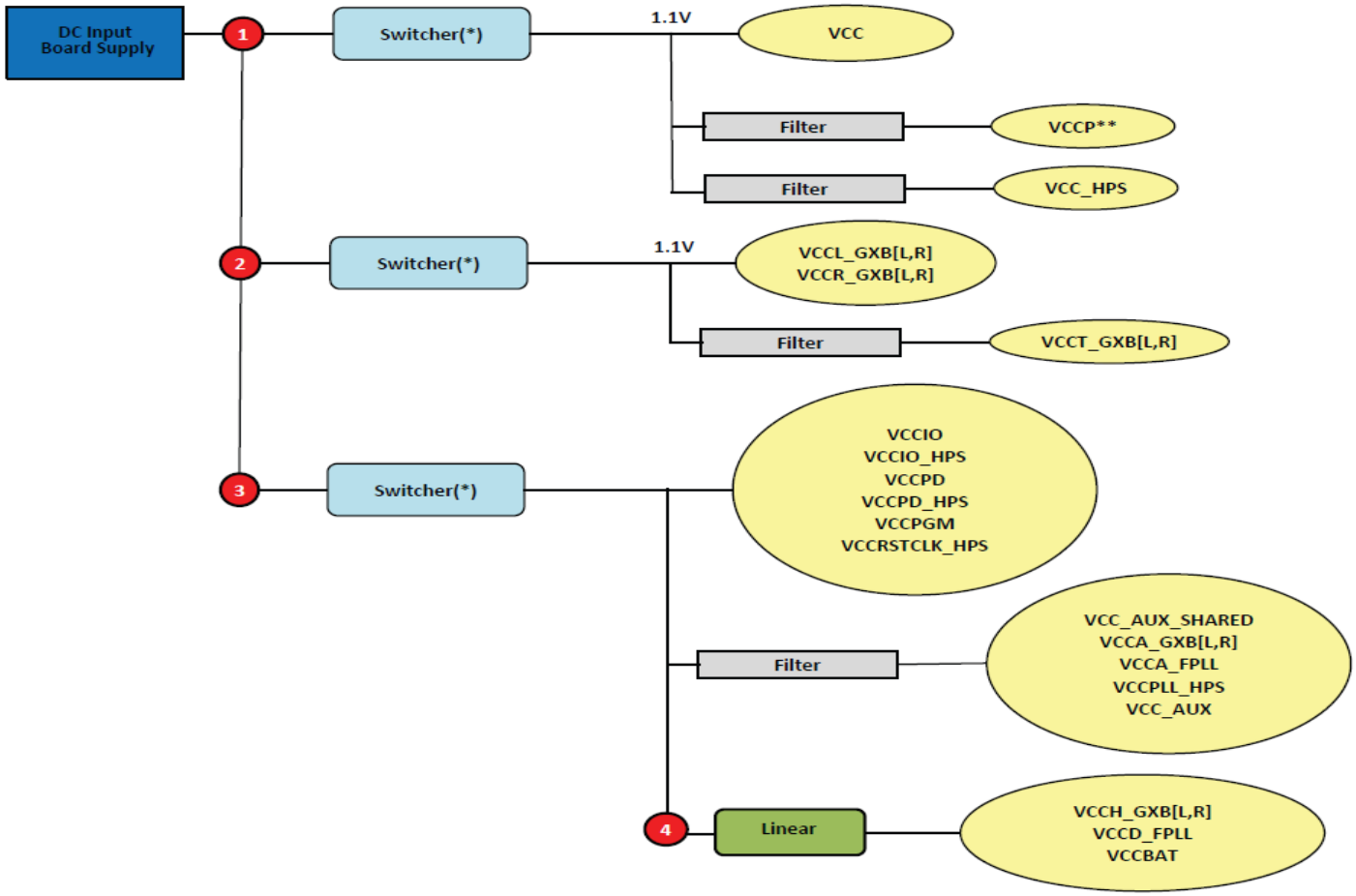
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP, VCC_HPS with same regulator as VCC with proper isolation filters.
VCCP					Isolate	
VCC_HPS					Isolate	
VCCL_GXB[L,R]	2	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require the same voltage level, and when the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCIO_HPS						
VCCPD						
VCCPD_HPS						
VCCPGM						
VCCRSTCLK_HPS						
VCC_AUX_SHARED		2.5			Isolate	VCC_AUX, VCCA_FPLL, VCCA_GXB, and VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED, VCCA_GXB, VCCA_FPLL, VCCPLL_HPS and VCC_AUX with the same regulator as VCCIO, VCCIO_HPS, VCCPD, VCCPD_HPS, VCCPGM and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCPLL_HPS						
VCC_AUX						
VCCBAT	4	Varies	± 5%	Linear	Share if 1.5V	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices. If you use the design security feature, VCCBAT should be powered by battery with voltage range as listed in the device datasheet.
VCCH_GXB[L,R]		1.5				
VCCD_FPLL						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V SX –C4, C5, I5, and C6 is provided in Figure 10.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 10. Example Power Supply Block Diagram for Arria V SX –C4, C5, I5, and C6 with Transceiver Data Rate <= 3.2 Gbps (FPGA & HPS Share Power)



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V SX –C4, C5, I5, and C6

Example 11. Power Supply Sharing Guidelines for Arria V SX –C4, C5, I5, and C6 with Transceiver Data Rate <= 3.2 Gbps

Example Requiring 6 Power Regulators (FPGA & HPS Do Not Share Power)

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCA_GXB[L,R]		2.5			Isolate	VCC_AUX must always be powered up for the PLL operation. May be able to share VCCA_GXB, VCCA_FPLL and VCC_AUX with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_FPLL						
VCC_AUX						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						
VCC_HPS	5	1.1	± 30mV	Switcher (*)	Isolate	Separate regulator allows the FPGA to be powered off while the HPS is powered on. VCC_HPS should be placed at power layers nearest to the Arria V device.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

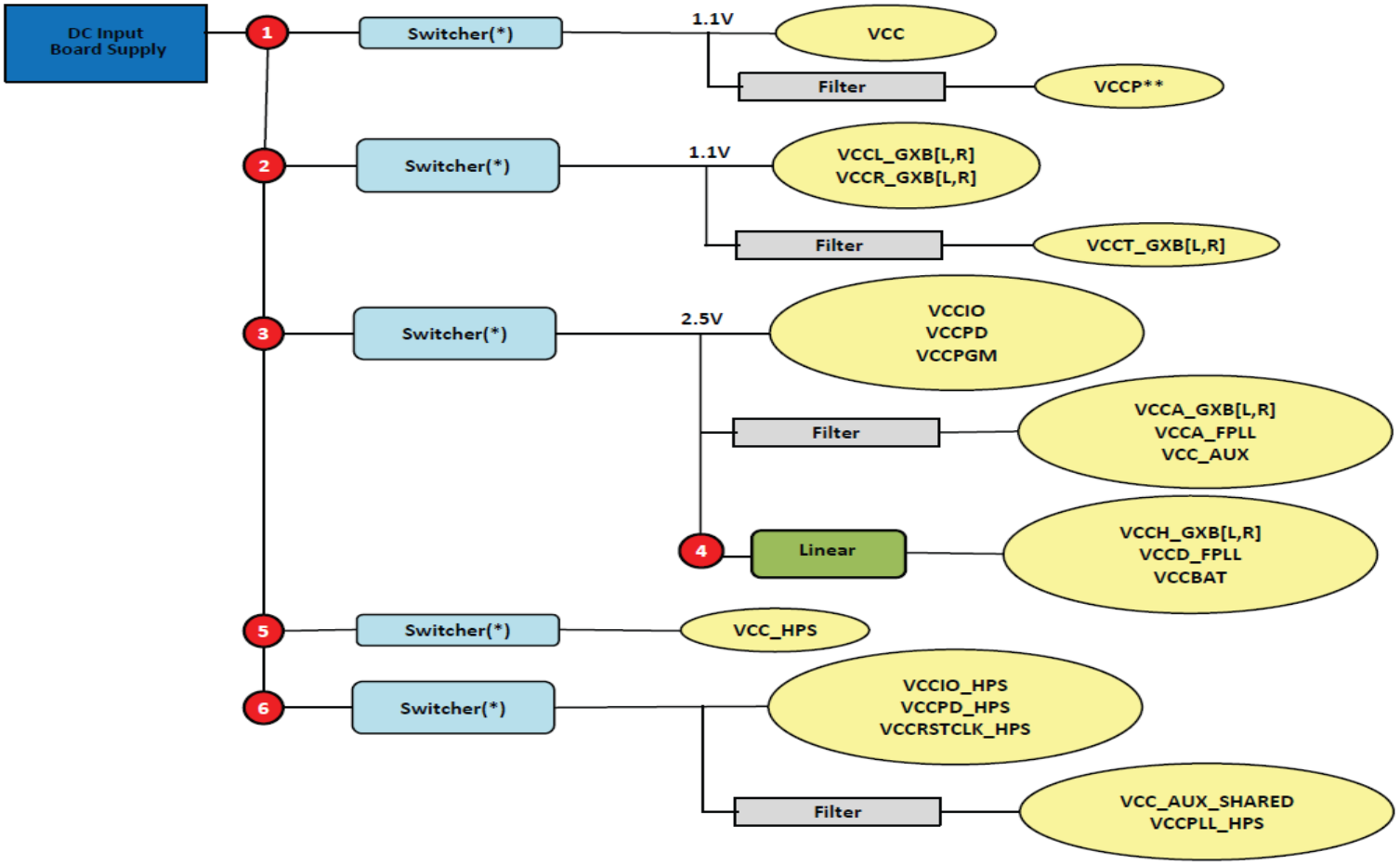
<table>
<tr><th>Power Pin Name</th><th>Regulator Count</th><th>Voltage Level (V)</th><th>Supply Tolerance</th><th>Power Source</th><th>Regulator Sharing</th><th>Notes</th></tr>
<tr><td>VCCIO_HPS</td><td rowspan="5">6</td><td rowspan="3">Varies</td><td rowspan="5">± 5%</td><td rowspan="5">Switcher (*)</td><td rowspan="3">Share if 2.5V</td><td rowspan="3">If all of these supplies require the same voltage level, and when the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design.
Use the EPE tool to assist in determining the power required for your specific design.</td></tr>
<tr><td>VCCPD_HPS</td></tr>
<tr><td>VCCRSTCLK_HPS</td></tr>
<tr><td>VCC_AUX_SHARED</td><td rowspan="2">2.5</td><td rowspan="2">Isolate</td><td rowspan="2">VCC_AUX_SHARED must always be powered up for the HPS operation. VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED and VCCPLL_HPS with the same regulator as VCCIO_HPS, VCCPD_HPS, and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter.</td></tr>
<tr><td>VCCPLL_HPS</td></tr>
</table>

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V SX –C4, C5, I5, and C6 is provided in Figure 11.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 11. Example Power Supply Block Diagram for Arria V SX –C4, C5, I5, and C6 with Transceiver Data Rate <= 3.2 Gbps (FPGA & HPS Do Not Share Power)



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V SX –C4, C5, I5, and C6

Example 12. Power Supply Sharing Guidelines for Arria V SX –C4, C5, I5, and C6 with Transceiver Data Rate > 3.2 Gbps

Example Requiring 4 Power Regulators (FPGA & HPS Share Power)

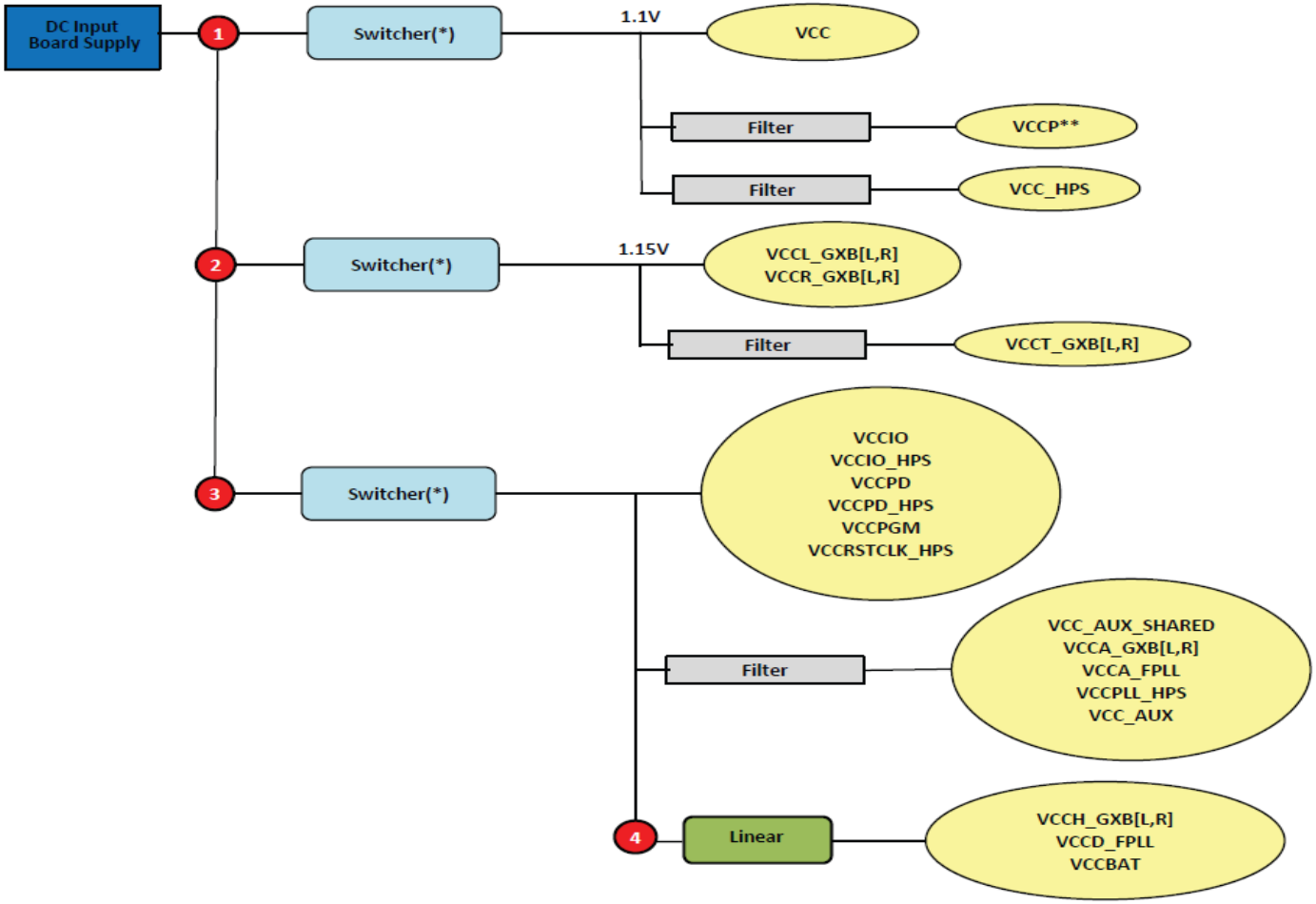
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP, VCC_HPS with same regulator as VCC with proper isolation filters.
VCCP					Isolate	
VCC_HPS					Isolate	
VCCL_GXB[L,R]	2	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require the same voltage level, and when the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCIO_HPS						
VCCPD						
VCCPD_HPS						
VCCPGM						
VCCRSTCLK_HPS						
VCC_AUX_SHARED		2.5			Isolate	VCC_AUX, VCCA_FPLL, VCCA_GXB, and VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED, VCCA_GXB, VCCA_FPLL, VCCPLL_HPS and VCC_AUX with the same regulator as VCCIO, VCCIO_HPS, VCCPD, VCCPD_HPS, VCCPGM and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCPLL_HPS						
VCC_AUX						
VCCBAT	4	Varies	± 5%	Linear	Share if 1.5V	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices. If you use the design security feature, VCCBAT should be powered by battery with voltage range as listed in the device datasheet.
VCCH_GXB[L,R]		1.5				
VCCD_FPLL						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V SX –C4, C5, I5, and C6 is provided in Figure 12.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 12. Example Power Supply Block Diagram for Arria V SX –C4, C5, I5, and C6 with Transceiver Data Rate > 3.2 Gbps (FPGA & HPS Share Power)



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V SX –C4, C5, I5, and C6

Example 13. Power Supply Sharing Guidelines for Arria V SX –C4, C5, I5, and C6 with Transceiver Data Rate > 3.2 Gbps

Example Requiring 6 Power Regulators (FPGA & HPS Do Not Share Power)

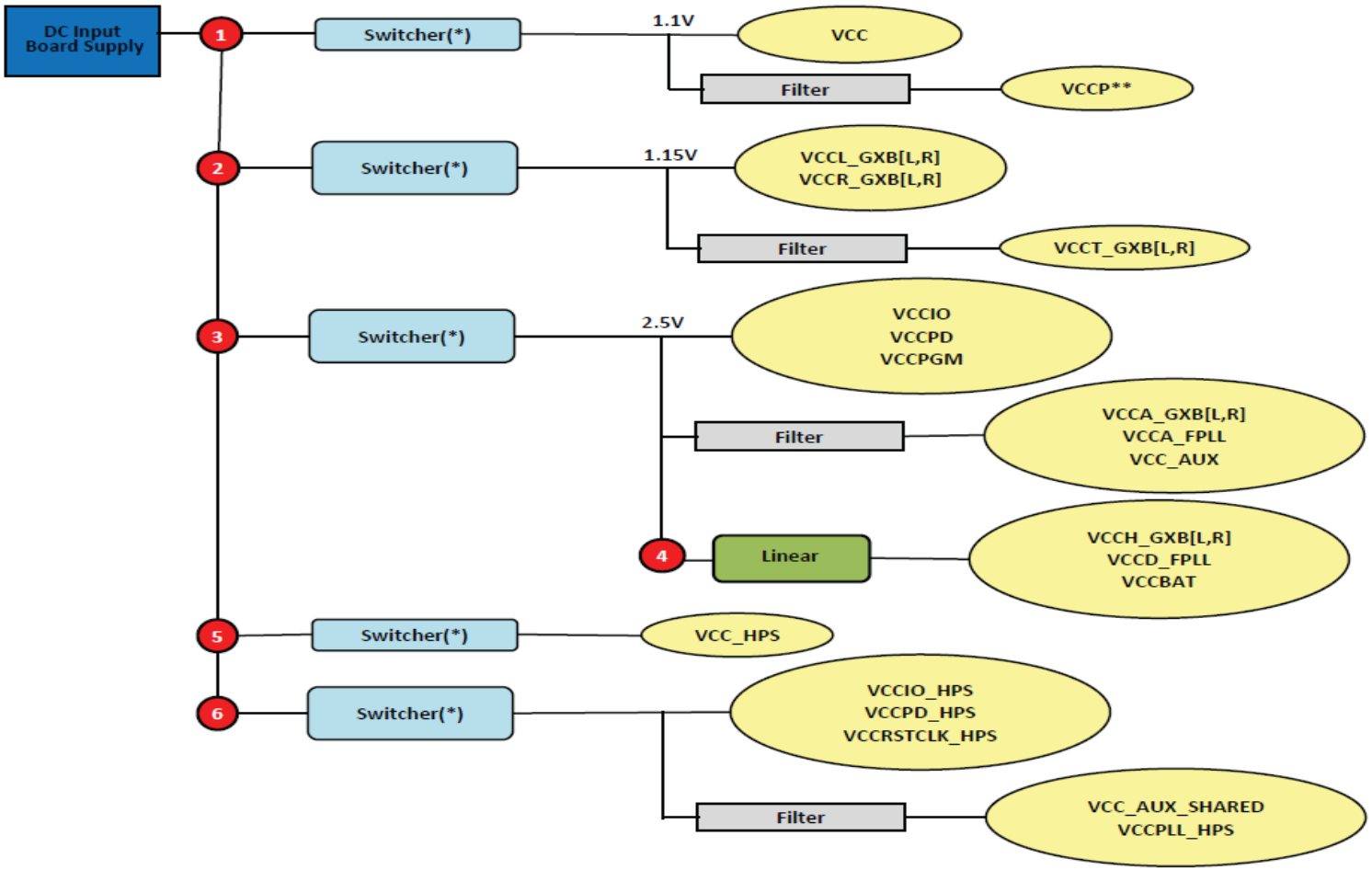
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCA_GXB[L,R]		2.5			Isolate	VCC_AUX must always be powered up for the PLL operation. May be able to share VCCA_GXB, VCCA_FPLL and VCC_AUX with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_FPLL						
VCC_AUX						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						
VCC_HPS	5	1.1	± 30mV	Switcher (*)	Isolate	Separate regulator allows the FPGA to be powered off while the HPS is powered on. VCC_HPS should be placed at power layers nearest to the Arria V device.
VCCIO_HPS	6	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require the same voltage level, and when the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD_HPS						
VCCRSTCLK_HPS						
VCC_AUX_SHARED		2.5			Isolate	VCC_AUX_SHARED must always be powered up for the HPS operation. VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED and VCCPLL_HPS with the same regulator as VCCIO_HPS, VCCPD_HPS, and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter.
VCCPLL_HPS						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V SX –C4, C5, I5, and C6 is provided in Figure 13.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 13. Example Power Supply Block Diagram for Arria V SX –C4, C5, I5, and C6 with Transceiver Data Rate > 3.2 Gbps (FPGA & HPS Do Not Share Power)



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V SX –I3

Example 14. Power Supply Sharing Guidelines for Arria V SX –I3

Example Requiring 4 Power Regulators (FPGA & HPS Share Power)

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCP with same regulator as VCC with proper isolation filters.
VCCP					Isolate	
VCC_HPS					Isolate	May be able to share VCC_HPS with same regulator as VCC with proper isolation filters.
VCCL_GXB[L,R]	2	1.15(**)	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require the same voltage level, and when the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCIO_HPS						
VCCPD						
VCCPD_HPS						
VCCPGM						
VCCRSTCLK_HPS						
VCC_AUX_SHARED		2.5			Isolate	VCC_AUX, VCCA_FPLL, VCCA_GXB, and VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED, VCCA_GXB, VCCA_FPLL, VCCPLL_HPS and VCC_AUX with the same regulator as VCCIO, VCCIO_HPS, VCCPD, VCCPD_HPS, VCCPGM and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCPLL_HPS						
VCC_AUX						
VCCBAT	4	Varies	± 5%	Linear	Share if 1.5V	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices. If you use the design security feature, VCCBAT should be powered by battery with voltage range as listed in the device datasheet.
VCCH_GXB[L,R]		1.5				
VCCD_FPLL						

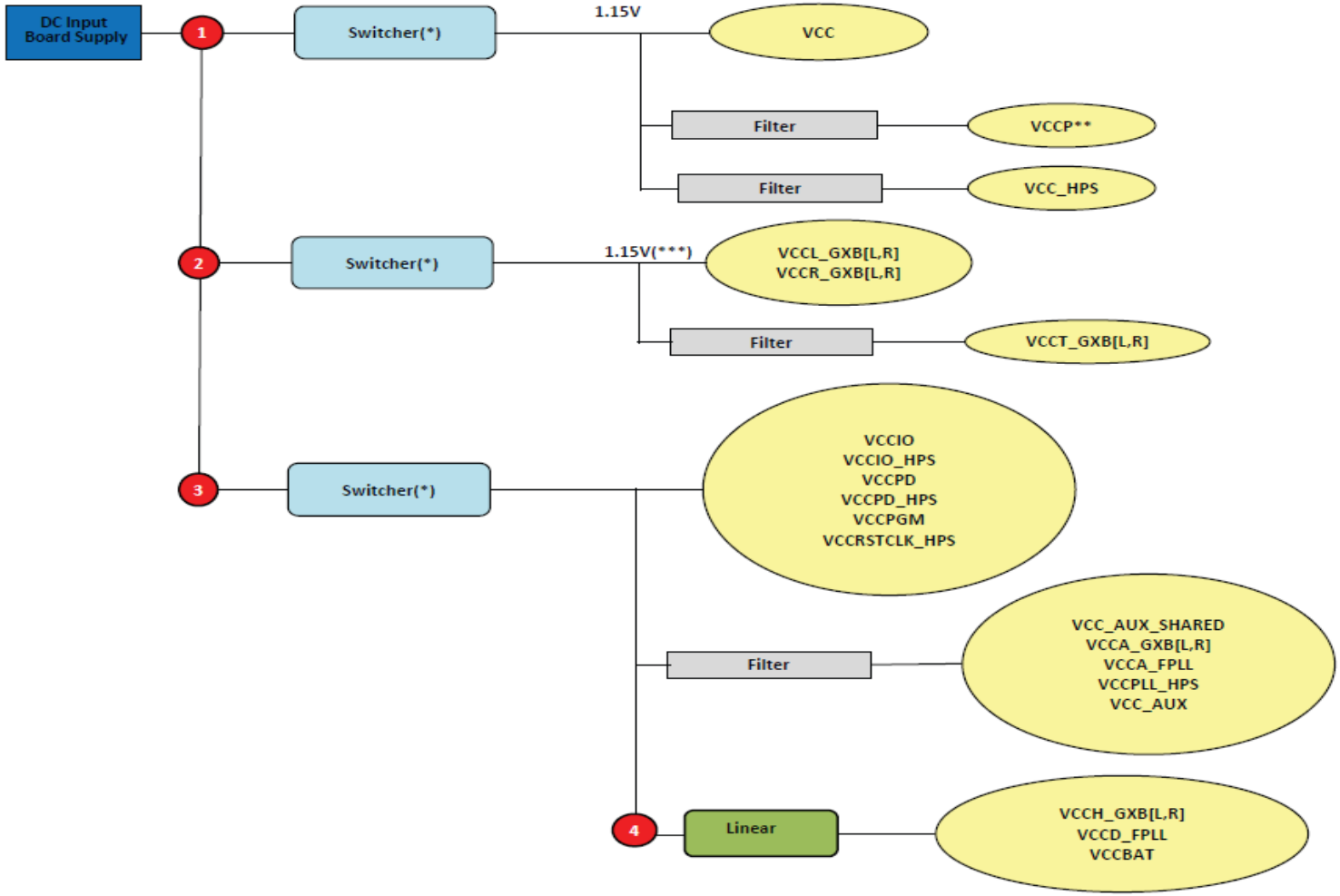
(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
(**) VCCL_GXB[L,R], VCCR_GXB[L,R], and VCCT_GXB[L,R] can be 1.1V when the transceiver data rate is <= 3.2 Gbps.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V SX –I3 is provided in Figure 14.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 14. Example Power Supply Block Diagram for Arria V SX –I3 (FPGA & HPS Share Power)



* When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
*** VCCL_GXB[L,R], VCCR_GXB[L,R], and VCCT_GXB[L,R] can be 1.1V when the transceiver data rate is <= 3.2 Gbps.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V SX –I3

Example 15. Power Supply Sharing Guidelines for Arria V SX –I3

Example Requiring 6 Power Regulators (FPGA & HPS Do Not Share Power)

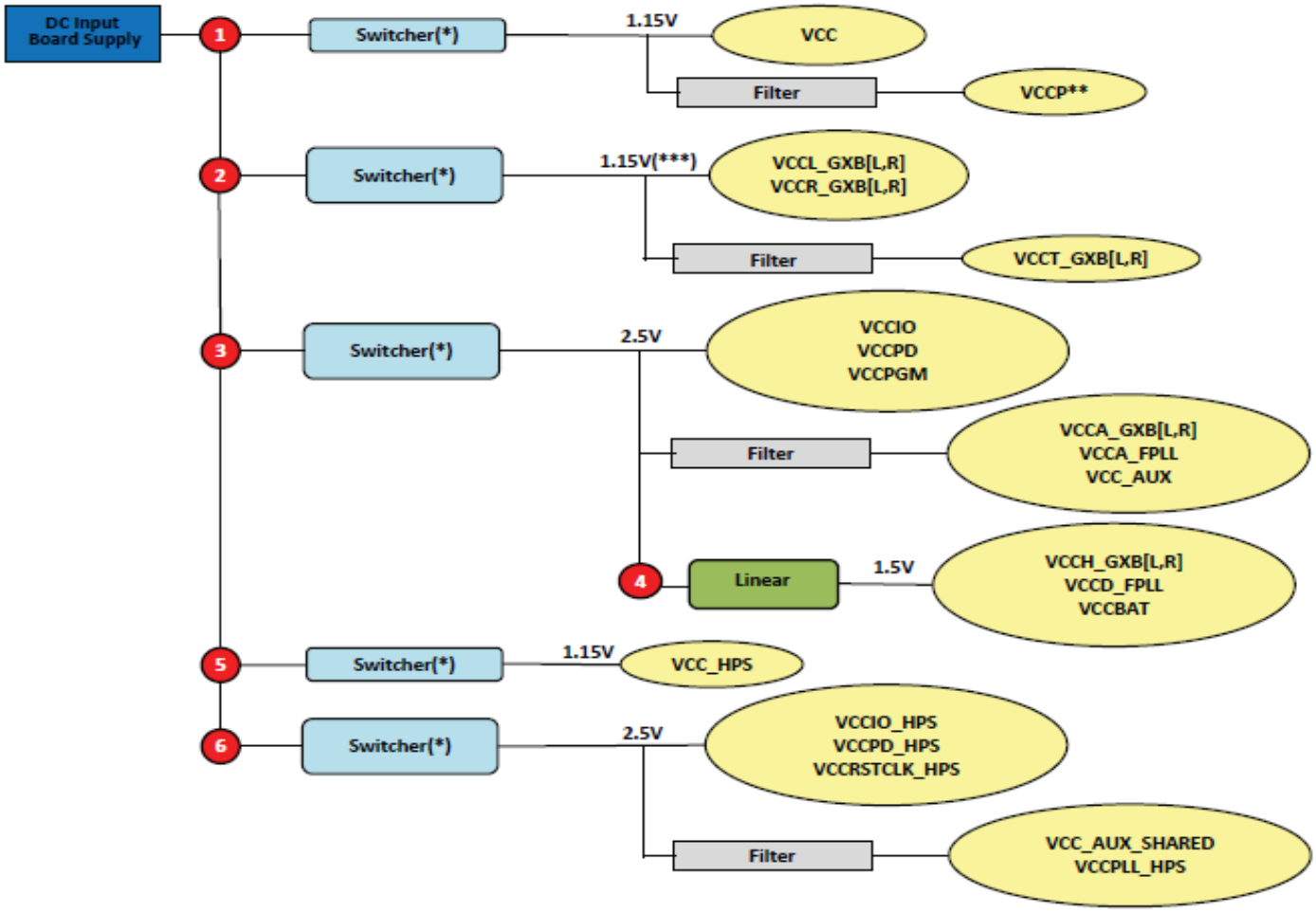
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.15(**)	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCA_GXB[L,R]		2.5			Isolate	VCC_AUX must always be powered up for the PLL operation. May be able to share VCCA_GXB, VCCA_FPLL and VCC_AUX with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_FPLL						
VCC_AUX						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						
VCC_HPS	5	1.15	± 30mV	Switcher (*)	Isolate	Separate regulator allows the FPGA to be powered off while the HPS is powered on. VCC_HPS should be placed at power layers nearest to the Arria V device.
VCCIO_HPS	6	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require the same voltage level, and when the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage level, you will require many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD_HPS						
VCCRSTCLK_HPS						
VCC_AUX_SHARED		2.5			Isolate	VCC_AUX_SHARED must always be powered up for the HPS operation. VCCPLL_HPS must always be powered up for the PLL operation. May be able to share VCC_AUX_SHARED and VCCPLL_HPS with the same regulator as VCCIO_HPS, VCCPD_HPS, and VCCRSTCLK_HPS when all power rails require 2.5V, but only with a proper isolation filter.
VCCPLL_HPS						

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
(**) VCCL_GXB[L,R], VCCR_GXB[L,R], and VCCT_GXB[L,R] can be 1.1V when the transceiver data rate is <= 3.2 Gbps.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V SX –I3 is provided in Figure 15.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Figure 15. Example Power Supply Block Diagram for Arria V SX –I3 (FPGA & HPS Do Not Share Power)



* When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping the VCC and VCCP power rails isolated from each other and on separate layers of the PCB.
*** VCCL_GXB[L,R], VCCR_GXB[L,R], and VCCT_GXB[L,R] can be 1.1V when the transceiver data rate is <= 3.2 Gbps.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Revision History

Revision	Description of Changes	Date
1.0	Initial release.	8/17/2011
1.1	Split VCC to VCC and VCCP.	1/9/2012
1.2	Updated the transceivers voltages.	6/1/2012
1.3	Updated the transceivers voltages for the Arria V GX -C4, -C5, -I5, and -C6 devices.	6/22/2012
1.4	Added Arria V GX -I3 information, updated VCCPD connection guidelines, and RREF connection guidelines.	7/24/2012
1.5	Added [B,T]_DQS_[#], [B,T]_DQS#_[#], and [B,T]_DQ_[#] pins, updated GXB_RX_[L,R] connection guidelines, and updated the data rate from 3.125Gbps to 3.2Gbps for VCCL_GXB, VCCR_GXB, and VCCT_GXB pins.	11/19/2012
1.6	-Added note (4) to VCC, VCCP, VCCIO[3,4,7,8], VCCPGM, VCCR_GXB[L,R], VCCT_GXB[L,R][0..3], and VCCL_GXB[L,R][0..3] pins. -Updated the connection guidelines for REFCLK[0:3][L,R]_[p:n] and nPERST[L0,R0]. -Updated pin description of the VCCL_GXB[L,R][0..3] pin. -Updated notes (7) and (10) in the Pin Connection Guidelines. -Moved RREF_BR and RREF_TL pins to the Reference Pins section.	4/19/2013
1.7	-Added the HPS Pin Connection Guidelines. -Added Arria V ST and SX Power Supply Sharing Guidelines. -Updated the connection guidelines for the CLKUSR pin. -Updated the pin description for DIFFIO_RX_[T,B][#,#]p, DIFFIO_RX_[T,B][#,#]n, DIFFOUT_[B,T][#,#]p, and DIFFOUT_[B,T][#,#]n pins. -Updated the connection guidelines for the VCC_AUX pin.	6/28/2013
1.8	-Updated the connection guidelines for VCC, VCCP, VCC_HPS, TMS, and TDI pins. -Updated the connection guidelines for SDMMC_CMD and SDMMC_D0 pins. -Updated power suppy sharing guidelines for Arria V ST –I3: (i) Example Requiring 4 Power Regulators (FPGA & HPS Share Power) (ii) Example Requiring 6 Power Regulators (FPGA & HPS Do Not Share Power) -Updated power suppy sharing guidelines for Arria V SX –I3: (i) Example Requiring 4 Power Regulators (FPGA & HPS Share Power) (ii) Example Requiring 6 Power Regulators (FPGA & HPS Do Not Share Power)	8/23/2013

© 2017 Intel Corporation.

Arria® V GT, GX, ST, and SX Device Family Pin Connection Guidelines
PCG-01013-2.4

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Revision	Description of Changes	Date
1.9	-Updated note (10) for both Pin Connection Guidelines and HPS Pin Connection Guidelines. -Updated the connection guidelines for VCC_AUX, VCCA_GXB, VCCA_FPLL, VCCPLL_HPS, and VCC_AUX_SHARED.	10/7/2013
2.0	-This document is no longer preliminary. -Updated the connection guidelines for VCCT_GXB[L,R][0..3], VCCL_GXB[L,R][0..3], and VCCR_GXB[L,R] pins. -Updated the connection guidelines for the VCCP pin. -Updated the connection guidelines for CQ[#][B,T,R], CQn[#][B,T,R], QK[#][B,T,R], and QKn[#][B,T,R] pins. -Updated the connection guidelines for the VCCBAT pin. -Updated the connection guidelines for REFCLK[0:3][L,R]_[p:n] pins. -Updated the connection guidelines for BOOTSEL0, BOOTSEL1, and BOOTSEL2 pins. -Updated the connection guidelines for VREF[#]N0 pins. -Updated the connection guidelines for VREFB[#]N0_HPS pins. -Updated the pin type for HPS_PORSEL pin. -Added a note to VCCL_GXB[L,R], VCCR_GXB[L,R], and VCCT_GXB[L,R] in Example 1, Example 2, Example 3, Example 4, and Example 5.	11/14/2014
2.1	-Updated content in the Disclaimer section. -Added links referring to Arria V Device Handbook: Power Management in Arria V Devices for all power sharing guidelines tables and figures. -Added Note 13 for HPS Peripheral Pins and General Purpose Input Pins.	5/19/2015
2.2	- Updated list of Arria V GX devices which should combine and share VCCR_GXB, VCCT_GXB, and VCCL_GXB power supply.	4/6/2016
2.3	- Updated that all GXB_TX pin (p,n) can be left floating when unused. - Removed SDMMC_FB_CLK_IN pin. - Added HPS_GPIO44 pin as General Purpose I/O bit 44. - Removed 1.2 LVTTL/LVCMOS and HSTL 12 support for VCCIO[#]_HPS pin.	10/28/2016

© 2017 Intel Corporation.

Intel recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime design will check your pin connections according to I/O assignments and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

2.4	- Added a note (15) to SDMMC_D3 pin. - Added guideline to pull-up SDMMC_D1, SDMMC_D2, SDMMC_D3, SDMMC_D4, SDMMC_D5, SDMMC_D6, and SDMMC_D7 pins when booting HPS from an MMC/eMMC device.	11/17/2017

© 2017 Intel Corporation.