

### FEATURES

- isoPower* integrated isolated dc-to-dc converter
- Regulated 3 V or 5 V output
- Up to 500 mW output power
- Dual dc-to-25 Mbps (NRZ) signal isolation channels
- Schmitt trigger inputs
- 16-lead SOIC package with >8 mm creepage
- High temperature operation: 105°C maximum
- High common-mode transient immunity: >25 kV/μs
- Safety and regulatory approvals
  - UL recognition
    - 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A (pending)
  - VDE certificate of conformity (pending)
  - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - $V_{IORM} = 560$  V peak

### APPLICATIONS

- RS-232/RS-422/RS-485 transceivers
- Industrial field bus isolation
- Power supply startups and gate drives
- Isolated sensor interfaces
- Industrial PLCs

### GENERAL DESCRIPTION

The ADuM520x<sup>1</sup> are dual channel digital isolators with *isoPower*, an integrated, isolated dc-to-dc converter. Based on the Analog Devices, Inc., *iCoupler*<sup>®</sup> technology, the dc-to-dc converter provides up to 500 mW of regulated, isolated power with 5.0 V input and 5.0 V output voltage, or 200 mW of power with 3.3 V input and 3.3 V output voltage. This eliminates the need for a separate isolated dc-to-dc converter in low power isolated designs. The Analog Devices chip scale transformer *iCoupler* technology is used for the isolation of the logic signals as well as for the dc-to-dc converter. The result is a small form factor, total isolation solution.

ADuM520x units can be used in combination with the ADuM5401, ADuM5402, ADuM5403, ADuM5404, and ADuM5000 with *isoPower*<sup>®</sup> to achieve higher output power

<sup>1</sup> Protected by U.S. Patents: 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

#### Rev. 0

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### FUNCTIONAL BLOCK DIAGRAM

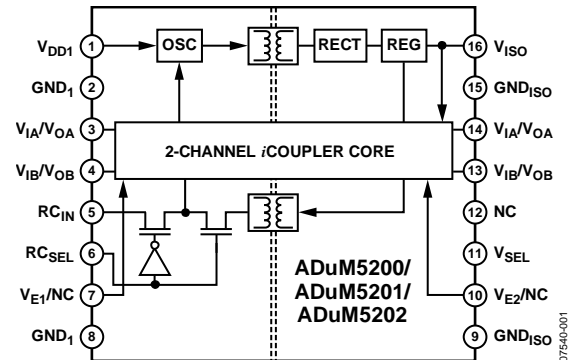


Figure 1.

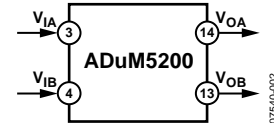


Figure 2. ADuM5200

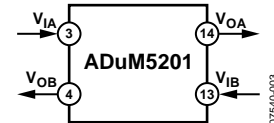


Figure 3. ADuM5201

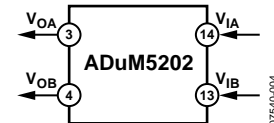


Figure 4. ADuM5202

levels and greater channel counts (see the Increasing Available Power section).

The ADuM520x isolators provide two independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide for options).

*isoPower* uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to the AN-0971 application note for details on board layout recommendations.

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## REVISION HISTORY

10/08—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

$4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $V_{SEL} = V_{ISO}$ ; each voltage is relative to its respective ground. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $V_{ISO} = 5.0\text{ V}$ ,  $V_{SEL} = V_{ISO}$ .

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC-TO-DC CONVERTER POWER SUPPLY</b>						
Setpoint	$V_{ISO}$	4.7	5.0	5.4	V	$I_{ISO} = 0\text{ mA}$
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	$I_{ISO} = 50\text{ mA}$ , $V_{DD1} = 4.5\text{ V to }5.5\text{ V}$
Load Regulation	$V_{ISO(LOAD)}$		1	5	%	$I_{ISO} = 10\text{ mA to }90\text{ mA}$
Output Ripple	$V_{ISO(RIP)}$		75		mV p-p	20 MHz bandwidth, $C_{BO} = 0.1\text{ }\mu\text{F}  10\text{ }\mu\text{F}$ , $I_{ISO} = 90\text{ mA}$
Output Noise	$V_{ISO(IN)}$		200		mV p-p	$C_{BO} = 0.1\text{ }\mu\text{F}  10\text{ }\mu\text{F}$ , $I_{ISO} = 90\text{ mA}$
Switching Frequency	$f_{OSC}$		180		MHz	
Pulse-Width Modulation Frequency	$f_{PWM}$		625		kHz	
DC-to-2 Mbps Data Rate <sup>1</sup>						
Maximum Output Supply Current <sup>2</sup>	$I_{ISO(MAX)}$	100			mA	$V_{ISO} > 4.5\text{ V}$ , dc to 1 MHz logic signal frequency
Efficiency @ Maximum Output Supply Current <sup>3</sup>			34		%	$I_{ISO} = 100\text{ mA}$ , dc to 1 MHz logic signal frequency
$I_{DD1}$ Supply Current, No $V_{ISO}$ Load	$I_{DD1(Q)}$		8	22	mA	$I_{ISO} = 0\text{ mA}$ , dc to 1 MHz logic signal frequency
<b>25 Mbps Data Rate (CRWZ Grade Only)</b>						
$I_{DD1}$ Supply Current, No $V_{ISO}$ Load						
ADuM5200	$I_{DD1(D)}$		34		mA	$I_{ISO} = 0\text{ mA}$ , $C_L = 15\text{ pF}$ , 12.5 MHz logic signal frequency
ADuM5201	$I_{DD1(D)}$		38		mA	$I_{ISO} = 0\text{ mA}$ , $C_L = 15\text{ pF}$ , 12.5 MHz logic signal frequency
ADuM5202	$I_{DD1(D)}$		41		mA	$I_{ISO} = 0\text{ mA}$ , $C_L = 15\text{ pF}$ , 12.5 MHz logic signal frequency
Available $V_{ISO}$ Supply Current <sup>4</sup>						
ADuM5200	$I_{ISO(LOAD)}$		94		mA	$C_L = 15\text{ pF}$ , 12.5 MHz logic signal frequency
ADuM5201	$I_{ISO(LOAD)}$		92		mA	$C_L = 15\text{ pF}$ , 12.5 MHz logic signal frequency
ADuM5202	$I_{ISO(LOAD)}$		90		mA	$C_L = 15\text{ pF}$ , 12.5 MHz logic signal frequency
$I_{DD1}$ Supply Current, Full $V_{ISO}$ Load <sup>5</sup>	$I_{DD1(MAX)}$		290		mA	$C_L = 0\text{ pF}$ , dc to 1 MHz logic signal frequency, $V_{DD} = 4.5\text{ V}$ , $I_{ISO} = 100\text{ mA}$
<b>Undervoltage Lockout, <math>V_{DD1}</math> and <math>V_{ISO}</math> Supply<sup>6</sup></b>						
Positive Going Threshold	$V_{UV+}$		2.7		V	
Negative Going Threshold	$V_{UV-}$		2.4		V	
Hysteresis	$V_{UVH}$		0.3		V	
<b>iCoupler DATA CHANNELS</b>						
I/O Input Currents	$I_{IA}, I_{IB}$	-20	+0.01	+20	$\mu\text{A}$	
Logic High Input Threshold	$V_{IH}$	$0.7 \times V_{ISO}$ , $0.7 \times V_{DD1}$			V	
Logic Low Input Threshold	$V_{IL}$			$0.3 \times V_{ISO}$ , $0.3 \times V_{DD1}$	V	

# ADuM5200/ADuM5201/ADuM5202

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Logic High Output Voltages	$V_{OAH}, V_{OBH}$	$V_{DD1} - 0.3,$ $V_{ISO} - 0.3$	5.0		V	$I_{Ox} = -20 \mu A, V_{Ix} = V_{IxH}$
	$V_{OAH}, V_{OBH}$	$V_{DD1} - 0.5,$ $V_{ISO} - 0.5$	4.8		V	$I_{Ox} = -4 \text{ mA}, V_{Ix} = V_{IxH}$
Logic Low Output Voltages	$V_{OAL}, V_{OBL}$		0.0	0.1	V	$I_{Ox} = 20 \mu A, V_{Ix} = V_{IxL}$
			0.0	0.4	V	$I_{Ox} = 4 \text{ mA}, V_{Ix} = V_{IxL}$
AC SPECIFICATIONS						
ADuM520xARWZ <sup>7</sup>						
Minimum Pulse Width	PW			1000	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Maximum Data Rate		1			Mbps	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay	$t_{PHL}, t_{PLH}$		55	100	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $	PWD			40	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew	$t_{PSK}$			50	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching	$t_{PSKCD}, t_{PSKOD}$			50	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
ADuM520xCRWZ						
Minimum Pulse Width <sup>7</sup>	PW			40	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Maximum Data Rate		25			Mbps	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay	$t_{PHL}, t_{PLH}$		45	60	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $	PWD			6	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew	$t_{PSK}$			15	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	$t_{PSKCD}$			6	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels	$t_{PSKOD}$			15	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
For All Models						
Output Rise/Fall Time (10% to 90%)	$t_R/t_F$		2.5		ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$ CM_H $	25	35		kV/ $\mu$ s	$V_{Ix} = V_{DD}$ or $V_{ISO}$ , $V_{CM} = 1000 \text{ V}$ , transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$ CM_L $	25	35		kV/ $\mu$ s	$V_{Ix} = 0 \text{ V}$ , $V = 1000 \text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$		1.0		Mbps	

<sup>1</sup> The contributions of supply current values for all four channels are combined at identical data rates.

<sup>2</sup>  $V_{ISO}$  supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and be included in the  $V_{ISO}$  power budget.

<sup>3</sup> The power demands of the quiescent operation of the data channels cannot be separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of its internal power consumption.

<sup>4</sup> This current is available for driving external loads at the  $V_{ISO}$  pin. All channels are simultaneously driven at a maximum data rate of 25 Mbps with the full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for the calculation of available current at less than the maximum data rate.

<sup>5</sup>  $I_{DD1(MAX)}$  is the input current under full dynamic and  $V_{ISO}$  load conditions.

<sup>6</sup> Undervoltage lockout (UVLO) holds the outputs in a low state if the corresponding input or output power supply is below the referenced threshold. Hysteresis is built into the detection threshold to prevent oscillations and noise sensitivity.

<sup>7</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

**ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY**

3.0 V ≤ V<sub>DD1</sub> ≤ 3.6 V, V<sub>SEL</sub> = GND<sub>ISO</sub>; each voltage is relative to its respective ground. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T<sub>A</sub> = 25°C, V<sub>DD</sub> = 3.3 V, V<sub>ISO</sub> = 3.3 V, V<sub>SEL</sub> = GND<sub>ISO</sub>.

**Table 2.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC-TO-DC CONVERTER POWER SUPPLY</b>						
Setpoint	V <sub>ISO</sub>	3.13	3.3	3.37	V	I <sub>ISO</sub> = 0 mA
Line Regulation	V <sub>ISO(LINE)</sub>		1		mV/V	I <sub>ISO</sub> = 30 mA, V <sub>DD1</sub> = 3.0 V to 3.6 V
Load Regulation	V <sub>ISO(LOAD)</sub>		1	5	%	I <sub>ISO</sub> = 6 mA to 54 mA
Output Ripple	V <sub>ISO(RIP)</sub>		50		mV p-p	20 MHz bandwidth, C <sub>BO</sub> = 0.1 μF  10μF, I <sub>ISO</sub> = 54 mA
Output Noise	V <sub>ISO(N)</sub>		130		mV p-p	C <sub>BO</sub> = 0.1 μF  10μF, I <sub>ISO</sub> = 54 mA
Switching Frequency	f <sub>OSC</sub>		180		MHz	
Pulse-Width Modulation Frequency	f <sub>PWM</sub>		625		kHz	
DC to 2 Mbps Data Rate <sup>1</sup>						
Maximum Output Supply Current <sup>2</sup>	I <sub>ISO(MAX)</sub>	60			mA	V <sub>ISO</sub> > 3.0 V, dc to 1 MHz logic signal frequency
Efficiency @ Maximum Output Supply Current <sup>3</sup>			36		%	I <sub>ISO</sub> = 60 mA, dc to 1 MHz logic signal frequency
I <sub>DD1</sub> Supply Current, No V <sub>ISO</sub> load	I <sub>DD1(Q)</sub>		6	15	mA	I <sub>ISO</sub> = 0 mA, dc to 1 MHz logic signal frequency
I <sub>DD1</sub> Supply Current, Full V <sub>ISO</sub> load	I <sub>DD1(MAX)</sub>		175		mA	C <sub>L</sub> = 0 pF, f = 0 MHz, V <sub>DD</sub> = 3.3 V, I <sub>ISO</sub> = 60 mA
<b>25 Mbps Data Rate (CRWZ Grade Only)</b>						
I <sub>DD1</sub> Supply Current, No V <sub>ISO</sub> Load <sup>4</sup>						
ADuM5200	I <sub>DD1(D)</sub>		23		mA	I <sub>ISO</sub> = 0 mA, C <sub>L</sub> = 15 pF, 12.5 MHz logic signal frequency
ADuM5201	I <sub>DD1(D)</sub>		25		mA	I <sub>ISO</sub> = 0 mA, C <sub>L</sub> = 15 pF, 12.5 MHz logic signal frequency
ADuM5202	I <sub>DD1(D)</sub>		27		mA	I <sub>ISO</sub> = 0 mA, C <sub>L</sub> = 15 pF, 12.5 MHz logic signal frequency
Available V <sub>ISO</sub> Supply Current <sup>5</sup>						
ADuM5200	I <sub>ISO(LOAD)</sub>		56		mA	C <sub>L</sub> = 15 pF, 12.5 MHz logic signal frequency
ADuM5201	I <sub>ISO(LOAD)</sub>		55		mA	C <sub>L</sub> = 15 pF, 12.5 MHz logic signal frequency
ADuM5202	I <sub>ISO(LOAD)</sub>		54		mA	C <sub>L</sub> = 15 pF, 12.5 MHz logic signal frequency
Undervoltage Lockout (UVLO), V <sub>DD1</sub> and V <sub>ISO</sub> Supply <sup>6</sup>						
Positive Going Threshold	V <sub>UV+</sub>		2.7		V	
Negative Going Threshold	V <sub>UV-</sub>		2.4		V	
Hysteresis	V <sub>UVH</sub>		0.3		V	
<b>iCoupler DATA CHANNELS</b>						
I/O Input Currents	I <sub>IA</sub> , I <sub>IB</sub>	-20	+0.01	+20	μA	
Logic High Input Threshold	V <sub>IH</sub>	0.7 × V <sub>ISO</sub> , 0.7 × V <sub>DD1</sub>			V	
Logic Low Input Threshold	V <sub>IL</sub>			0.3 × V <sub>ISO</sub> , 0.3 × V <sub>DD1</sub>	V	
Logic High Output Voltages	V <sub>OAH</sub> , V <sub>OBH</sub>	V <sub>DD1</sub> - 0.2, V <sub>ISO</sub> - 0.2	3.3		V	I <sub>OX</sub> = -20 μA, V <sub>IX</sub> = V <sub>IXH</sub>
	V <sub>OAH</sub> , V <sub>OBH</sub>	V <sub>DD1</sub> - 0.5, V <sub>ISO</sub> - 0.5	3.1		V	I <sub>OX</sub> = -4 mA, V <sub>IX</sub> = V <sub>IXH</sub>
Logic Low Output Voltages	V <sub>OAL</sub> , V <sub>OBL</sub>		0.0	0.1	V	I <sub>OX</sub> = 20 μA, V <sub>IX</sub> = V <sub>IXL</sub>
	V <sub>OAL</sub> , V <sub>OBL</sub>		0.0	0.4	V	I <sub>OX</sub> = 4 mA, V <sub>IX</sub> = V <sub>IXL</sub>

# ADuM5200/ADuM5201/ADuM5202

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
AC SPECIFICATIONS						
ADuM520xARWZ						
Minimum Pulse Width <sup>7</sup>	PW			1000	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay	t <sub>PHL</sub> , t <sub>PLH</sub>		60	100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>	PWD			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew	t <sub>PSK</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t <sub>PSKCD</sub> , t <sub>PSKOD</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
ADuM520xCRWZ						
Minimum Pulse Width <sup>7</sup>	PW			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay	t <sub>PHL</sub> , t <sub>PLH</sub>		45	60	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>	PWD			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew	t <sub>PSK</sub>			45	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t <sub>PSKCD</sub>			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels	t <sub>PSKOD</sub>			15	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
For All Models						
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>F</sub>		2.5		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	CM <sub>H</sub>	25	35		kV/μs	V <sub>ix</sub> = V <sub>DD</sub> or V <sub>ISO</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	CM <sub>L</sub>	25	35		kV/μs	V <sub>ix</sub> = 0 V, V = 1000 V, transient magnitude = 800 V
Refresh Rate	f <sub>r</sub>		1.0		Mbps	

<sup>1</sup> The contributions of supply current values for all four channels are combined at identical data rates.

<sup>2</sup> V<sub>ISO</sub> supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and be included in the V<sub>ISO</sub> power budget.

<sup>3</sup> The power demands of the quiescent operation of the data channels cannot be separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of its internal power consumption.

<sup>4</sup> I<sub>DD1(D)</sub> is the typical input supply current with all channels simultaneously driven at a maximum data rate of 25 Mbps with the full capacitive load representing the maximum dynamic load conditions. Treat resistive loads on the outputs separately from the dynamic load.

<sup>5</sup> This current is available for driving external loads at the V<sub>ISO</sub> pin. All channels are simultaneously driven at a maximum data rate of 25 Mbps with the full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for the calculation of available current at less than the maximum data rate.

<sup>6</sup> Undervoltage lockout (UVLO) holds the outputs in a low state if the corresponding input or output power supply is below the referenced threshold. Hysteresis is built into the detection threshold to prevent oscillations and noise sensitivity.

<sup>7</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

**PACKAGE CHARACTERISTICS**

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>RESISTANCE AND CAPACITANCE</b>						
Resistance (Input-to-Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	f = 1 MHz
Capacitance (Input-to-Output) <sup>1</sup>	C <sub>I-O</sub>		2.2		pF	
Input Capacitance <sup>2</sup>	C <sub>I</sub>		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ <sub>JA</sub>		45		°C/W	Thermocouple located at the center of the package underside; test conducted on a 4-layer board with thin traces <sup>3</sup>
<b>THERMAL SHUTDOWN</b>						
Threshold	TS <sub>SD</sub>		150		°C	T <sub>J</sub> rising
Hysteresis	TS <sub>SD-HYS</sub>		20		°C	

<sup>1</sup> This device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

<sup>3</sup> Refer to the Power Considerations section for thermal model definitions.

**REGULATORY INFORMATION**

The ADuM5200/ADuM5201/ADuM5202 are approved by the organizations listed in Table 4. Refer to Table 9 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 4.

UL	CSA (Pending)	VDE (Pending)
Recognized under 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 <sup>2</sup>
Single Protection 2500 V RMS Isolation Voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

<sup>1</sup> In accordance with UL 1577, each ADuM520x is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 sec (current leakage detection limit = 5 μA).

<sup>2</sup> In accordance with DIN V VDE V 0884-10, each ADuM520x is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN V VDE V 0884-10 approval.

**INSULATION AND SAFETY-RELATED SPECIFICATIONS**

Table 5.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	>8 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	>8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Distance through the insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material group (DIN VDE 0110, 1/89, Table 1)

# ADuM5200/ADuM5201/ADuM5202

## DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The \* marking on packages denotes DIN V VDE V 0884-10 approval.

Table 6.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to IV I to III I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		$V_{IORM}$	560	V peak
Input-to-Output Test Voltage Method b1	$V_{IORM} \times 1.875 = V_{PR}$ , 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	$V_{PR}$	1050	V peak
Method a After Environmental Tests Subgroup 1 After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, partial discharge < 5 pC $V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, partial discharge < 5 pC	$V_{PR}$	896 672	V peak V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ sec	$V_{TR}$	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 5)			
Case Temperature		$T_S$	150	°C
Side 1 $I_{DD1}$ Current		$I_{S1}$	555	mA
Insulation Resistance at $T_S$	$V_{IO} = 500$ V	$R_S$	>10 <sup>9</sup>	Ω

### Thermal Derating Curve

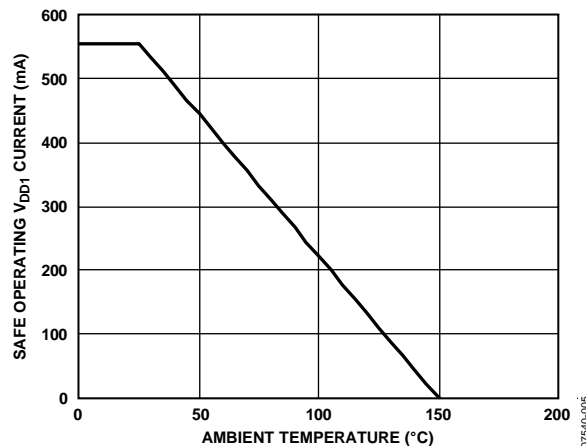


Figure 5. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

**RECOMMENDED OPERATING CONDITIONS**

Table 7.

Parameter	Symbol	Min	Max	Unit
OPERATING TEMPERATURE	$T_A$	-40	+105	°C
SUPPLY VOLTAGES <sup>1</sup>				
$V_{DD1}$ @ $V_{SEL} = 0\text{ V}$	$V_{DD}$	3.0	3.6	V
$V_{DD1}$ @ $V_{SEL} = V_{DD1}\text{ V}$	$V_{DD}$	4.5	5.5	V
Minimum Load	$I_{ISO(MIN)}$	10		mA
Minimum Power-On Slew Rate	$V_{SLEW}$	150		V/ms

<sup>1</sup> Each voltage is relative to its respective ground.

## ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
Storage Temperature (T <sub>ST</sub> )	–55°C to +150°C
Ambient Operating Temperature (T <sub>A</sub> )	–40°C to +105°C
Supply Voltages (V <sub>DD</sub> , V <sub>ISO</sub> ) <sup>1</sup>	–0.5 V to +7.0 V
V <sub>ISO</sub> Supply Current <sup>2</sup>	100 mA
Input Voltage (V <sub>IA</sub> , V <sub>IB</sub> , V <sub>E1</sub> , V <sub>E2</sub> , R <sub>CSEL</sub> , V <sub>SEL</sub> ) <sup>1,3</sup>	–0.5 V to V <sub>DDI</sub> + 0.5 V
Output Voltage (V <sub>OA</sub> , V <sub>OB</sub> ) <sup>1,3</sup>	–0.5 V to V <sub>DDO</sub> + 0.5 V
Average Output Current per Data Output Pin <sup>4</sup>	–10 mA to +10 mA
Common-Mode Transients <sup>5</sup>	–100 kV/μs to +100 kV/μs

<sup>1</sup> Each voltage is relative to its respective ground.

<sup>2</sup> The V<sub>ISO</sub> provides current for dc and dynamic loads on the Side 2 input/output channels. This current must be included when determining the total V<sub>ISO</sub> supply current.

<sup>3</sup> V<sub>DDI</sub> and V<sub>DDO</sub> refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.

<sup>4</sup> See Figure 5 for maximum rated current values for various temperatures.

<sup>5</sup> Refers to common-mode transients across the isolation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Maximum Continuous Working Voltage Supporting a 50-Year Minimum Lifetime<sup>1</sup>

Parameter	Max	Unit	Reference Standard
AC Voltage			
Bipolar Waveform	424	V peak	50-year minimum lifetime
Unipolar Waveform			
Basic Insulation	600	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Basic Insulation	600	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

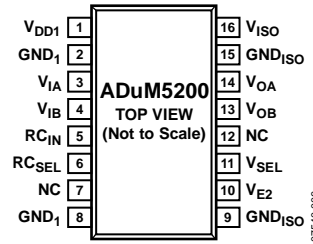
<sup>1</sup> Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



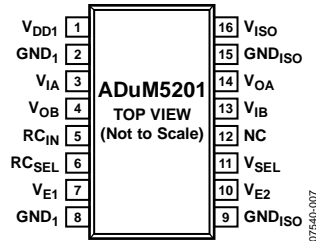
NC = NO CONNECT

Figure 6. ADuM5200 Pin Configuration

Table 10. ADUM5200 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Primary Supply Voltage 3.0 V to 5.5 V.
2, 8	GND <sub>1</sub>	Ground 1. Ground reference for the isolator primary side. Pin 2 and Pin 8 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	RC <sub>IN</sub>	Regulation Control Input. This pin must be connected to an RC <sub>OUT</sub> signal from another device or tied low. Note: This pin must not be tied high if RC <sub>SEL</sub> is low; this combination causes excessive voltage on the secondary side, damaging the ADuM5200 and possibly the devices that it powers.
6	RC <sub>SEL</sub>	Control Input. Determines self-regulation (RC <sub>SEL</sub> high) mode or slave mode (RC <sub>SEL</sub> low) allowing external regulation. This pin is weakly pulled to the high state. In noisy environments, tie it either high or low.
7, 12	NC	No Internal Connection.
9, 15	GND <sub>ISO</sub>	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10	V <sub>E2</sub>	Data Enable Input. When high or no connect, the secondary outputs are active; when low, the outputs are in a high-Z state.
11	V <sub>SEL</sub>	Output Voltage Selection. When V <sub>SEL</sub> = V <sub>ISO</sub> , the V <sub>ISO</sub> setpoint is 5.0 V. When V <sub>SEL</sub> = GND <sub>ISO</sub> , the V <sub>ISO</sub> setpoint is 3.3 V. In slave regulation mode, this pin has no function.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
16	V <sub>ISO</sub>	Secondary Supply Voltage. Output for secondary side isolated data channels and external loads.

# ADuM5200/ADuM5201/ADuM5202

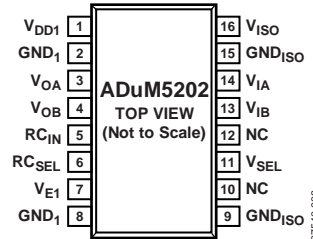


NC = NO CONNECT

Figure 7. ADuM5201 Pin Configuration

Table 11. ADuM5201 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Primary Supply Voltage 3.0 V to 5.5 V.
2, 8	GND <sub>1</sub>	Ground 1. Ground reference for isolator primary side. Pin 2 and Pin 8 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>OB</sub>	Logic Output B.
5	RC <sub>IN</sub>	Regulation Control Input. This pin must be connected to an RC <sub>OUT</sub> signal from another device or tied low. Note: This pin must not be tied high if RC <sub>SEL</sub> is low; this combination causes excessive voltage on the secondary side, damaging the ADuM5201 and possibly the devices that it powers.
6	RC <sub>SEL</sub>	Control Input. Determines self-regulation mode (RC <sub>SEL</sub> high) or slave mode (RC <sub>SEL</sub> low) allowing external regulation. This pin is weakly pulled to the high state. In noisy environments, tie it either high or low.
7	V <sub>E1</sub>	Data Enable Input. When high or no connect, the primary output is active; when low, the outputs are in a high-Z state.
9, 15	GND <sub>ISO</sub>	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10	V <sub>E2</sub>	Data Enable Input. When high or no connect, the secondary output is active; when low, the outputs are in a high-Z state.
11	V <sub>SEL</sub>	Output Voltage Selection. When V <sub>SEL</sub> = V <sub>ISO</sub> , the V <sub>ISO</sub> setpoint is 5.0 V. When V <sub>SEL</sub> = GND <sub>ISO</sub> , the V <sub>ISO</sub> setpoint is 3.3 V. In slave regulation mode, this pin has no function.
12	NC	No Internal Connection.
13	V <sub>IB</sub>	Logic Input B.
14	V <sub>OA</sub>	Logic Output A.
16	V <sub>ISO</sub>	Secondary Supply Voltage. Output for secondary side isolated data channels and external loads.



NC = NO CONNECT

Figure 8. ADuM5202 Pin Configuration

**Table 12. ADuM5202 Pin Function Descriptions**

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Primary Supply Voltage 3.0 V to 5.5 V.
2, 8	GND <sub>1</sub>	Ground 1. Ground reference for the isolator primary. Pin 2 and Pin 8 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
3	V <sub>OA</sub>	Logic Output A.
4	V <sub>OB</sub>	Logic Output B.
5	RC <sub>IN</sub>	Regulation Control Input. This pin must be connected to an RC <sub>OUT</sub> signal from another device or tied low. Note: This pin must not be tied high if RC <sub>SEL</sub> is low; this combination causes excessive voltage on the secondary side, damaging the ADuM5202 and possibly the devices that it powers.
6	RC <sub>SEL</sub>	Control Input. Determines self-regulation (RC <sub>SEL</sub> high) mode or slave mode (RC <sub>SEL</sub> low) allowing external regulation. This pin is weakly pulled to the high state. In noisy environments, tie it either high or low.
7	V <sub>E1</sub>	Data Enable Input. When high or no connect, the primary output is active; when low, the outputs are in a high-Z state.
9, 15	GND <sub>ISO</sub>	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10, 12	NC	No Internal Connection.
11	V <sub>SEL</sub>	Output Voltage Selection. When V <sub>SEL</sub> = V <sub>ISO</sub> , the V <sub>ISO</sub> setpoint is 5.0 V. When V <sub>SEL</sub> = GND <sub>ISO</sub> , the V <sub>ISO</sub> setpoint is 3.3 V.
13	V <sub>IB</sub>	Logic Input B.
14	V <sub>IA</sub>	Logic Input A.
16	V <sub>ISO</sub>	Secondary Supply Voltage. Output for secondary side isolated data channels and external loads.

# ADuM5200/ADuM5201/ADuM5202

Table 13. Truth Table (Positive Logic)

RC <sub>IN</sub> Input	RC <sub>SEL</sub> Input	V <sub>SEL</sub> Input <sup>1</sup>	V <sub>DDI</sub> Input	V <sub>ISO</sub> Output	V <sub>IX</sub> Input	V <sub>OX</sub> Output	Operation
X	H	H	5.0V	5.0V	X	X	Master mode operation, self-regulating.
X	H	L	5.0V	3.3V	X	X	Power configuration not supported.
X	H	H	3.3V	5.0V	X	X	Power configuration not supported.
X	H	L	3.3V	3.3V	X	X	Master mode operation, self-regulating.
EXT-PWM <sup>1</sup>	L	X	X	X	X	X	Slave mode operation, regulation from another <i>isoPower</i> part.
L	L	L	X	0V	X	X	Low power mode, converter disabled.
X	X	X	X	X	H	H	Data outputs valid for any active power configuration.
X	X	X	X	X	L	L	Data outputs valid for any active power configuration.
H	L	X	X	X	X	X	Note: This combination of RC <sub>IN</sub> and RC <sub>SEL</sub> is prohibited. Damage occurs on the secondary side of the converter due to excess output voltage at V <sub>ISO</sub> . RC <sub>IN</sub> must be either low or a PWM signal from a master <i>isoPower</i> part.

<sup>1</sup> PWM refers to the regulation control signal. This signal is derived from the secondary side regulator or from the RC<sub>IN</sub> input, depending on the value of RC<sub>SEL</sub>.

## TYPICAL PERFORMANCE CHARACTERISTICS

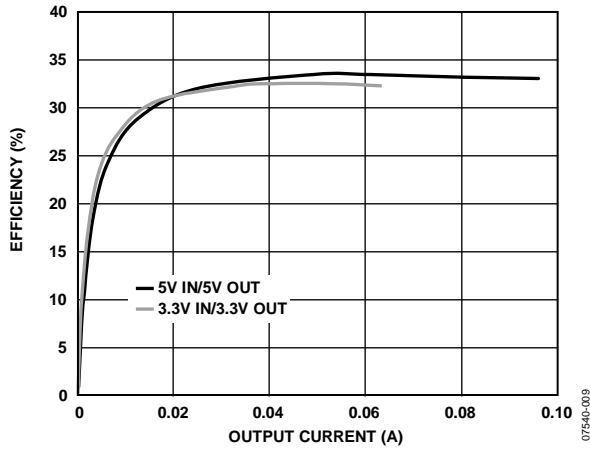


Figure 9. Typical Power Supply Efficiency at 5 V/5 V and 3.3 V/3.3 V

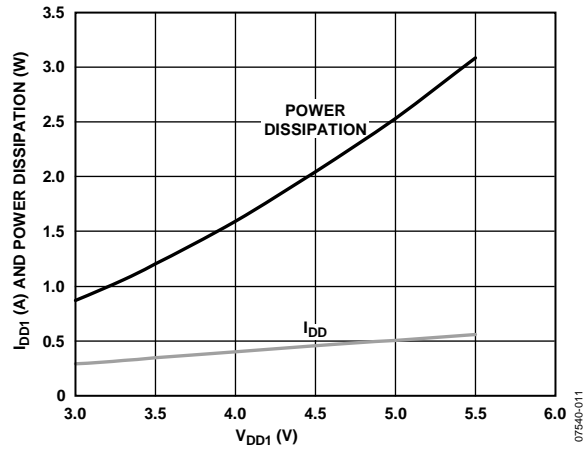


Figure 12. Typical Short-Circuit Input Current and Power vs.  $V_{DD1}$  Supply Voltage

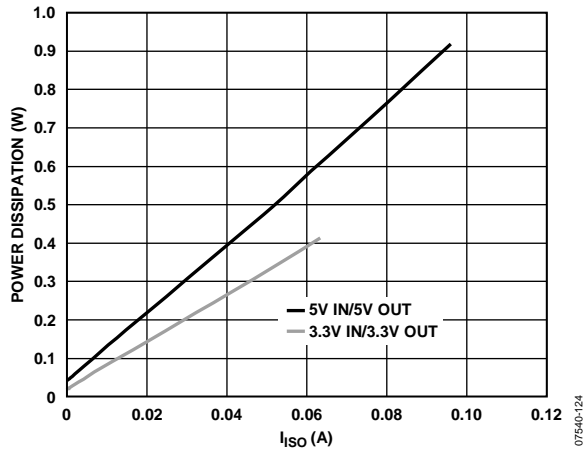


Figure 10. Typical Total Power Dissipation vs.  $I_{ISO}$  with Data Channels Idle

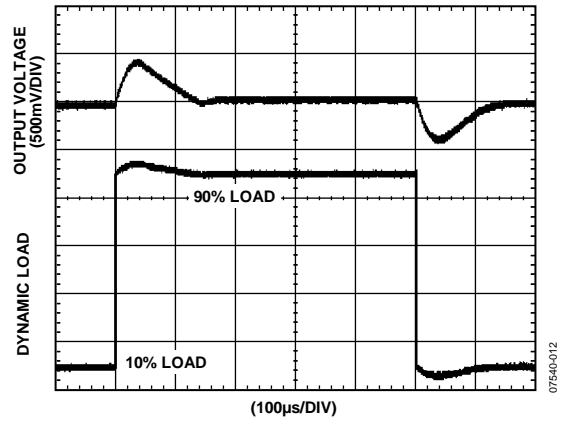


Figure 13. Typical  $V_{ISO}$  Transient Load Response 5 V Output 10% to 90% Load Step

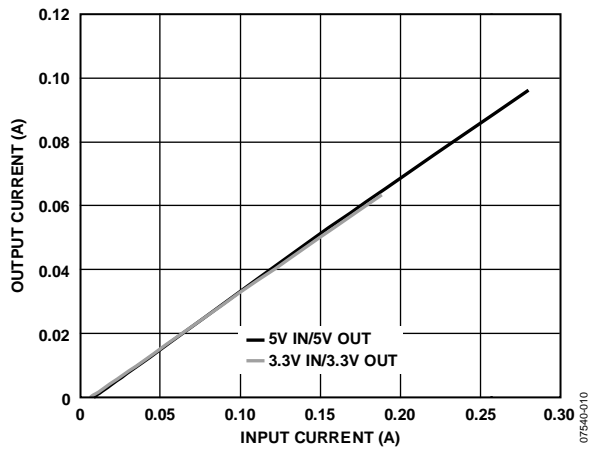


Figure 11. Typical Isolated Output Supply Current,  $I_{ISO}$  as a Function of External Load, No Dynamic Current Draw at 5 V/5 V and 3.3 V/3.3 V

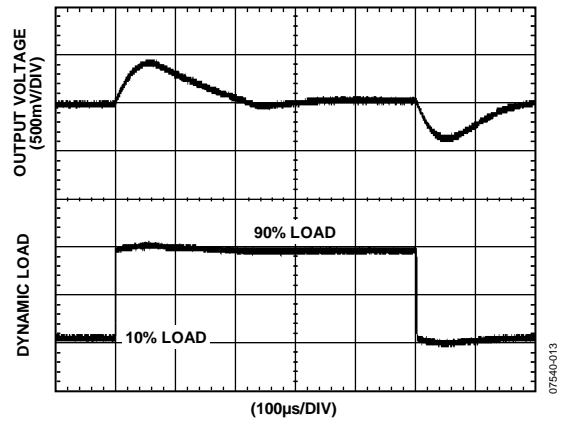


Figure 14. Typical Transient Load Response 3 V Output 10% to 90% Load Step

# ADuM5200/ADuM5201/ADuM5202

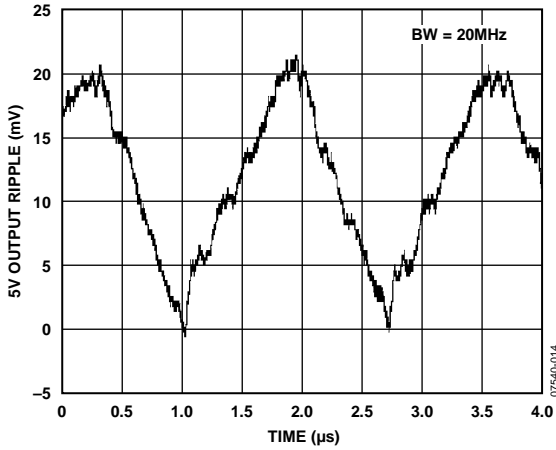


Figure 15. Typical  $V_{ISO} = 5V$  Output Voltage Ripple at 90% Load

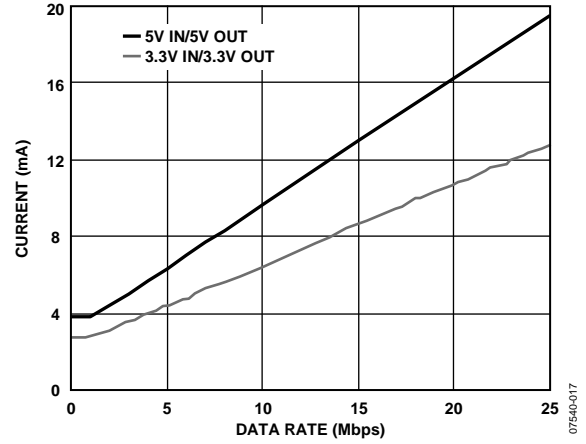


Figure 18. Typical  $I_{CH}$  Supply Current per Reverse Data Channel (15 pF Output Load)

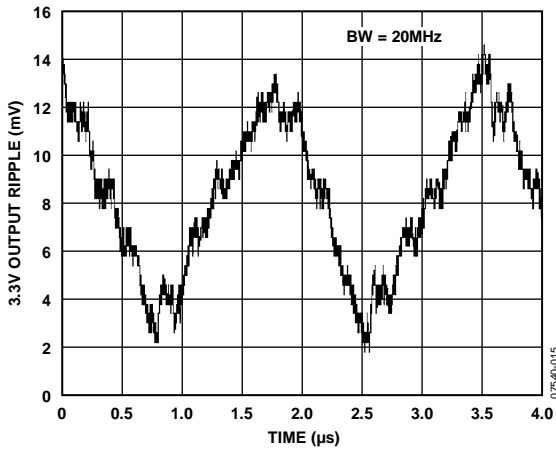


Figure 16. Typical  $V_{ISO} = 3.3V$  Output Voltage Ripple at 90% Load

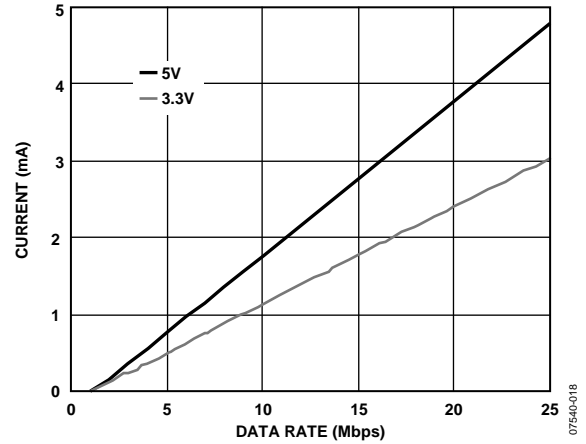


Figure 19. Typical  $I_{ISO(D)}$  Dynamic Supply Current per Input

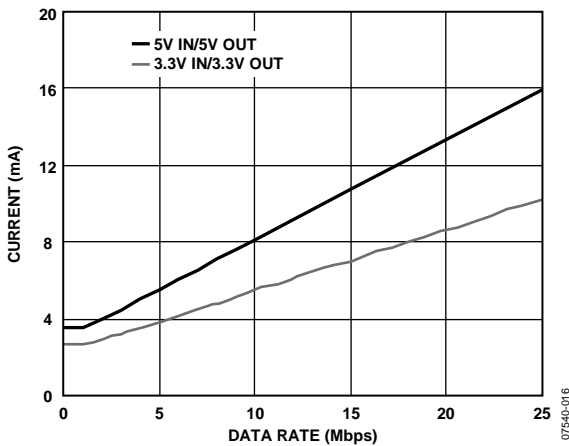


Figure 17. Typical  $I_{CH}$  Supply Current per Forward Data Channel (15 pF Output Load)

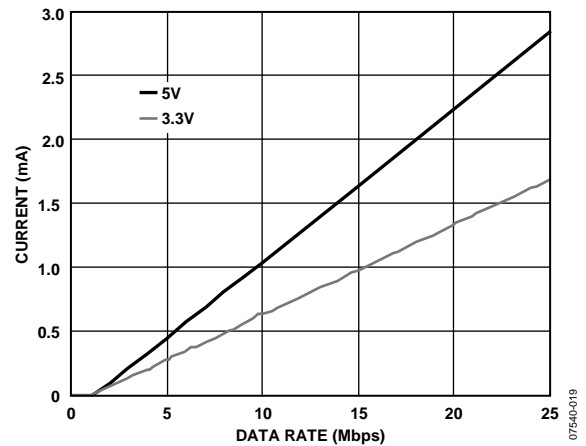


Figure 20. Typical  $I_{ISO(D)}$  Dynamic Supply Current per Output (15 pF Output Load)

## TERMINOLOGY

### $I_{DD1(Q)}$

$I_{DD1(Q)}$  is the minimum operating current drawn at the  $V_{DD1}$  pin when there is no external load at  $V_{ISO}$  and the I/O pins are operating below 2 Mbps, requiring no additional dynamic supply current.  $I_{DD1(Q)}$  reflects the minimum current operating condition.

### $I_{DD1(D)}$

$I_{DD1(D)}$  is the typical input supply current with all channels simultaneously driven at a maximum data rate of 25 Mbps with the full capacitive load representing the maximum dynamic load conditions. Treat resistive loads on the outputs separately from the dynamic load.

### $I_{DD1(MAX)}$

$I_{DD1(MAX)}$  is the input current under full dynamic and  $V_{ISO}$  load conditions.

### $t_{PHL}$ Propagation Delay

$t_{PHL}$  propagation delay is measured from the 50% level of the falling edge of the  $V_{IX}$  signal to the 50% level of the falling edge of the  $V_{OX}$  signal.

### $t_{PLH}$ Propagation Delay

$t_{PLH}$  propagation delay is measured from the 50% level of the rising edge of the  $V_{IX}$  signal to the 50% level of the rising edge of the  $V_{OX}$  signal.

### Propagation Delay Skew ( $t_{PSK}$ )

$t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

### Channel-to-Channel Matching

Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels when operated with identical loads.

### Minimum Pulse Width

The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

### Maximum Data Rate

The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

## APPLICATIONS INFORMATION

The dc-to-dc converter section of the ADuM520x works on principles that are common to most power supplies. It has a secondary side controller architecture with isolated pulse-width modulation (PWM) feedback.  $V_{DD1}$  power is supplied to an oscillating circuit that switches current into a chip scale air core transformer. Power transferred to the secondary side is rectified and regulated to either 3.3 V or 5 V. The secondary ( $V_{ISO}$ ) side controller regulates the output by creating a PWM control signal that is sent to the primary ( $V_{DD1}$ ) side by a dedicated *iCoupler* data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

The ADuM520x implements undervoltage lockout (UVLO) with hysteresis on the  $V_{DD1}$  power input. This feature ensures that the converter does not enter oscillation due to noisy input power or slow power on ramp rates.

A minimum load current of 10 mA is recommended to ensure optimum load regulation. Smaller loads can generate excess noise on chip due to short or erratic PWM pulses. Excess noise generated this way can cause data corruption in some circumstances.

The ADuM520x can accept an external regulation control signal ( $RC_{IN}$ ) that can be connected to other *isoPower* devices. This allows a single regulator to control multiple power modules without contention. When accepting control from a master power module, the  $V_{ISO}$  pins can be connected together adding their power. Because there is only one feedback control path, the supplies work together seamlessly. The ADuM520x can only regulate itself or accept regulation (slave device) from another device in this product line; it cannot provide a regulation signal to other devices.

### PCB LAYOUT

The ADuM520x digital isolators with 0.5 W *isoPower* integrated dc-to-dc converters require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 21). Note that low ESR bypass capacitors are required between Pin 1 and Pin 2 and between Pin 15 and Pin 16, as close to the chip pads as possible.

The power supply section of the ADuM520x uses a 180 MHz oscillator frequency to efficiently pass power through its chip scale transformers. In addition, normal operation of the data section of the *iCoupler* introduces switching transients on the power supply pins. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor, whereas ripple suppression and proper regulation require a large value capacitor. These are most conveniently connected between Pin 1 and Pin 2 for  $V_{DD1}$  and between Pin 15 and Pin 16 for  $V_{ISO}$ . To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1  $\mu\text{F}$  and 10  $\mu\text{F}$  for  $V_{DD1}$ . The smaller capacitor must have a low ESR; for example, use of a ceramic capacitor is advised.

Note that the total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm. Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption. Consider bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 unless both of the common ground pins are connected together close to the package.

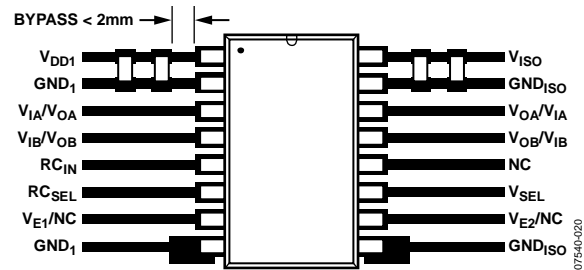


Figure 21. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause differential voltages between pins exceeding the absolute maximum ratings for the device (specified in Table 8) thereby leading to latch-up and/or permanent damage.

The ADuM520x is a power device that dissipates approximately 1 W of power when fully loaded and running at maximum speed. Because it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipation into the PCB through the GND pins. If the device is used at high ambient temperatures, provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 21 shows enlarged pads for Pin 2, Pin 8, Pin 9, and Pin 15. Multiple vias should be implemented from the pad to the ground plane to significantly reduce the temperature inside the chip. The dimensions of the expanded pads are at the discretion of the designer and depend on the available board space.

### EMI CONSIDERATIONS

The dc-to-dc converter section of the ADuM520x components must operate at a very high frequency to allow efficient power transfer through the small transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge emissions and dipole radiation between the primary and secondary ground planes. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, follow good RF design practices in layout of the PCB. See [www.analog.com](http://www.analog.com) for the most current PCB layout recommendations specifically for the ADuM520x.

## PROPAGATION DELAY PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high.

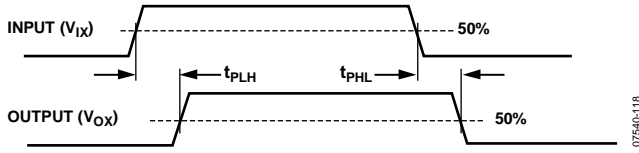


Figure 22. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM520x component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM520x components operating under the same conditions.

## DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 μs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 13) by the watchdog timer circuit.

The limitation on the magnetic field immunity of the ADuM520x is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM520x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum\pi r_n^2; n = 1, 2, \dots, N$$

where:

$\beta$  is the magnetic flux density (gauss).

$N$  is the number of turns in the receiving coil.

$r_n$  is the radius of the  $n^{\text{th}}$  turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM520x and an imposed requirement that the induced voltage be, at most,

50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 23.

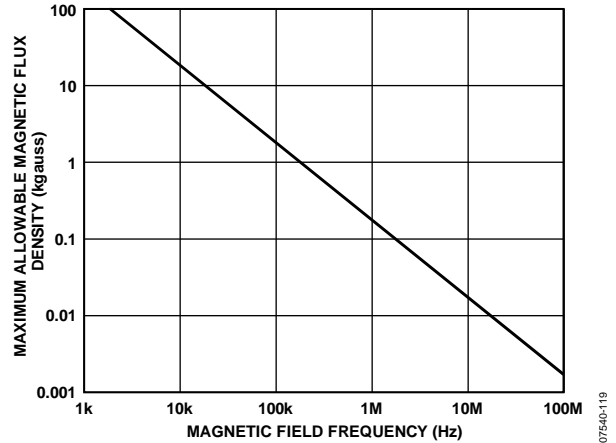


Figure 23. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM520x transformers. Figure 24 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM520x is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, a 0.5 kA current placed 5 mm away from the ADuM520x is required to affect the operation of the component.

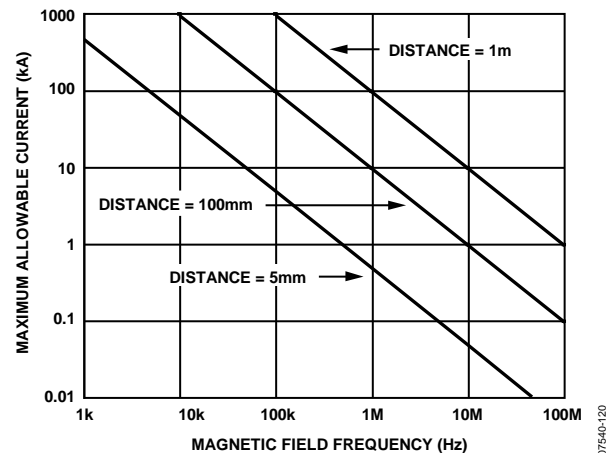


Figure 24. Maximum Allowable Current for Various Current-to-ADuM520x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error

# ADuM5200/ADuM5201/ADuM5202

voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The  $V_{DD1}$  power supply input provides power to the iCoupler data channels as well as to the power converter. For this reason, the quiescent currents drawn by the data converter and the primary and secondary input/output channels cannot be determined separately. All of these quiescent power demands have been combined into the  $I_{DD1(Q)}$  current shown in Figure 25. The total  $I_{DD1}$  supply current is the sum of the quiescent operating current, dynamic current  $I_{DD1(D)}$  demanded by the I/O channels, and any external  $I_{ISO}$  load.

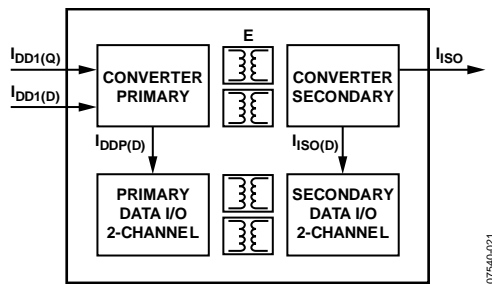


Figure 25. Power Consumption Within the ADuM520x

Both dynamic input and output current is consumed only when operating at channel speeds higher than the rate of  $f_r$ . Because each channel has a dynamic current determined by its data rate, Figure 17 shows the current for a channel in the forward direction, which means that the input is on the primary side of the part. Figure 18 shows the current for a channel in the reverse direction, which means that the input is on the secondary side of the part. Both figures assume a typical 15 pF load. The following relationship allows the total  $I_{DD1}$  current to be calculated:

$$I_{DD1} = (I_{ISO} \times V_{ISO}) / (E \times V_{DD1}) + \sum I_{CHn}; n = 1 \text{ to } 4 \quad (1)$$

where :

$I_{DD1}$  is the total supply input current.

$I_{CHn}$  is the current drawn by a single channel determined from Figure 17 or Figure 18, depending on channel direction.

$I_{ISO}$  is the current drawn by the secondary side external loads.

$E$  is the power supply efficiency at 100 mA load from Figure 9 at the  $V_{ISO}$  and  $V_{DD1}$  condition of interest.

Calculate the maximum external load by subtracting the dynamic output load from the maximum allowable load.

$$I_{ISO(LOAD)} = I_{ISO(MAX)} - \sum I_{ISO(D)n}; n = 1 \text{ to } 4 \quad (2)$$

where:

$I_{ISO(LOAD)}$  is the current available to supply an external secondary side load.

$I_{ISO(MAX)}$  is the maximum external secondary side load current available at  $V_{ISO}$ .

$I_{ISO(D)n}$  is the dynamic load current drawn from  $V_{ISO}$  by an input or output channel, as shown in Figure 17 and Figure 18. Data is presented assuming a typical 15 pF load

The preceding analysis assumes a 15 pF capacitive load on each data output. If the capacitive load is larger than 15 pF, the additional current must be included in the analysis of  $I_{DD1}$  and  $I_{ISO(LOAD)}$ .

To determine  $I_{DD1}$  in Equation 1, additional primary side dynamic output current ( $I_{AOD}$ ) is added directly to  $I_{DD1}$ . Additional secondary side dynamic output current ( $I_{AOD}$ ) is added to  $I_{ISO}$  on a per channel basis.

To determine  $I_{ISO(LOAD)}$  in Equation 2, additional secondary side output current ( $I_{AOD}$ ) is subtracted from  $I_{ISO(MAX)}$  on a per channel basis.

For each output channel with  $C_L$  greater than 15 pF, the additional capacitive supply current is given by

$$I_{AOD} = 0.5 \times 10^{-3} \times (C_L - 15) \times V_{ISO} \times (2f - f_r) \quad f > 0.5 f_r \quad (3)$$

where:

$C_L$  is the output load capacitance (pF).

$V_{ISO}$  is the output supply voltage (V).

$f$  is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.

$f_r$  is the input channel refresh rate (Mbps).

## CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADuM520x is protected against damage due to excessive power dissipation by thermal overload protection circuits. Thermal overload protection limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature starts to rise above 150°C, the PWM is turned off, reducing the output current to zero. When the junction temperature drops below 130°C (typical), the PWM turns on again, restoring the output current to its nominal value.

Consider the case where a hard short from  $V_{ISO}$  to ground occurs. At first, the ADuM520x reaches its maximum current, which is proportional to the voltage applied at  $V_{DD1}$ . Power dissipates on the primary side of the converter (see Figure 12). If self-heating of the junction becomes great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the PWM and reducing the output current to zero. As the junction temperature cools and drops below 130°C, the PWM turns on and power dissipates again on the primary side of the converter, causing the junction temperature to rise to 150°C again. This thermal oscillation between 130°C and 150°C causes the part to cycle on and off as long as the short remains at the output.

Thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, externally limit device power dissipation to prevent junction temperatures from exceeding 130°C.

## POWER CONSIDERATIONS

The ADuM5200/ADuM5201/ADuM5202 power input, data input channels on the primary side, and data input channels on the secondary side are all protected from premature operation by UVLO circuitry. Below the minimum operating voltage, the power converter holds its oscillator inactive and all input channel drivers and refresh circuits are idle. Outputs remain in a high impedance state to prevent transmission of undefined states during power-up and power-down operations.

During application of power to  $V_{DD1}$ , the primary side circuitry is held idle until the UVLO preset voltage is reached. At that time, the data channels initialize to their default low output state until they receive data pulses from the secondary side.

When the primary side is above the UVLO threshold, the data input channels sample their inputs and begin sending encoded pulses to the inactive secondary output channels. The outputs on the primary side remain in their default low state because no data comes from the secondary side inputs until secondary power is established. The primary side oscillator also begins to operate, transferring power to the secondary power circuits. The secondary  $V_{ISO}$  voltage is below its UVLO limit at this point; the regulation control signal from the secondary is not being generated. The primary side power oscillator is allowed to free run in this circumstance, supplying the maximum amount of power to the secondary, until the secondary voltage rises to its regulation setpoint. This creates a large inrush current transient at  $V_{DD1}$ . When the regulation point is reached, the regulation control circuit produces the regulation control signal that modulates the oscillator on the primary side. The  $V_{DD1}$  current is reduced and is then proportional to the load current. The inrush current is less than the short-circuit current shown in Figure 12. The duration of the inrush depends on the  $V_{ISO}$  loading conditions and the current available at the  $V_{DD1}$  pin.

As the secondary side converter begins to accept power from the primary, the  $V_{ISO}$  voltage starts to rise. When the secondary side UVLO is reached, the secondary side outputs are initialized to their default low state until data is received from the corresponding primary side input. It can take up to 1  $\mu$ s after the secondary side is initialized for the state of the output to correlate with the primary side input.

Secondary side inputs sample their state and transmit it to the primary side. Outputs are valid about 1  $\mu$ s after the secondary side becomes active.

Because the rate of charge of the secondary side power supply is dependent on loading conditions, the input voltage, and the output voltage level selected, take care with the design to allow the converter sufficient time to stabilize before valid data is required.

When power is removed from  $V_{DD1}$ , the primary side converter and coupler shut down when the UVLO level is reached. The secondary side stops receiving power and starts to discharge. The outputs on the secondary side hold the last state that they received from the primary side. Either the UVLO level is reached and the

outputs are placed in their high impedance state, or the outputs detect a lack of activity from the primary side inputs and the outputs are set to their default low value before the secondary power reaches UVLO.

## THERMAL ANALYSIS

The ADuM520x consists of four internal die, attached to a split lead frame with two die attach paddles. For the purposes of thermal analysis, it is treated as a thermal unit with the highest junction temperature reflected in the  $\theta_{JA}$  from Table 3. The value of  $\theta_{JA}$  is based on measurements taken with the part mounted on a JEDEC standard 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM520x operates at full load across the full temperature range without derating the output current. However, following the recommendations in the PCB Layout section decreases the thermal resistance to the PCB allowing increased thermal margin at high ambient temperatures.

## INCREASING AVAILABLE POWER

The ADuM520x devices are designed with the capability of running in combination with other compatible *isoPower* devices. The  $RC_{IN}$  and  $RC_{SEL}$  pins allow the ADuM520x to receive a PWM signal from another device through the  $RC_{IN}$  pin and act as a slave to that control signal. The  $RC_{SEL}$  pin chooses whether the part acts as a standalone self-regulated device or a slave device. When the ADuM520x is acting as a slave, its power is regulated by a PWM signal coming from a master device. This allows multiple *isoPower* parts to be combined in parallel while sharing the load equally. When the ADuM520x is configured as a standalone unit, it generates its own PWM feedback signal to regulate itself.

The ADuM5000 can act as a master or a slave device, the ADuM5401, ADuM5402, ADuM5403, and ADuM5404 can only be master/standalone, and the ADuM520x can only be a slave/standalone device. This means that the ADuM5000, ADuM520x, and ADuM5401 to ADuM5404 can only be used in certain master/slave combinations as listed in Table 14.

**Table 14. Allowed Combinations of *isoPower* Parts**

Master	Slave		
	ADuM5000	ADuM520x	ADuM5401 to ADuM5404
ADuM5000	Yes	Yes	No
ADuM520x	No	No	No
ADuM5401 to ADuM5404	Yes	Yes	No

The allowed combinations of master and slave configured parts listed in Table 14 is sufficient to make any combination of power and channel count.

Table 15 illustrates how *isoPower* devices can provide many combinations of data channel count and multiples of the single unit power.

# ADuM5200/ADuM5201/ADuM5202

**Table 15. Configurations for Power and Data Channels**

Power Units	Number of Data Channels			
	0	2	4	6
<b>1-Unit Power</b>	ADuM5000 master	ADuM520x master	ADuM5401 to ADuM5404 master	ADuM5401 to ADuM5404 master ADuM121x
<b>2-Unit Power</b>	ADuM5000 master ADuM5000 slave	ADuM5000 master ADuM520x slave	ADuM5401 to ADuM5404 master ADuM520x slave	ADuM5401 to ADuM5404 master ADuM520x slave
<b>3-Unit Power</b>	ADuM5000 master ADuM5000 slave ADuM5000 slave	ADuM5000 master ADuM5000 slave ADuM520x slave	ADuM5401 to ADuM5404 master ADuM5000 slave ADuM5000 slave	ADuM5401 to ADuM5404 master ADuM520x slave ADuM5000 slave

## INSULATION LIFETIME

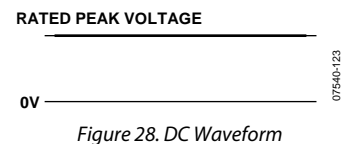
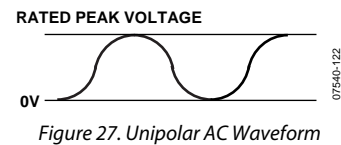
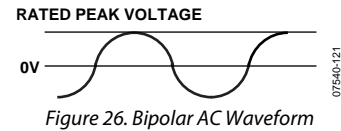
All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM520x.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 9 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition, and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than a 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

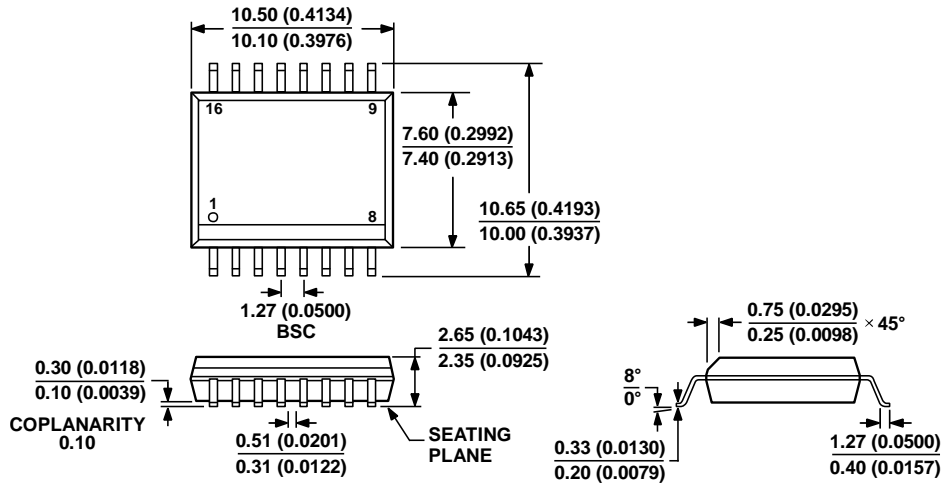
The insulation lifetime of the ADuM520x depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 26, Figure 27, and Figure 28 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 9 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross insulation voltage waveform that does not conform to Figure 27 or Figure 28 should be treated as a bipolar ac waveform and its peak voltage limited to the 50-year lifetime voltage value listed in Table 9. The voltage presented in Figure 27 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.



## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 29. 16-Lead Standard Small Outline Package [SOIC\_W]  
 Wide Body (RW-16)  
 Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model	Number of Inputs, V <sub>DD1</sub> Side	Number of Inputs, V <sub>DD2</sub> Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Description	Package Option
ADuM5200ARWZ <sup>1,2</sup>	2	0	1	100	40	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5200CRWZ <sup>1,2</sup>	2	0	25	70	3	-40°C to +105°C	16-Lead SOIC_W	RW-16
<b>CAN :</b> ADuM5201ARWZ <sup>1,2</sup>	<b>1</b>	<b>1</b>	<b>1</b>	<b>100</b>	<b>40</b>	<b>-40°C to +105°C</b>	<b>16-Lead SOIC_W</b>	<b>RW-16</b>
ADuM5201CRWZ <sup>1,2</sup>	1	1	25	70	3	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5202ARWZ <sup>1,2</sup>	0	2	1	100	40	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5202CRWZ <sup>1,2</sup>	0	2	25	70	3	-40°C to +105°C	16-Lead SOIC_W	RW-16

<sup>1</sup> Tape and reel are available. The additional -RL suffix designates a 13-inch (1,000 units) tape and reel option.

<sup>2</sup> Z = RoHS Compliant Part.

**NOTES**