

## Reliability Data Sheet

### Description

The reliability data shown includes Avago Technologies reliability test data from the reliability qualification done on this product family. All of these products use the same LEDs, similar IC, and the same packaging materials, processes, stress conditions and testing. The data in Table 1 and Table 2 reflect actual test data for devices on a per channel basis. Before stress, all devices are preconditioned at MSL 1 using a solder reflow process (260°C peak temp) and 20 temperature cycles (-55°C to +125°C, 15 mins dwell, 1 min transfer). These data are taken from testing on Avago Technologies devices using internal Avago Technologies process, material specifications, design standards, and statistical process controls. **THEY ARE NOT TRANSFERABLE TO OTHER MANUFACTURERS' SIMILAR PART TYPES.**

### Operating Life Test

For valid system reliability calculations it is necessary to adjust for the time when the system is not in operation. Note that if you are using MIL-HDBK-217 for predicting component reliability, the results may not be comparable to those given in Table 2 due to different conditions and factors that have been accounted for in MIL-HDBK-217. For example it is unlikely that your application will exercise all available channels at full rated power with the LED(s) always ON as Avago Technologies testing does. Thus, your application total power and duty cycle must be carefully considered when comparing Table 2 to predictions using MIL-HDBK-217.

### Definition of Failure

Inability to switch, i.e. "functional failure" is the definition of failure in this data sheet. Specifically, failure occurs when the device fails to switch ON with 2 times the minimum recommended drive current (but not exceeding the max rating) or fails to switch off when there is no input current

### Failure Rate Projections

The demonstrated point mean time to failure (MTTF) is measured at the absolute maximum stress condition. The failure rate projections in Table 2 uses the Arrhenius acceleration relationship, where a 0.43 eV activation energy is used as in the hybrid section of MIL-HDBK-217.

### Application Information

The data of Table 1 and 2 were obtained on devices with high temperature operating life duration. An exponential (random) failure distribution is assumed, expressed in units of FIT (failures per billion device hours) are only defined in the random failure portion of the reliability curve.

**Table 1. Demonstrated Operating Life Test Performance**

Stress Test Condition	Total Device Tested	Total Device Hours	Number of Failed Units	Demonstrated MTTF(hr) @ Ta = 125 °C	Demonstrated FITs @ Ta = 125 °C
Ta = 125 °C If=12mA Vdd=5.5V Io=10mA	1018	1,095,000	0	> 1.095,000	<913

**Table 2. Reliability Projection for Device Listed in Title**

Ambient Temperature (°C)	Junction Temperature (°C)	Typical (60% Confidence)		90% Confidence	
		MTTF (Hr/fail)	FITs (Fail/10 <sup>9</sup> h)	MTTF (Hr/fail)	FITs (Fail/10 <sup>9</sup> h)
125	140	1,195,036	837	475,552	2,103
120	135	1,385,449	722	551,326	1,814
110	125	1,883,000	531	749,321	1,335
100	115	2,600,034	385	1,034,658	967
90	105	3,651,926	274	1,453,248	688
80	95	5,224,968	191	2,079,224	481
70	85	7,626,685	131	3,034,963	329
60	75	11,376,999	88	4,527,363	221
50	65	17,377,901	58	6,915,362	145
40	55	27,238,586	37	10,839,323	92
30	45	43,918,524	23	17,476,938	57
25	40	56,409,270	18	22,447,506	45

**Table 3. Mechanical Tests (Testing done on a constructional basis)**

Test Name	Reference Standard	Test Conditions	Units Tested	Units Failed
Temp Cycling	JESD-A104	-55 to 125 °C Transfer = 1 min Dwell = 15 mins 1000 cycles	154	0
Physical Dimensions	JESD-B100	Conformance to datasheet package drawings	30	0
Solderability (RoHS condition)	JESD-B102	8hrs steam aging (93 °C), followed by solder dip (260 °C,5sec)	10	0
Preconditioning	J-STD-20 JA113	As per reference standard ( to conform to MSL 1)	540	0

**Table 4. Environmental Testing**

Test Name	Reference Standard	Test Conditions	Units Tested	Units Failed
Highly Accelerated Stress Test	JESD-A110	Ta = 130 °C, RH=85% Vo=Vcc=5.5V Time = 96 hrs	38	0
Low Temperature Operating Life Test	JESD-A108	Ta = -40 °C If=20mA Vdd=5.5V Io=10mA	32	0
Temperature Humidity (without Bias)	JESD-A101	Ta = 85 °C, RH =85% Unbiased Time = 1000 hrs	50	0
High Temperature Bake	JESD-A103	Ta = 150 °C Unbiased Time = 1000hrs	50	0

For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries. Data subject to change. Copyright © 2005-2012 Avago Technologies. All rights reserved. AV02-2423EN - June 13, 2012

