



HS-81C55RH HS-81C56RH

Radiation Hardened
256 x 8 CMOS RAM

December 1992

T-46-23-12

Features

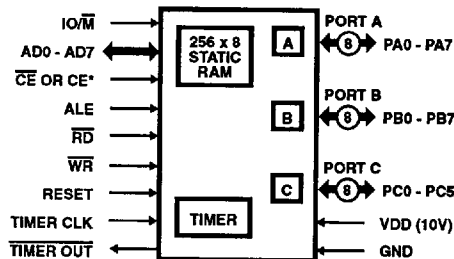
- Radiation Hardened EPI-CMOS
 - Parametrics Guaranteed 1×10^5 RAD(Si)
 - Transient Upset $> 1 \times 10^8$ RAD(Si)/s
 - Latch-Up Free $> 1 \times 10^{12}$ RAD(Si)/s
- Electrically Equivalent to Sandia SA 3001
- Pin Compatible with Intel 8155/56
- Bus Compatible with HS-80C85RH
- Single 5V Power Supply
- Low Standby Current 200 μ A Max
- Low Operating Current 2mA/MHz
- Completely Static Design
- Internal Address Latches
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Multiplexed Address and Data Bus
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range -55°C to +125°C

Description

The HS-81C55/56RH are radiation hardened RAM and I/O chips fabricated using the Harris radiation hardened Self-Aligned Junction Isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

The HS-81C55/56RH is intended for use with the HS-80C85RH radiation hardened microprocessor system. The RAM portion is designed as 2048 static cells organized as 256 x 8. A maximum post irradiation access time of 500ns allows the HS-81C55/56RH to be used with the HS-80C85RH CPU without any wait states. The HS-81C55RH requires an active low chip enable while the HS-81C56RH requires an active high chip enable. These chips are designed for operation utilizing a single 5V power supply.

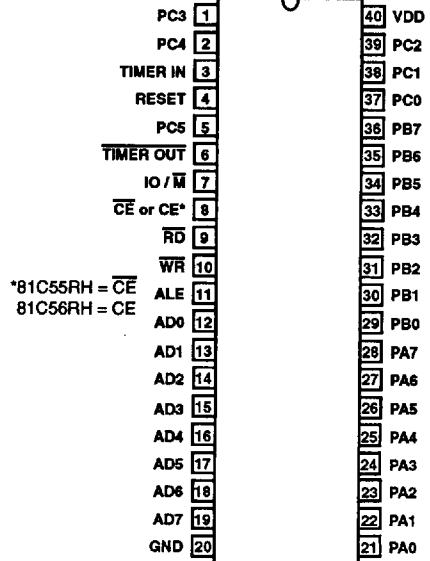
Functional Diagram



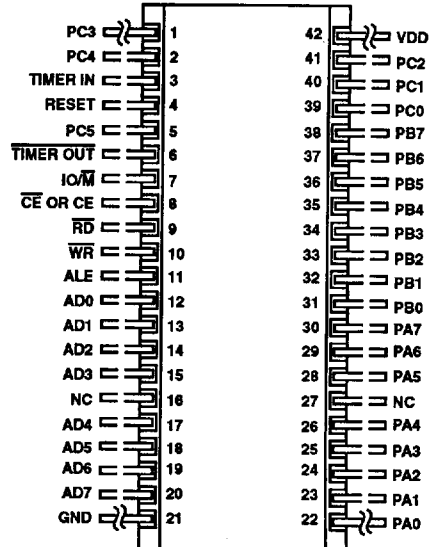
*81C55RH = \overline{CE}
81C56RH = CE

Pinouts

40 PIN CERAMIC DIP
CASE OUTLINE D5, CONFIGURATION 3
TOP VIEW



42 PIN FLATPACK
INTERNAL PACKAGE CODE HWN
TOP VIEW



HS-81C55RH, HS-81C56RH**Pin Description**

SYMBOL	TYPE	NAME AND FUNCTION
RESET	I	Reset: Pulse provided by the HS-80C85RH to initialize the system (connect to HS-80C85RH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two HS-80C85RH clock cycle times.
AD0 - AD7	I/O	Address/Data: Tri-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the HS-81C55 and HS-81C56RH on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/M input. The 8-bit data is either written into the chip or read from the chip, depending on the WR or RD input signal.
\overline{CE} or CE	I	Chip Enable: On the HS-81C55RH, this pin is \overline{CE} and is ACTIVE LOW. On the HS-81C56RH, this pin is CE and is ACTIVE HIGH.
\overline{RD}	I	Read Control: Input low on this line with the Chip Enable active enables and AD0 - AD7 buffers. If IO/M pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
\overline{WR}	I	Write Control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/M.
ALE	I	Address Latch Enable: This control signal latches both the address on the AD0 - AD7 lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.
IO/M	I	I/O Memory: Selects memory if low and I/O and command/status registers if high.
PA0 - PA7 (8)	I/O	Port A: These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB0 - PB7 (8)	I/O	Port B: These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC0 - PC7 (8)	I/O	Port C: These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC0 - PC5 are used as control signals, they will provide the following: PC0 - A INTR (Port A Interrupt) PC1 - A BF (Port A Buffer Full) PC2 - A STB (Port A Strobe) PC3 - B INTR (Port B Interrupt) PC4 - B BF (Port B Buffer Full) PC5 - B STB (Port B Strobe)
TIMER IN	I	Timer Input: Input to the counter-timer.
$\overline{TIMER OUT}$	O	Timer Output: This output can be either a square wave or a pulse, depending on the timer mode.
VDD	I	Voltage: +5V.
GND	I	Ground: Ground reference.

Specifications HS-81C55RH, HS-81C56RH

Absolute Maximum Ratings

Supply Voltage	+7.0V
Input, Output or I/O Voltage	GND-0.3V to VDD+0.3V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+175°C
Lead Temperature (Soldering 10s)	+300°C
Typical Derating Factor	2mA/MHz Increase in IDDOP
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	25.8°C/W	9.9°C/W
Braze Seal Flatpack Package	36.1°C/W	9.9°C/W
Maximum Package Power Dissipation at +125°C		
Braze Seal DIP Package	1.94W	
Braze Seal Flatpack Package	1.39W	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.75V to +5.25V	Input Low Voltage0V to +0.8V
Operating Temperature Range	-55°C to +125°C	Input High Voltage	VDD -0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Input Leakage Current	I _{IH}	VDD = 5.25V, V _{IN} = 0V, Pin under test = VDD	1, 2, 3	-55°C, +25°C, +125°C	-	1	µA
Low Input Leakage Current	I _{IL}	VDD = 5.25V, V _{IN} = 5.25V, Pin under test = 0V	1, 2, 3	-55°C, +25°C, +125°C	-1	-	µA
Low Output Voltage	VOL	VDD = 5.25V, I _{OL} = 2mA	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
High Output Voltage	VOH	VDD = 4.75V, I _{OH} = 2mA	1, 2, 3	-55°C, +25°C, +125°C	4.25	-	V
Static Current	IDDSB	VDD = 5.25V	1, 2, 3	-55°C, +25°C, +125°C	-	200	µA
Dynamic Current	IDDOP	VDD = 5.25V, f = 1MHz	1, 2, 3	-55°C, +25°C, +125°C	-	2	mA
Functional Tests	FT	VDD = 4.75V and 5.25V, V _{IH} = VDD-0.5V, V _{IL} = 0.8V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTE: All devices are guaranteed at worst case limits and over radiation. Dynamic current is proportional to operating frequency (2mA/MHz).

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Latch Setup Time	TAL	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	60	-	ns
Address Hold Time After Latch	TLA	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	60	-	ns
Latch to READ/WRITE Control	TLC	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	200	-	ns
Valid Data Out From Read Control	TRD	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	250	ns
Address Stable to Data Out Valid	TAD	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	500	ns
Latch Enable Width	TLL	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	200	-	ns
READ/WRITE Control to Latch Enable	TCL	Notes 1, 4, 7	9, 10, 11	-55°C ≤ T _A ≤ +125°C	20	-	ns
READ/WRITE Control Width	TCC	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	250	-	ns
Data In to WRITE Setup Time	TDW	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	200	-	ns
Data In Hold Time After WRITE	TWD	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	25	-	ns
WRITE to Port Output	TWP	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	300	ns

Specifications HS-81C55RH, HS-81C56RH

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Port Input Setup Time	TPR	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	50	-	ns
Port Input Hold Time	TRP	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	15	-	ns
Strobe to Buffer Full	TSBF	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	300	ns
Strobe Width	TSS	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	150	-	ns
READ to Buffer Empty	TRBE	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	300	ns
Strobe to INTR Off	TSI	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	300	ns
READ to INTR Off	TRDI	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C		360	ns
Port Setup Time to Strobe	TPSS	Notes 1, 4, 5	9, 10, 11	-55°C ≤ T _A ≤ +125°C	100	-	ns
Post Hold Time After Strobe	TPHS	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	100	-	ns
Strobe to Buffer Empty	TSBE	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	300	ns
WRITE to Buffer full	TWBF	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	300	ns
WRITE to INTR Off	TWI	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	340	ns
TIMER-IN to TIMER OUT Low	TTL	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	300	ns
TIMER-IN to TIMER-OUT High	TTH	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	-	300	ns
Data Bus Enable from READ Control	TRDE	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	120	-	ns
TIMER-IN Low Time	T1	Notes 1, 4, 6	9, 10, 11	-55°C ≤ T _A ≤ +125°C	40	-	ns
TIMER-IN High Time	T2	Notes 1, 4	9, 10, 11	-55°C ≤ T _A ≤ +125°C	115	-	ns

NOTES:

- All devices guaranteed at worst case limits and over radiation.
- Operating supply current (IDDOP) is proportional to operating frequency.
- Output timings are measured with purely capacitive load.
- For design purposes the limits are given as shown. For compatibility with the 80C85RH microprocessor, the AC parameters are tested as maximums.
- Parameter tested as part of the functional test. No read and record data available.
- At low temperature, T1 is measured down to 10ns. If the reading is less than 10ns, the parameter will read 10ns.
- Read and Record data available on failing data only.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground	T _A = +25°C	-	10	pF
I/O Capacitance	C I/O	VDD = Open, f = 1MHz, All measurements referenced to device ground	T _A = +25°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground	T _A = +25°C	-	10	pF
Data Bus Float After READ	TRDF	VDD = 4.75V	-55°C, +25°C, +125°C	10	100	ns
Recovery Time Between Controls	TRV	VDD = 4.75V	-55°C, +25°C, +125°C	-	220	ns

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

Specifications HS-81C55RH, HS-81C56RH

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

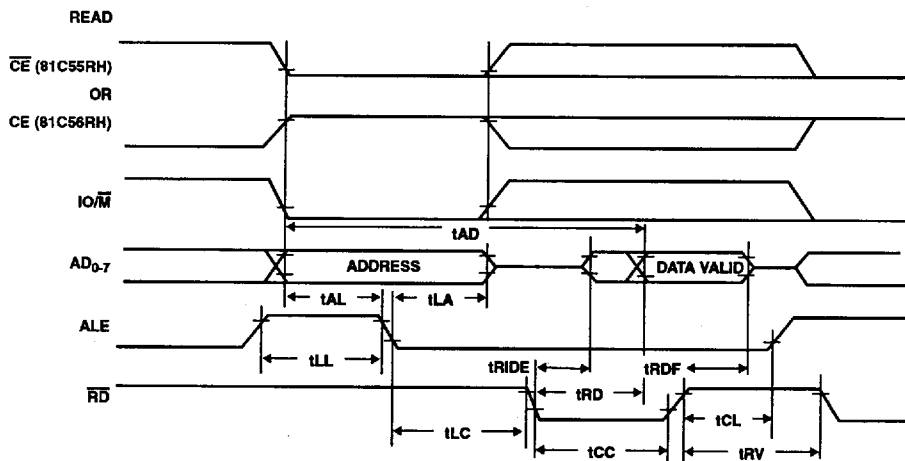
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current	IDDSB	$\pm 40\mu\text{A}$
Low Input Leakage Current	IIL	$\pm 100\text{nA}$
High Input Leakage Current	IiH	$\pm 100\text{nA}$
Low Level Output Voltage	VOL	$\pm 60\text{mV}$
High Level Output Voltage	VOH	$\pm 400\text{mV}$

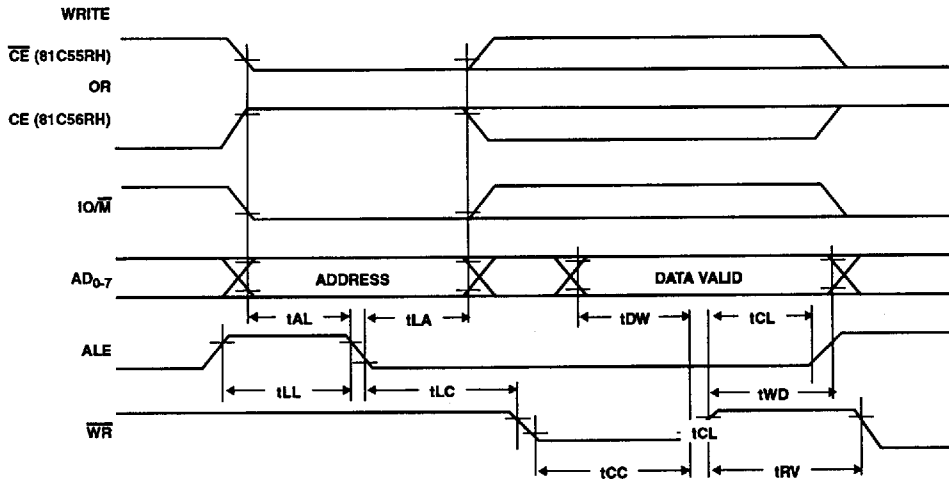
TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test	100%/5004	1, 7, 9
PDA	100%/5004	1, 7
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D Others	Samples/5004	1, 7
Group E Subgroup 2	Samples/5004	1, 7, 9

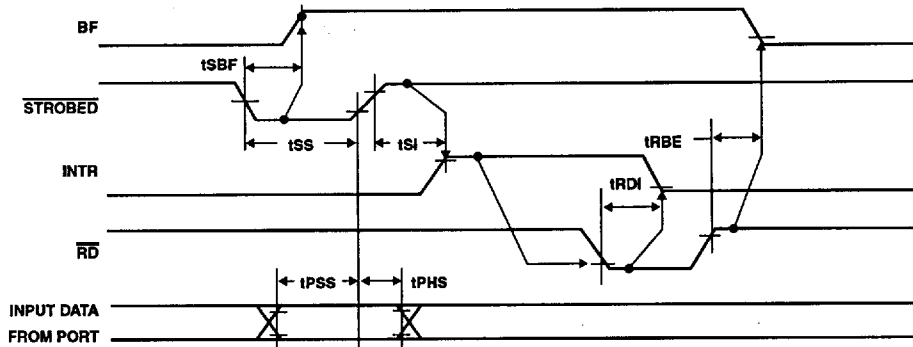
Waveforms



Waveforms (Continued)



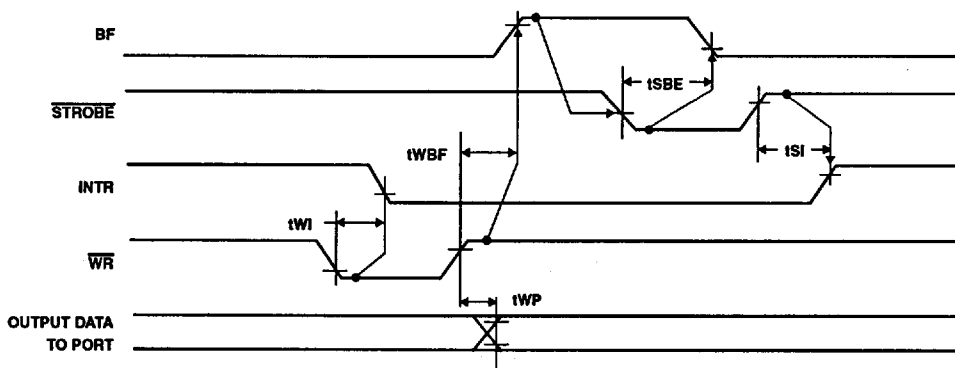
STROBED INPUT



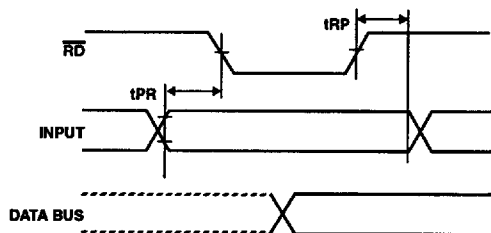
HS-81C55RH, HS-81C56RH

Waveforms (Continued)

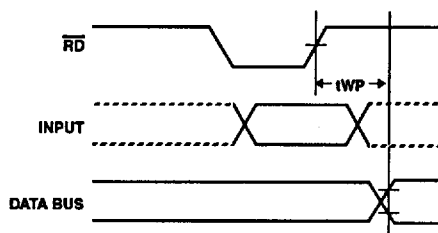
STROBED OUTPUT



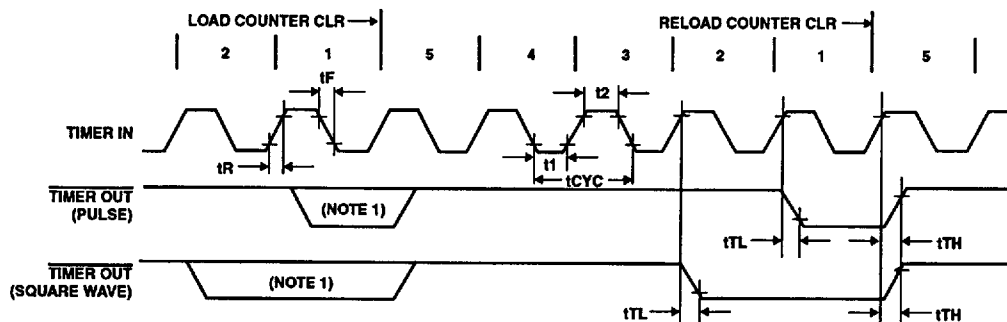
BASIC INPUT



BASIC INPUT



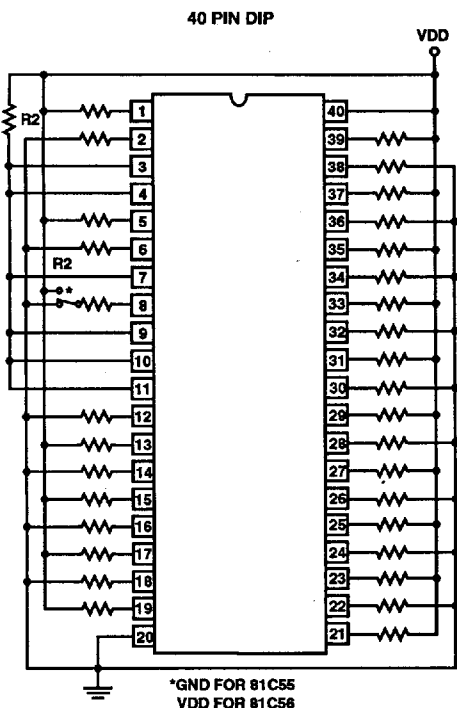
TIMER OUTPUT COUNTDOWN FROM 5 TO 1



NOTE: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M, MODE BIT = 1)

HS-81C55RH, HS-81C56RH

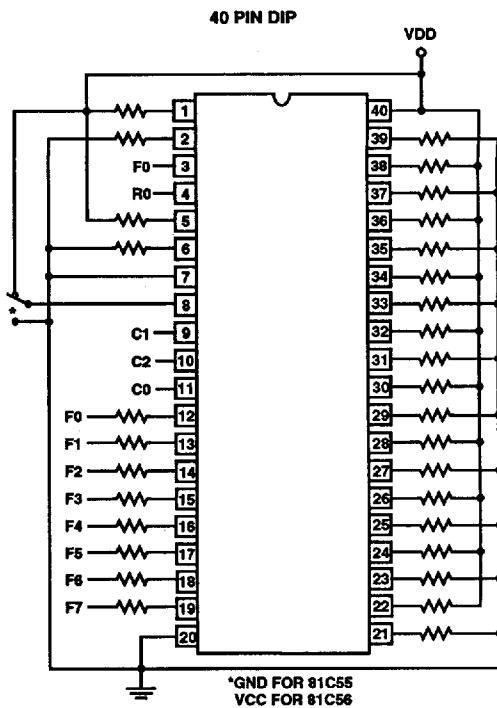
Burn-In Circuits



STATIC CONFIGURATION

NOTES:

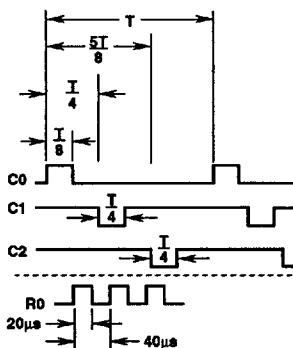
VDD = 10V ± 10%
 All resistors R1 = 100kΩ unless otherwise marked; R2 = 50K
 Pin 8 tied through a resistor to two position switch.
 Label ground side "81C55" and VDD side "81C56".



DYNAMIC CONFIGURATION

NOTES:

Minimum Temperature +125°C
 All resistors 100kΩ 1/4 Watt. VDD = 10V ± 10%.
 Pin 8 tied to two position switch. Label ground side "81C55" and VDD side "81C56".
 Period of C0 = C1 = C2 = T = 10μs
 C0 active HIGH, C1 and C2 active LOW.
 C0, C1, C2 cannot overlap each other.
 R0 shall have at least 3 pulses on power up as indicated below.
 Pulses shall stop and R0 shall go to 0V no more than 60 seconds after power-up.

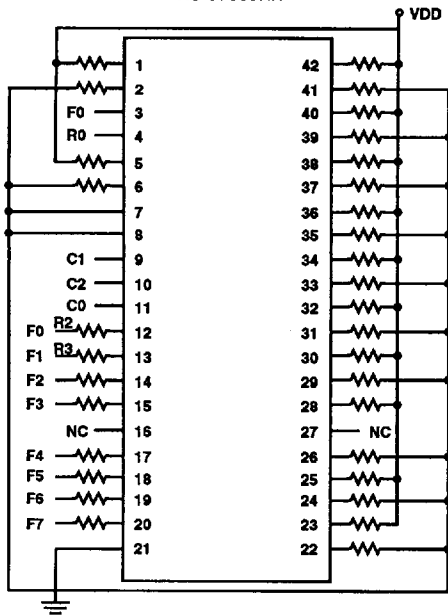


SIGNAL NAME	FREQUENCY	DUTY CYCLE
F0	50KHz	50%
F1	F0/2	50%
F2	F1/2	50%
F3	F2/2	50%
F4	F3/2	50%
F5	F4/2	50%
F6	F5/2	50%
F7	F6/2	50%

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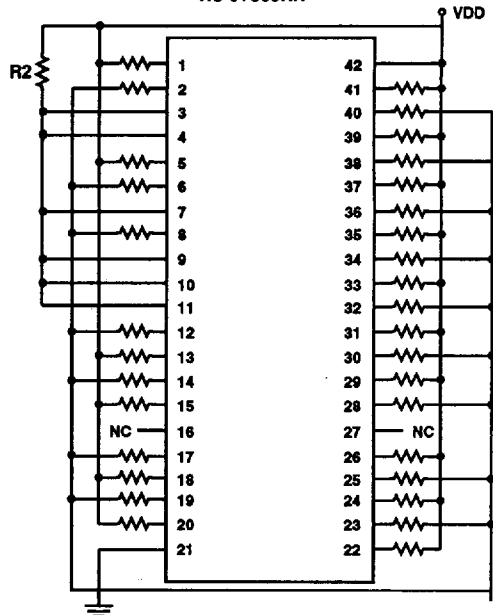
Burn-In Circuits (Continued)

**42 PIN FLATPACK
HS-81C55RH**



STATIC CONFIGURATION

**42 PIN FLATPACK
HS-81C55RH**



DYNAMIC CONFIGURATION

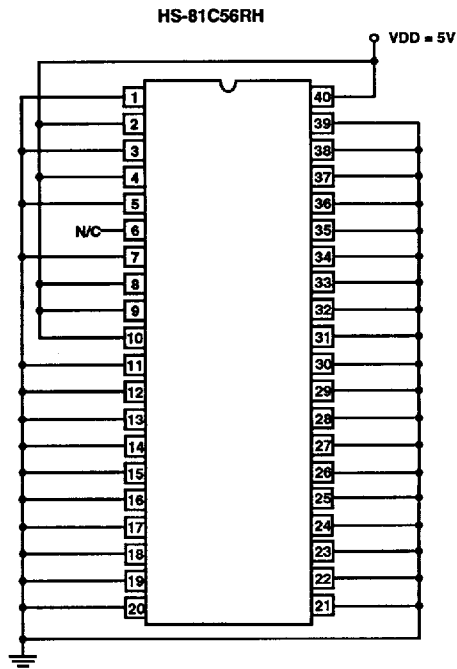
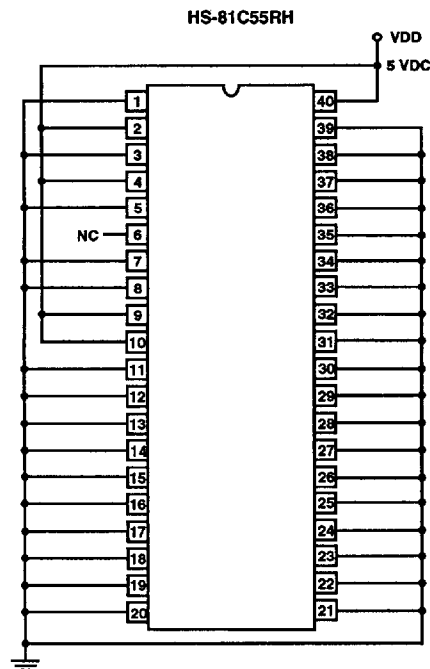
HS-81C55RH, HS-81C56RH**Radiation Screening Procedure**

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality, in a ceramic dip.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Ras(Si) +10% from a Gamma-cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Bias circuit is shown.
5. The sample devices shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-81C55RH and HS-81C56RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latching up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained when special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1×10^5 Rad(Si). Transient radiation tests have shown the following results:

- Latch-up free to doses $\geq 1 \times 10^{12}$ rads/sec.
- Upset (loss of stored data) $\geq 1 \times 10^8$ rads/sec.

Irradiation Circuits

HS-81C55RH, HS-81C56RH**Harris - Space Level Product Flow** (Note 1)

SEM - Traceable to Diffusion - Method 2018	Electrical Tests - Subgroup 1; Read and Record (T2)
Wafer Lot Acceptance Method 5007	Alternate Group A - Subgroups 1, 7, 9; Method 5005; Paragraph 3.5.1.1
Internal Visual Inspection - Method 2010, Condition A	Burn-In Delta Calculation (T0-T2)
Gamma Radiation Assurance Tests - Method 1019	PDA Calculation 3%: Subgroup 7 5% Subgroups 1, 7, Delta
Nondestructive Bond Pull - Method 2023	Electrical Tests - Subgroup 3; Read and Record
Customer Pre-Cap Visual Inspection (Notes 2)	Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Paragraph 3.5.1.1
Temperature Cycling - Method 1010, Condition C	Marking
Constant Acceleration - Method 2001, Condition E Min., Y1	Electrical Tests - Subgroup 2; Read and Record
Particle Impact Noise Detection - Method 2020, Condition A	Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Paragraph 3.5.1.1
Electrical Tests - Harris' Option	Fine and Gross Leak Tests - Method 1014, 100%
Serialization	Customer Source Inspection (Note 2)
X-Ray Inspection - Method 2012	Group B Inspection - Method 5005 (Notes 2)
Electrical Tests - Subgroup 1; Read and Record (T0)	End-Point Electrical Parameters: B5; Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11
Static Burn-In - Method 1015, Condition B, 72 Hours, +125°C Minimum	Group D Inspection - Method 5005 (Notes 2, 4)
Electrical Tests - Subgroup 1; Read and Record (T1)	End-Point Electrical Parameters: B5; Subgroups 1, 7, 9
Burn-In Delta Calculation (T0-T1)	External Visual Inspection - Method 2009
PDA Calculation 3%: Subgroup 7 5% Subgroups 1, 7, Delta	Data Package Generation (Note 5)
Dynamic Burn-In, Method 1015, Condition D, 240 Hours, +125°C (Note 3)	

NOTES:

1. The notes of Method 5004, Table I shall apply; unless otherwise specified.
2. These steps are optional, and should be listed on the purchase order if required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table O of Method 1015.
4. For Group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
 - Assembly Attributes (post seal)
 - Test Attributes (includes Group A)
 - Shippable Serial Number List
 - Radiation Testing Certificate of Conformance
 - Wafer Lot Acceptance Report (includes SEM report)
 - X-Ray Report and Film
 - Test Variables Data

HS-81C55RH, HS-81C56RH

Metallization Topology

DIE DIMENSIONS:

76 x 63 x 14 ± 1mils

METALLIZATION:

Type: AlSi

Thickness: 11kÅ ± 2kÅ

GLASSIVATION:

Type: SiO₂

Thickness: 8kÅ ± 1kÅ

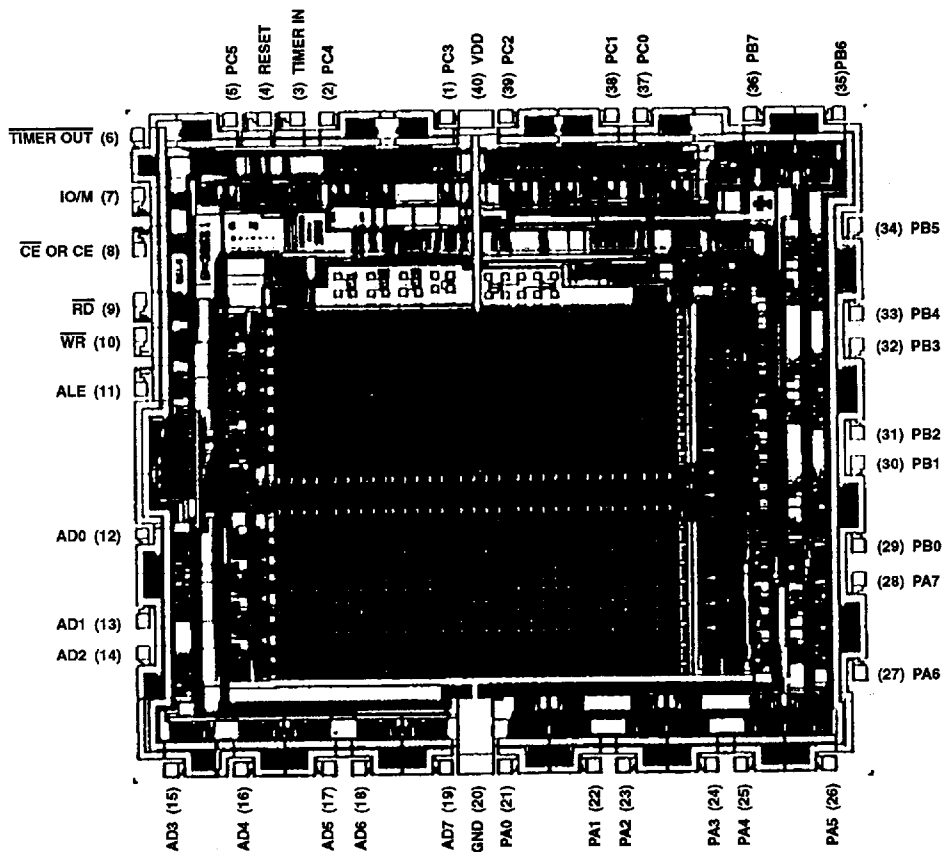
DIE ATTACH:

Material: Gold Silicon Eutectic Alloy

Temperature: Ceramic DIP- 460°C (Max)

Metallization Mask Layout

HS-81C55RH, HS-81C56RH



11
μPROCESSOR
PERIPHERALS

HS-81C55RH, HS-81C56RH

Functional Description

The HS-81C55RH and 81C56RH contains the following:

- 2K Bit Static RAM Organized as 256 x 8
- Two 8-Bit I/O Ports (PA and PB) and One 6-Bit I/O Port (PC)
- 14-Bit Timer-Counter

The IO/M (IO/Memory Select) pin selects either the five register (Command, Status, PA0 - PA7, PB0 - PB7, PC0 - PC5) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input CE or CE and IO/M are all latched on-chip at the falling edge of ALE.

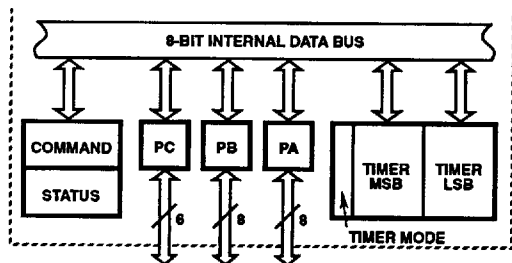


FIGURE 1. INTERNAL REGISTERS

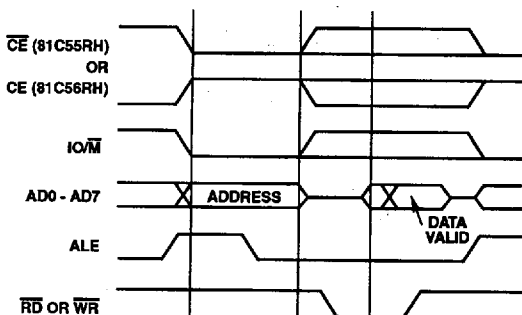


FIGURE 2. ON-BOARD MEMORY READ/WRITE CYCLE

Programming of the Command Register

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bit (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at anytime by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/M = 1. The meaning of each bit of the command byte is defined in Figure 3. The contents of the command register may never be read.

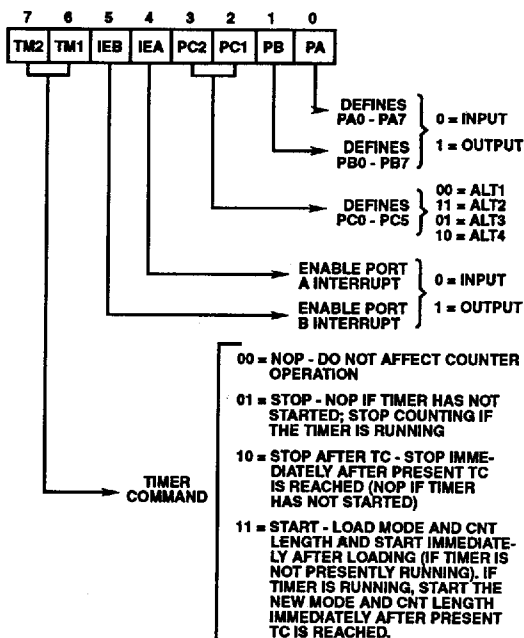


FIGURE 3. COMMAND REGISTER BIT ASSIGNMENT

Reading the Status Register

The status register consists of seven latches, one for each bit six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 4. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

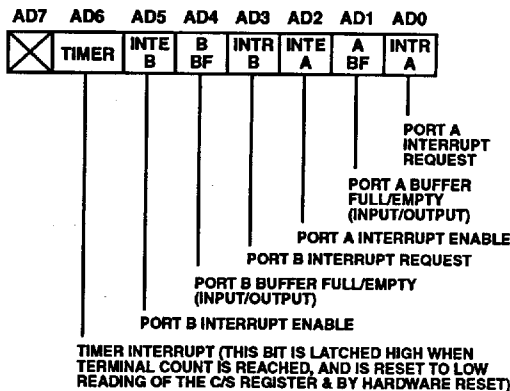


FIGURE 4. STATUS REGISTER BIT ASSIGNMENT

HS-81C55RH, HS-81C56RH

Input/Output Section

The I/O section of the HS-81C55RH and HS-81C56RH consists of five registers: (See Figure 5)

- **Command/Status Register (C/S)** - Both register are assigned the address XXXXX000. The C/S address serves the dual purpose.

When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are not accessible through the pins.

When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD0 - AD7 lines.

- **PA Register** - This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). the I/O pins assigned in relation to this register are PA0 - PA7. The address of this register is XXXXX001.
- **PB Register** - This register functions the same as PA Register. the I/O pins assigned are PB0 - PB7. The address of this register is XXXXX010
- **PC Register** - This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD2 and AD3 bits of the C/S register.

When PC0 - PC5 is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an Interrupt that the HS-81C55RH and HS-81C56RH sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 1).

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and Pb are initialized as follows: :

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS†								SELECTION
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Interval Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	General Purpose I/O or Control Port C
X	X	X	X	X	1	0	0	Low-Order 8 Bits of Timer Count
X	X	X	X	X	1	0	1	High 6 Bits of Timer Count and 2 Bits of Timer Mode

† I/O Address must be qualified by $\overline{CE} = 1$ (81C56RH) or $\overline{CE} = 0$ (81C55RH) and $\overline{IO/M} = 1$ in order to select the appropriate register. X = Don't Care

FIGURE 5. I/O PORT AND TIMER ADDRESSING SCHEME

Figure 6 shows how I/O Ports A and B are structured within the HS-81C55RH and HS-81C56RH.

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

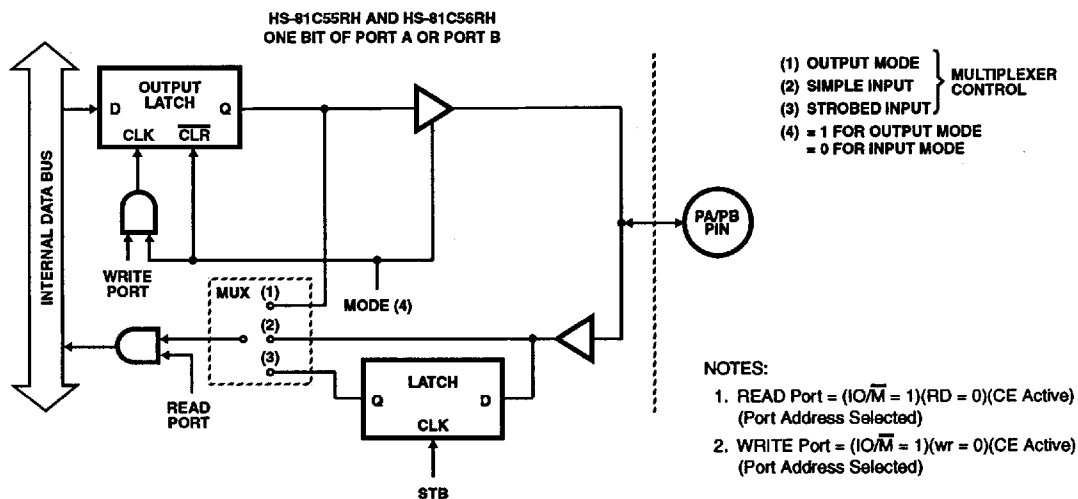


FIGURE 6. HS-81C55RH AND HS-81C56RH PORT FUNCTION

HS-81C55RH, HS-81C56RH

The outputs of the HS-81C55/56RH are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. the output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the HS-81C55/56RH is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT1 or ALT2 modes, the bits of Port C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 7 shows how the HS-81C55/56RH I/O ports might be configured in a typical system.

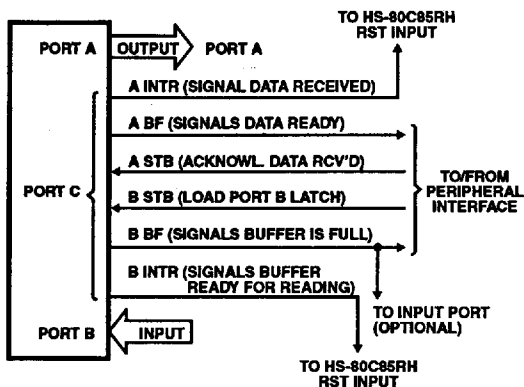


FIGURE 7. EXAMPLE: COMMAND REGISTER = 00111001

Timer Section

The timer is a 14 bit down counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 5).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 8). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0-13.

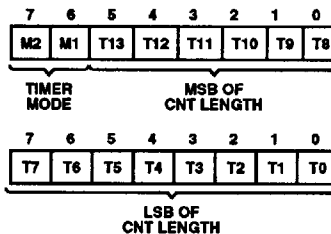


FIGURE 8. TIMER FORMAT

TABLE 1. PORT CONTROL ASSIGNMENT

PIN	ALT1	ALT2	ALT3	ALT4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A STB (Port A Strobe)	A STB (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B STB (Port B Strobe)

HS-81C55RH, HS-81C56RH

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 9.

TIMER OUT WAVEFORMS:

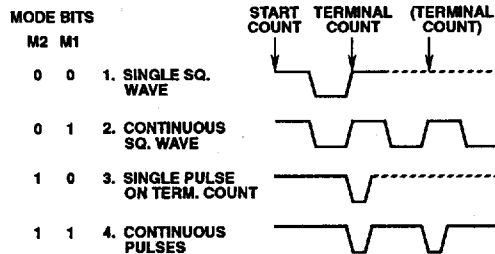


FIGURE 9. TIMER MODES

Bits 6-7 (TM2 and TM1) of command register contents are used to start and stop the counter. there are four commands to choose from:

TM2	TM1	
0	0	NOP - Do not affect counter operation
0	1	STOP-NOP - If timer has not started; stop counting if the timer is running
1	0	STOP AFTER TC - Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START - Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you *must* issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 10.

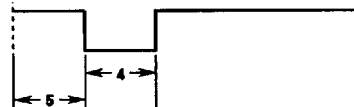


FIGURE 10. ASYMMETRICAL SQUARE-WAVE OUTPUT RESULTING FROM COUNT OF 9

The counter in the HS-81C55/56RH is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the HS-81C55/56RH chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the HS-80C85RH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16 bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count - 1 if full count is odd).

NOTE: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the HS-81C55/56RH always counts out the right number of pulses in generating the TIMER OUT waveforms.