Programming Specification for Atmel's AT17 and AT17A Series FPGA Configuration EEPROMs

The FPGA Configurator

The FPGA Configurator is a serial EEPROM memory which can also be used to load programmable devices. This document describes the features needed to program the Configurator from within its programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low).

Reference schematics are supplied for in-system programming applications.

Serial Bus Overview

The serial bus is a two-wire bus; one wire (CLOCK) functions as a clock and is provided by the programmer, the second wire (DATA) is a bi-directional signal and is used to provide data and control information.

Information is transmitted on the serial bus in messages. Each MESSAGE is preceded by a Start Condition and is ended with a Stop Condition. The message consists of an integer number of bytes, each byte consisting of 8 bits of data, followed by a ninth Acknowledge Bit. This Acknowledge Bit is provided by the recipient of the transmitted byte. This is possible because devices may only drive the DATA line Low. The system must provide a small pull-up current (1 kΩ equivalent) for the DATA line.

The MESSAGE FORMAT for read and write instructions consists of the bytes shown below.

While writing, the programmer is responsible for issuing the instruction and data. While reading, the programmer issues the instruction and acknowledges the data from the Configurator as necessary.

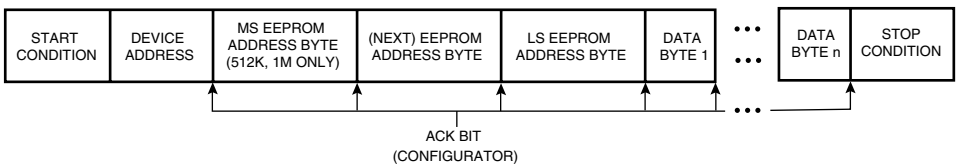
Again, the Acknowledge Bit is asserted on the DATA line by the receiving device on a byte-by-byte basis.

The factory blanks devices to all zeros before shipping. The array cannot otherwise be "initialized" except by explicitly writing a known value to each location using the serial protocol described herein.

Bit Format

Data on the DATA pin may change only during the CLOCK Low time; whereas Start and Stop Conditions are identified as transitions during the CLOCK High time.

Write Instruction Message Format

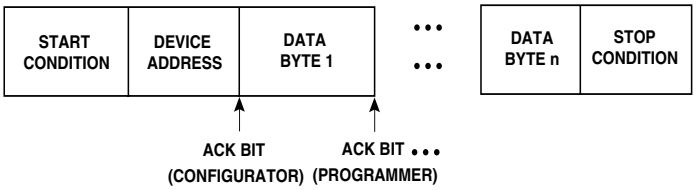


FPGA Configuration EEPROM Programming Specification

Application Note

Rev. 0437H–03/01

Current Address Read (Extended to Sequential Read) Instruction Message Format



Start and Stop Conditions

The Start Condition is indicated by a high-to-low transition of the DATA line when the CLOCK line is High. Similarly, the Stop Condition is generated by a low-to-high transition of the DATA line when the CLOCK line is High, as shown in Figure 1.

The Start Condition will return the device to the state where it is waiting for a Device Address (its normal quiescent mode).

The Stop Condition initiates an internally timed write signal whose maximum duration is t_{WR} (refer to AC Characteristics table for actual value). During this time, the Configurator must remain in programming mode (i.e., $\overline{SER\_EN}$ is driven Low). DATA and CLOCK lines are ignored until the cycle is completed. Since the write cycle typically completes in less than t_{WR} seconds, we recommend the use of "polling" as described in later sections. Input levels to all other pins should be held constant until the write cycle has been completed.

Acknowledge Bit

The Acknowledge (ACK) Bit shown in Figure 1 is provided by the Configurator receiving the byte. The receiving Configurator can accept the byte by asserting a Low value on the DATA line, or it can refuse the byte by asserting (allowing the signal to be externally pulled up to) a High value on the DATA line. All bytes from accepted messages must be terminated by either an Acknowledge Bit or a Stop Condition. Following an ACK Bit, when the DATA line is released during an exchange of control between the Configurator and the Programmer, the DATA line may be pulled High temporarily as shown above; due to the open-collector output nature of the line. Control of the line must resume before the next rising edge of the clock.

Bit Ordering Protocol

The most significant bit is the first bit of a byte transmitted on the DATA line for the Device Address Byte and the EEPROM Address Bytes. It is followed by the lesser significant bits until the eighth bit, the least significant bit, is transmitted. However, for Data Bytes (both writing and reading), the first bit transmitted is the least significant bit. This protocol is shown in the diagrams below.

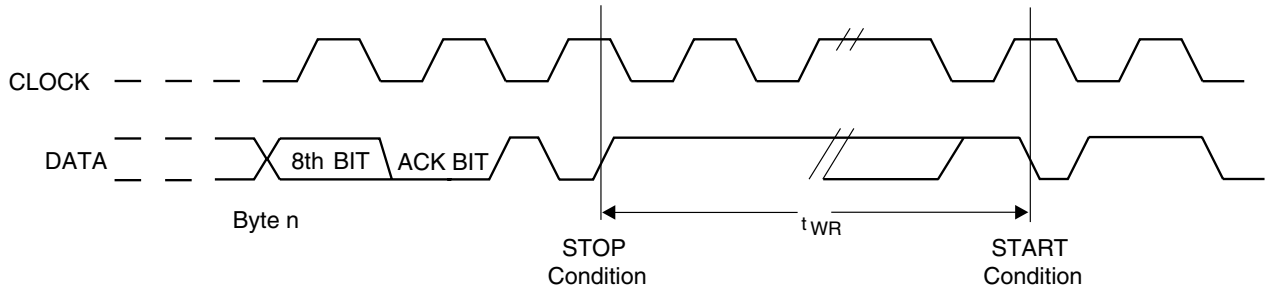
Device Address Byte

The contents of the Device Address Byte are shown below, along with the order in which the bits are clocked into the device. The A2 bit is provided to allow multiple Configurators to share a common bus. When programming a Configurator, the A2 pin on the Configurator must be forced to a logic "0" or "1" level. It is recommended that this pin be connected to 0V (GND) using a 4.7 kΩ pull-down (thereby matching the default setting of Atmel's programming utility). Thus, the A2 bit may be used as an Address Bit among two Configurators, or as a chip-enable mechanism for in-system programming employing more than two Configurators.

The $\overline{CE}$ pin cannot be used for device selection in programming mode (i.e., when $\overline{SER\_EN}$ is drive Low).

Note: For the 512K, 1M, 2M, and the 65K/128K/256K Configurators that have B label on the date code; only the A2 input pin will be pulled to ground via weak internal pull-downs if left floating. The 2M(002) in this document is referring to AT17C/LV002(A) EEPROM. The 2M(020) in this document is referring to AT17C/LV020(A) EEPROM. Atmel recommends using AT17C/LV002 instead of AT17C/LV020 for all new designs.

Figure 1. Start and Stop Conditions



Device Address Byte

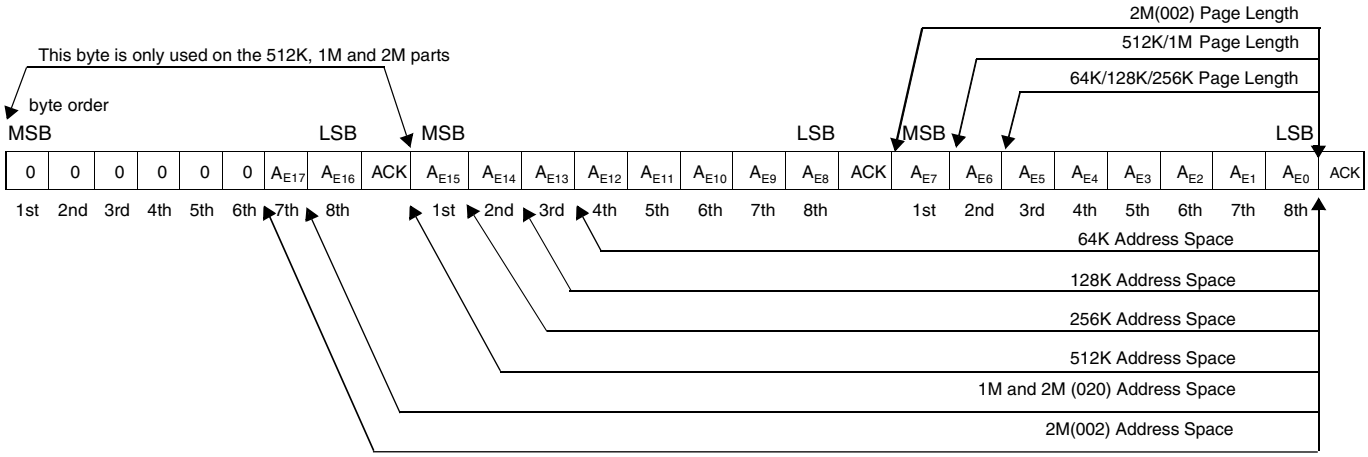
MSB							LSB
1	0	1	0	A_2	1	1	R/$\overline{W}$
1st	2nd	3rd	4th	5th	6th	7th	8th

Where: R/$\overline{W}$ = 1 Read
= 0 Write
A2 = 1 if A2 pin of target Configurator is at V_{CC}
= 0 if A2 pin of target Configurator is at GROUND

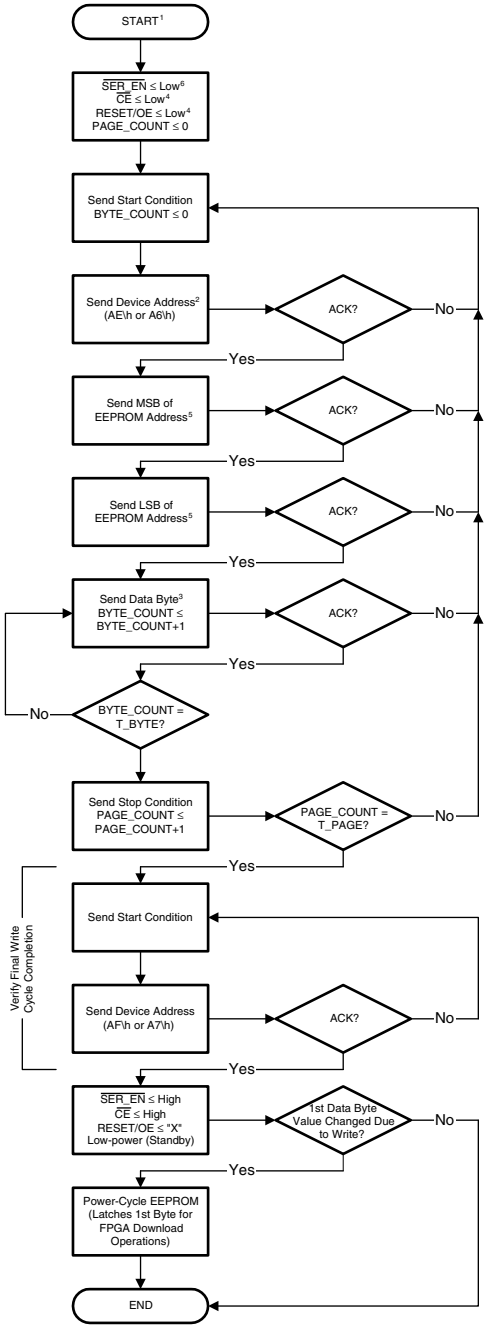
EEPROM Address

The EEPROM Address consists of two bytes on the 64K, 128K and 256K parts, and three bytes on the 512K, 1M and 2M parts. Each Address Byte is followed by an Acknowledge Bit (provided by the Configurator). These bytes define the normal address space of the Configurator, as described below. The order in which each byte is clocked into the Configurator is also indicated. Unused bits in an Address Byte must be set to “0”. Exceptions to this are:

1. when setting the reset polarity;
2. when reading Device and Manufacturer Codes; and
3. when enabling/disabling the internal oscillator in the AT17A Series Configurator (512K, 1M and 2M parts only).



Programming Summary: Write to Whole Device



Notes:
1. Pull-up resistor required on DATA line
2. Pull-up (AE\h) or pull-down (A6\h) required on A2 pin of EEPROM ($\overline{CEO}$)
3. Data byte received/sent LSB to MSB
4. These signals have “don’t care” conditions for the AT17C/LV512/010/020/002(A).
5. The 512K, 1M and 2M parts require three EEPROM address bytes; all three bytes must be individually ACK’d by the EEPROM.
6. WP pins on 512K, 1M and 2M(002) devices are internally pulled to GND; by default disabling the write protect feature of the devices.

EEPROM Address is Defined as:

65(A)			$000x_6$	$x_5x_4x_3x_2$	x_1x_000	0000
128(A)			$00x_7x_6$	$x_5x_4x_3x_2$	x_1x_000	0000
256(A)			$0x_8x_7x_6$	$x_5x_4x_3x_2$	x_1x_000	0000
512(A)	0000	0000	$x_8x_7x_6x_5$	$x_4x_3x_2x_1$	x_0000	0000
010(A)	0000	$000x_9$	$x_8x_7x_6x_5$	$x_4x_3x_2x_1$	x_0000	0000
020(A	0000	$000x_9$	$x_8x_7x_6x_5$	$x_4x_3x_2x_1$	x_0000	0000
002(A)	0000	$000x_9X_8$	$x_7x_6x_5x_4$	$x_3x_2x_1x_0$	0000	0000

Note: where X_n ... X_0 is (PAGE_COUNT)\b
where X_n ... X_0 is (PAGE_COUNT)\b

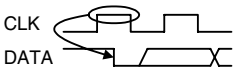
T_BYTE

AT17C/LV65/128/256(A)	64
AT17C/LV512/010/020(A)	128
AT17C/LV002(A)	256

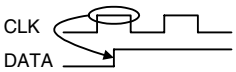
T_PAGE

AT17C/LV65(A)	128
AT17C/LV128(A)	256
AT17C/LV256(A)	512
AT17C/LV512(A)	512
AT17C/LV010/020(A)	1024
AT17C/LV002(A)	1024

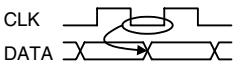
START CONDITION



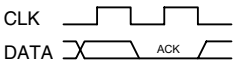
STOP CONDITION



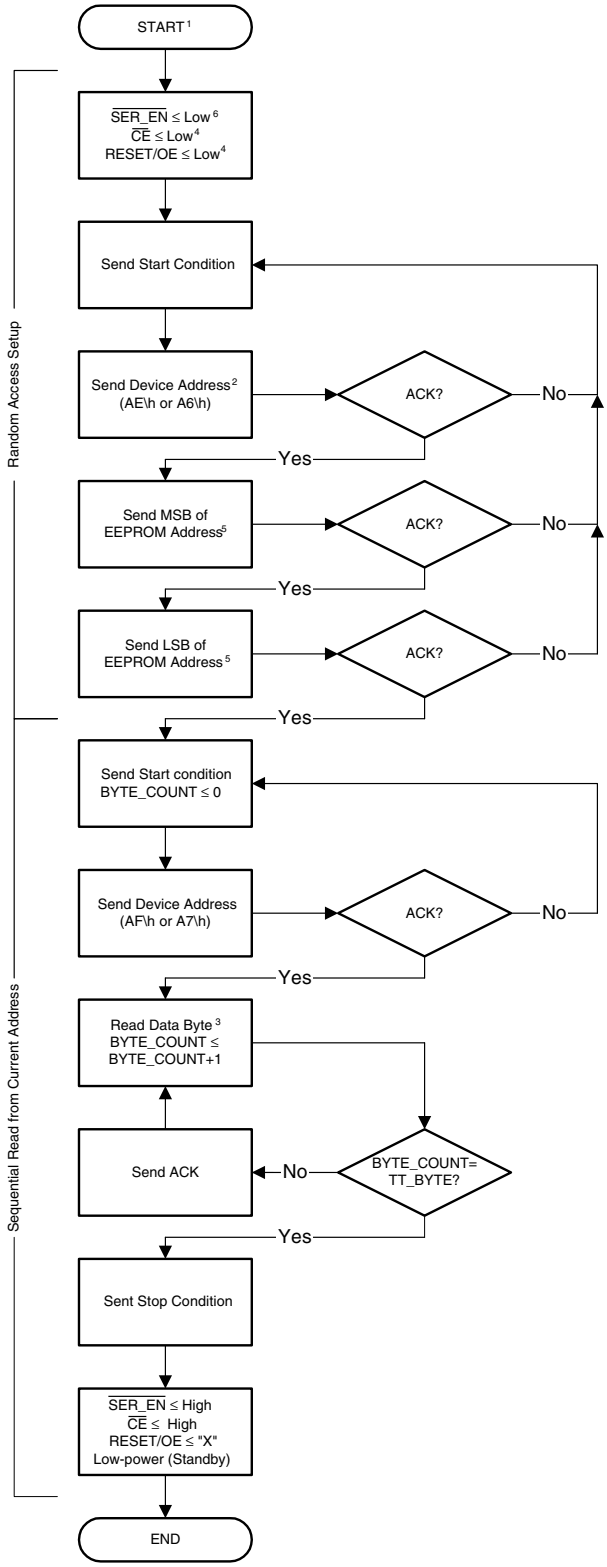
DATA BIT



ACK BIT



Programming Summary: Read from Whole Device



Notes:
1. Pull-up resistor required on DATA line
2. Pull-up (AE\h) or pull-down (A6\h) required on A2 pin of EEPROM ($\overline{CEO}$)
3. Data byte received/sent LSB to MSB
4. These signals have “don’t care” conditions for the AT17C/LV512/010/020/002(A).
5. The 512K, 1M and 2M parts require three EEPROM address bytes; all three bytes must be individually ACK’d by the EEPROM.
6. WP pins on 512K, 1M and 2M(002) devices are internally pulled to GND; by default disabling the write protect feature of the devices.

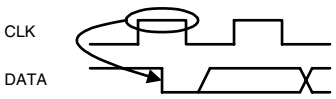
EEPROM Address is Defined as:

65/128/256	00 00 \h
512/010/002	00 00 00 \h

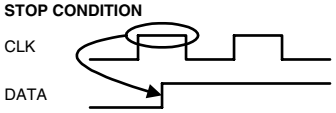
TT_BYTE

AT17C/LV65(A)	8192 \d
AT17C/LV128(A)	16384 \d
AT17C/LV256(A)	32768 \d
AT17C/LV512(A)	65536 \d
AT17C/LV010/020(A)	131072 \d
AT17C/LV002(A)	262144 \d

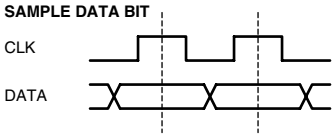
START CONDITION



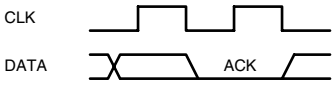
STOP CONDITION



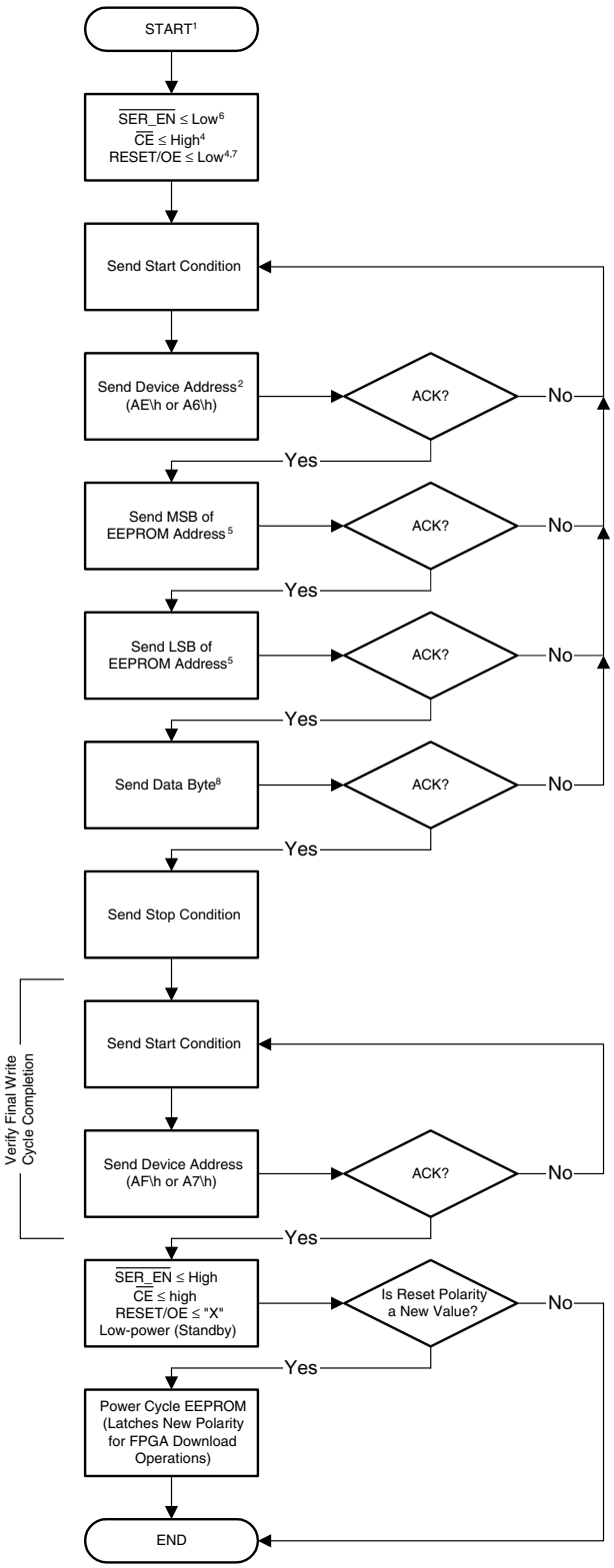
SAMPLE DATA BIT



ACK BIT



Programming Summary: Write Reset Polarity



Notes:
1. Pull-up resistor required on DATA line
2. Pull-up (AE\h) or pull-down (A6\h) required on A2 pin of EEPROM ($\overline{CEO}$)
3. Data byte received/sent LSB to MSB
4. These signals have “don’t care” conditions for the AT17C/LV512/010/020/002(A).
5. The 512K, 1M and 2M parts require three EEPROM address bytes; all three bytes must be individually ACK’d by the EEPROM.
6. WP pins on 512K, 1M, and 2M(002) devices are internally pulled to GND; by default disabling the write protect feature of the devices.
7. Drive RESET/OE high for active low RESET, active high OE. Drive RESET/OE low for active high RESET, active low OE.
8. The 512K, 1M and 2M parts require four data bytes of the same value to program the reset polarity; all four bytes must be individually ACK’d by the EEPROM.

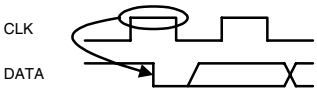
EEPROM Address is Defined as:

AT17C/LV65/128/256(A)	3F FF \h
AT17C/LV512/010(A)	02 00 00 \h
AT17C/LV002(A)	400 000 \h

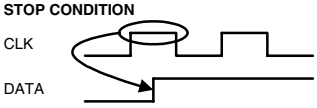
Data Byte is Defined as:

65/128/256	FF \h
512/010/002 (active low RESET)	FF \h
512/010/002 (active high RESET)	00 \h

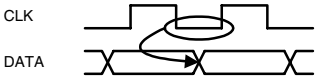
START CONDITION



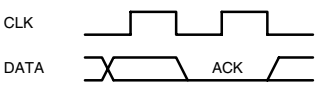
STOP CONDITION



DATA BIT



ACK BIT



Data Byte

The organization of the Data Byte is shown below. Note that in this case, the Data Byte is clocked into the device LSB first and MSB last.

Writing

Writing to the normal address space takes place in pages. A page is 64 bytes long in 64K, 128K, and 256K parts; 128 bytes long in 512K, 1M and 2M(020) parts, and 256 bytes long in the 2M(002) part. The page boundaries are, respectively, addresses where A_{E6} down to A_{EOS} are all zero, and A_{E6} down to A_{E0} are all zero. Writing can start at any address within a page and the number of bytes written must be 64 for the 64K, 128K and 256K parts, or 128 for the 512K and 1M parts, and 256 for the 2M(002) part. The first byte is written at the transmitted address. The address is incremented in the Configurator following the receipt of each Data Byte. Only the lower bits of the address (6, 7 or 8, depending on the page length) are incremented. Thus, after writing to the last byte address within the given page, the address will roll over to the first byte address of the same page.

Data Byte

LSB							MSB
D0	D1	D2	D3	D4	D5	D6	D7
1st	2nd	3rd	4th	5th	6th	7th	8th

```
A Write Instruction consists of
    a Start Condition
    a Device Address Byte with R/W = 0
      An Acknowledge Bit from the Configurator
    MS Byte of the EEPROM Address
            (512K, 1M, and 2M parts only)
      An Acknowledge Bit from the Configurator
    (Next) Byte of the EEPROM Address
      An Acknowledge Bit from the Configurator
    LS Byte of EEPROM Address
      An Acknowledge Bit from the Configurator
    One or more Data Bytes (sent to the
    Configurator)
      Each followed by an Acknowledge Bit from the
      Configurator
    a Stop Condition
```

WRITE POLLING: On receipt of the Stop Condition, the Configurator enters an internally-timed write cycle. While the Configurator is busy with this write cycle, it will not acknowledge any transfers. The programmer can start the next page write by sending the Start Condition followed by the Device Address, in effect polling the Configurator. If this is not acknowledged, then the programmer should abandon the transfer without asserting a Stop Condition. The programmer can then repeatedly initiate a write instruction as above, until an acknowledge is received. When the Acknowledge Bit is received, the write instruction should continue by sending the first EEPROM Address Byte to the Configurator.

An alternative to write polling would be to wait a period of t_{WR} before sending the next page of data or exiting the programming mode. All signals must be maintained during the entire write cycle.

Reading

Read instructions are initiated similarly to write instructions. However, with the R/$\overline{W}$ bit in the Device Address set to one. There are three variants of the read instruction: current address read, random read and sequential read.

For all reads, it is important to understand that the internal Data Byte address counter maintains the last address accessed during the previous read or write operation, incremented by one. This address remains valid between operations as long as the chip power is maintained and the device remains in 2-wire access mode (i.e., $\overline{SER\_EN}$ is driven Low). If the last operation was a read at address n, then the current address would be n + 1. If the final operation was a write at address n, then the current address would again be n + 1 with one exception. If address n was the last byte address in the page, the incremented address n + 1 would “roll over” to the first byte address on the next page.

CURRENT ADDRESS READ: Once the Device Address (with the R/$\overline{W}$ select bit set to High) is clocked in and acknowledged by the Configurator, the Data Byte at the current address is serially clocked out by the Configurator in response to the clock from the programmer. The programmer generates a Stop Condition to accept the single byte of data and terminate the read instruction.

```
A Current Address Read instruction consists of
    a Start Condition
    a Device Address with R/W = 1
      An Acknowledge Bit from the Configurator
    a Data Byte from the Configurator
    a Stop Condition from the programmer.
```

RANDOM READ: A Random Read is a Current Address Read preceded by an aborted write instruction. The write instruction is only initiated for the purpose of loading the EEPROM Address Bytes. Once the Device Address Byte and the EEPROM Address Bytes are clocked in and acknowledged by the Configurator, the programmer immediately initiates a Current Address Read.

A Random Address Read instruction consists of

- a Start Condition
- a Device Address with R/$\overline{W}$ = 0
- An Acknowledge Bit from the Configurator
- MS Byte of the EEPROM Address (512K, 1M, and 2M parts only)
- An Acknowledge Bit from the Configurator
- (Next) Byte of the EEPROM Address
- An Acknowledge Bit from the Configurator
- LS Byte of EEPROM Address
- An Acknowledge bit from the Configurator
- a Start Condition
- a Device Address with R/$\overline{W}$ = 1
- An Acknowledge Bit from the Configurator
- a Data Byte from the Configurator
- a Stop Condition from the programmer.

SEQUENTIAL READ: Sequential Reads follow either a Current Address Read or a Random Address Read. After the programmer receives a Data Byte, it may respond with an Acknowledge Bit. As long as the Configurator receives an Acknowledge Bit, it will continue to increment the Data Byte address and serially clock out sequential Data Bytes until the memory address limit is reached. The Sequential Read instruction is terminated when the programmer does not respond with an Acknowledge Bit but instead generates a Stop Condition following the receipt of a Data Byte.

Programmer Functions

The following programmer functions are supported while the Configurator is in programming mode (i.e., when $\overline{SER\_EN}$ is driven Low):

1. Read the Manufacturer's Code and the Device Code (optional for in-system programming).
2. Program the device.
3. Verify the device.
4. Set the Reset Polarity option.
5. Enable/disable the internal oscillator (AT17C/LV512A/010A/020A/002A devices only).

In the order given above, they are performed in the following manner. (The same protocol and operations are used for both 5V and 3.3V devices, as well as for the Altera pinout variants except where stated.)

Reading Manufacturer's and Device Codes

The 512/010/020/002 Configurators use a different algorithm than the 65/128/256 Configurators for reading the Manufacturer's and Device codes.

On 512/010/020 Configurators, the sequential reading of these bytes are accomplished by performing a Random Read at EEPROM Address 040000H.

On 002 Configurators, the sequential reading of these bytes are accomplished by performing a Random Read at EEPROM Address 100000H.

On 65/128/256 Configurators, the sequential read is done at EEPROM Address 0 by performing a Current Address Read with the following additional DC voltages set:

RESET/$\overline{OE}$ = 0V

$\overline{CE}$ = 11.5 ± 0.5V

The correct codes are

Manufacturers Code -Byte 0			1E
Device Code	- Byte 1	FF	AT17C/LV128(A)
		7F	AT17C/LV65(A)
		77	AT17C/LV256(A)
		37	AT17C/LV512(A)
		F7	AT17C/LV010(A)
		73	AT17C/LV020(A)
		78	AT17C/LV002(A)

Note: The Manufacturer's Code and Device Code are read using the byte ordering specified for Data Bytes; i.e., LSB first, MSB last. These procedures are not supported by the supplied ISP reference design schematics for 65/128/256 Configurators.

Programming the Device

All the bytes in a given page must be written. The page access order is not important but it is suggested that the Configurator be written sequentially from address 0. Writing is accomplished by using the DATA and CLOCK pins.

For the 65/128/256 Configurators only, two additional programming pins must be set as follows:

RESET/$\overline{OE}$ = 0V (Write protection disable)

$\overline{CE}$ = 0V

Important Note on AT17 and AT17A Series Configurators Programming

The first byte of data will not be cached for read back during FPGA Configuration (i.e., when $\overline{SER\_EN}$ is driven High) until the Configurator is power-cycled. This may be critical in cascaded ISP applications where the first byte of the second or subsequent EEPROM is likely to change between updated bitstreams.

Write Protect Operation

The AT17 and AT17A Series Configurators have a “Write Protect” feature that allows portions of the memory to be blocked during Write instructions. When the blocking is in effect, data will not be written in the blocked portion and the existing data in the blocked portion will be preserved.

For the 65/128/256 Configurators, the RESET/$\overline{OE}$ pin is used as a WRITE PROTECT pin while in programming mode (i.e., $\overline{SER\_EN}$ is Low with $\overline{CE}$ Low). When the RESET/$\overline{OE}$ pin is High under these conditions, memory is protected as follows:

65: The lower 1/2 of memory is protected (address 0000 - 0FFF)

128: The lower 1/4 of memory is protected (address 0000 - 0FFF)

256: The lower 1/4 of memory is protected (address 0000 - 1FFF)

For the 512/010/002 Configurators, there are up to two dedicated Write Protect pins; WP1 (pin 5) and WP2 (pin 7). They are decoded to provide protection as described below. (WP1/WP2 have weak internal pull-downs by default.)

The AT17A Series 512/010A/002A parts do not support WP2.

Note: AT17C/LV020(A) does not have Write Protect pins.

AT17 Series Write Protection (512/010)

WP2	WP1	Protection
0	0	No protection
0	1	Addresses 00000 - 07FFF (1/4 of 010, 1/2 of 512)
1	0	Addresses 00000 - 0FFFF (1/2 of 010, All of 512)
1	1	Addresses 00000 - 17FFF (3/4 of 010, All of 512)

AT17A Series Write Protection (512A/010A)

WP1	Protection
0	No protection
1	Addresses 00000 - 07FFF (1/4 of 010A, 1/2 of 512A)

AT17 Series Write Protection (002)

WP2	WP1	Protection
0	0	No protection/Normal mode
0	1	Addresses 0X000000 - 0X00FFFF (1/4 of 002)
1	0	Addresses 0X000000 - 0X01FFFF (1/2 of 002)
1	1	Addresses 0X000000 - 0X027FFF (3/4 of 002)

Verifying the Device

All bytes in the Configurator should be read and compared to their intended values. Reading is done using the CLOCK and DATA pins.

For the 65/128/256 Configurators, two additional programming pins must be set as follows:

RESET/$\overline{OE}$ = 0V (Write protection disable)

$\overline{CE}$ = 0V

RESET Polarity Option

All Configurators in the AT17 and AT17A Series have the ability to change the polarity of the RESET/$\overline{OE}$ pin. This is required to allow the devices to properly configure various FPGA families. The default condition is active Low OE and active High RESET.

The 65/128/256 Configurators use a different algorithm from the 512/010/020/002 Configurators; the algorithms are described below.

65/128/256 Configurator RESET/$\overline{OE}$ Polarity Programming

Setting the polarity option ACTIVE HIGH OE (ACTIVE LOW RESET): Write Data Byte “FF” to address 3FFFH, with two additional programming pins set to the following:

RESET/$\overline{OE}$ = V_{CC} +/- 0.25V

$\overline{CE}$ = V_{CC} +/- 0.25V

Setting the polarity option ACTIVE LOW OE (ACTIVE HIGH RESET): Write a byte “FF” to address 3FFFH, with two additional programming pins set to the following:

RESET/$\overline{OE}$ = 0V

$\overline{CE}$ = V_{CC} +/- 0.25V

Verifying the RESET Polarity: Power up the device with:

RESET/$\overline{OE}$ = 0V

$\overline{CE}$ = 0V

A2 ($\overline{CEO}$) = Input to programmer (High Z)

$\overline{SER\_EN}$ = V_{CC} +/- 0.25V

CLOCK = 0V

DATA = Input to programmer

In this condition, if the DATA pin is tri-stated, then the RESET/$\overline{OE}$ fuse is programmed for active High OE (active Low RESET); if the DATA pin reads a “0” or a “1”, the RESET/$\overline{OE}$ fuse is active Low OE (active High RESET).

512/010/020 Configurator RESET/$\overline{OE}$ Polarity Programming

Setting the polarity option ACTIVE HIGH OE (ACTIVE LOW RESET): Write four bytes “FF FF FF FF” to addresses 20000H - 20003H.

Setting the polarity option ACTIVE LOW OE (ACTIVE HIGH RESET): Write four bytes “00 00 00 00” to addresses 20000H - 20003H.

Verifying the RESET/$\overline{OE}$ Polarity 512/010/020 Configurators: Perform a Random Read of four Data Bytes from addresses 20000H - 20003H. If the data is “00 00 00 00” then the fuse is programmed for ACTIVE LOW OE (ACTIVE HIGH RESET); if the data is “FF FF FF FF” then the fuse is programmed for ACTIVE HIGH OE (ACTIVE LOW RESET).

002 Configurator RESET/$\overline{OE}$ Polarity Programming

Setting the polarity option ACTIVE HIGH OE (ACTIVE LOW RESET): Write four bytes “FF FF FF FF” to addresses 400000H - 400003H.

Setting the polarity option ACTIVE LOW OE (ACTIVE HIGH RESET): Write four bytes “00 00 00 00” to addresses 400000H - 400003H.

Verifying the RESET/$\overline{OE}$ Polarity 002 Configurators: Perform a Random Read of four Data Bytes from addresses 400000H - 400003H. If the data is “00 00 00 00” then the fuse is programmed for ACTIVE LOW OE (ACTIVE HIGH RESET); if the data is “FF FF FF FF” then the

Important Notes on AT17 and AT17A Series Configurators RESET Polarity Programming

1. The pin conditions above must be maintained during the entire write cycle; t_{WR} or until the next Device Address is acknowledged (if using Write polling).
2. After the RESET polarity has been modified, the Configurator must be powered down and back up again before attempting to verify functionality or use the newly programmed RESET function.

DCLK Pin Option

The 512A/010A/020A/002A devices have the ability to disable their DCLK output. These devices can be used in master mode where the clock pin is an output, or in slave mode where the clock pin is an input.

The mode is normally determined by the state of the nCS pin on power-up and reset. However, there are instances where it may be desirable to program the device into slave mode regardless of the power-up sequence.

The default status of the DCLK pin is with the internal oscillator enabled.

To disable the internal oscillator and program the device into slave mode for the 512A/010A/020A:

> Write a byte “00” of data to Address 0011100x xxxxxxxx xxxxxxxx with nCS held to ground.

To disable the internal oscillator and program the device into slave mode for the 002A:

> Write a byte “00” of data to Address 1110 00xx xxxx xxxx xxxx xxxx with nCS held to ground.

To enable the internal oscillator of 512A/010A/020A, which allows the device to act as either master or slave depending on the state of nCS during power-up and reset:

> Write a byte “FF” of data to Address 0011100x xxxxxxxx xxxxxxxx with nCS held to ground.

To enable the internal oscillator of 002A, which allows the device to act as either master or slave, depending on the state of nCS during power-up and reset:

> Write a byte “FF” of data to Address 1110 00xx xxxx xxxx xxxx xxxx with nCS held to ground.

In-System Programming Applications

The AT17 and AT17A Series Configurators are in-system (re)programmable (ISP). The examples shown on the following pages support the following programmer functions:

1. Read the Manufacturer's Code and the Device Code (512K, 1M and 2M parts only).
2. Program the device.
3. Verify the device data.
4. Set the Reset Polarity option.

While Atmel's FPGA Configurators can be programmed from various sources (e.g., on-board microcontrollers or PLDs), the applications shown here are designed to facilitate users of our ATDH2200E Configurator Programming Kit. The typical system setup is shown in Figure 2.

In selecting a device and generating a circuit for any SRAM-based FPGAs, the key issues to address are:

- Number of FPGA program bits versus Configurator data space
- Pinout compatibility and package availability
- Configurator master or slave operation (512A/010A/020A/002A only)
- Existence of weak internal pull-up or pull-down resistors on the inputs of the FPGA or Configurator
- Avoiding contention on the clock line during ISP
- Avoiding contention on the RESET/$\overline{OE}$ and $\overline{CE}$ (nCS) lines during ISP (65/128/256 only)
- Use of the A2 pin for addressing (up to two Configurators in cascade) or as a chip select (up to n Configurators in cascade) during ISP
- Use of the Ready pin, an external Reset signal, and/or an RC constant to delay configuration
- 3-wire (512/010/020/002 only) or 5-wire (65/128/256) ISP interface

Please note that the pages within the configuration EEPROM can be selectively rewritten. It follows that the reset polarity need only be written once. The reset polarity value is latched only during the power-on reset cycle.

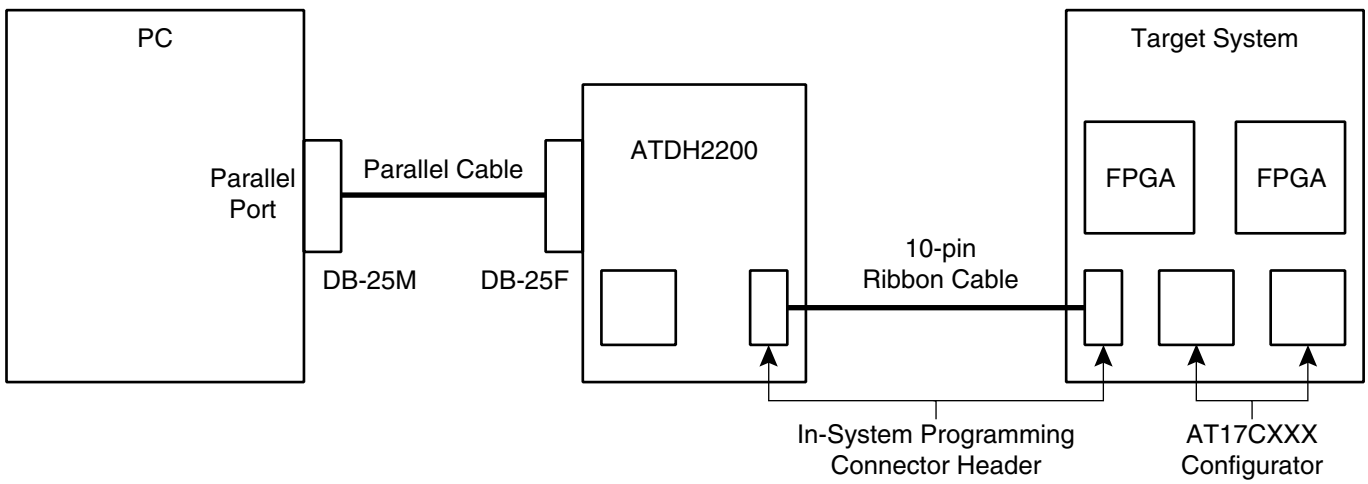
The AT17 Series Configurators can interface with many SRAM-based FPGA families. This document is limited to example implementations for the following applications:

1. Atmel AT6K and AT40K
2. Xilinx XC4000
3. Altera EPF6K, EPF8K, and EPF10K
4. Guidelines for cascading AT17C/LV020(A) Configurators

Atmel AT40K and AT6K Applications

All AT6K FPGAs and many of the AT40K FPGAs can be configured with our low-density AT17 Series Configurators (64K, 128K, 256K bit storage). The high-density AT17 Series Configurators (512K, 1M and 2M bit storage), however, introduce a simplified 3-wire interface that is highly desirable for ISP applications.

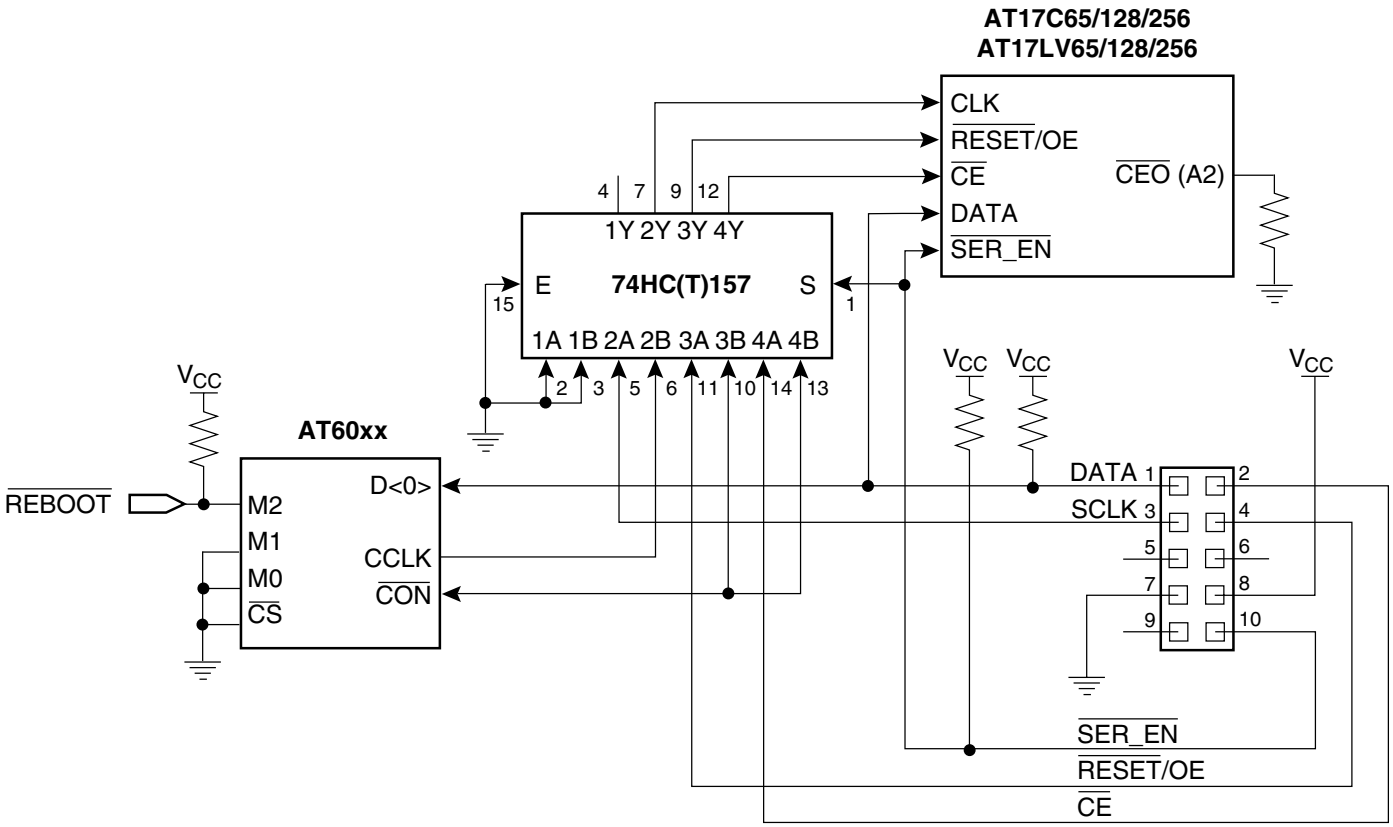
Figure 2. Typical System Setup



Figures 3 and 4 employ the low-density AT17 Configurators for a single AT6K and AT40K FPGA, respectively. The multiplexer IC "74HC(T)157" connects the Configurator signals to either the FPGA or the ISP header. The pull-down resistor on the A2 input pin of the Configurator provides the required addressing for the incoming bitstream messages during programming. $\overline{\text{SER\_EN}}$ serves as a control signal for the multiplexer select input and determines the operational mode of the EEPROM. For the low-density AT17 Configurators, control of the $\overline{\text{CE}}$ and RESET/$\overline{\text{OE}}$ pins is necessary for the programming of user data and setting of the reset polarity.

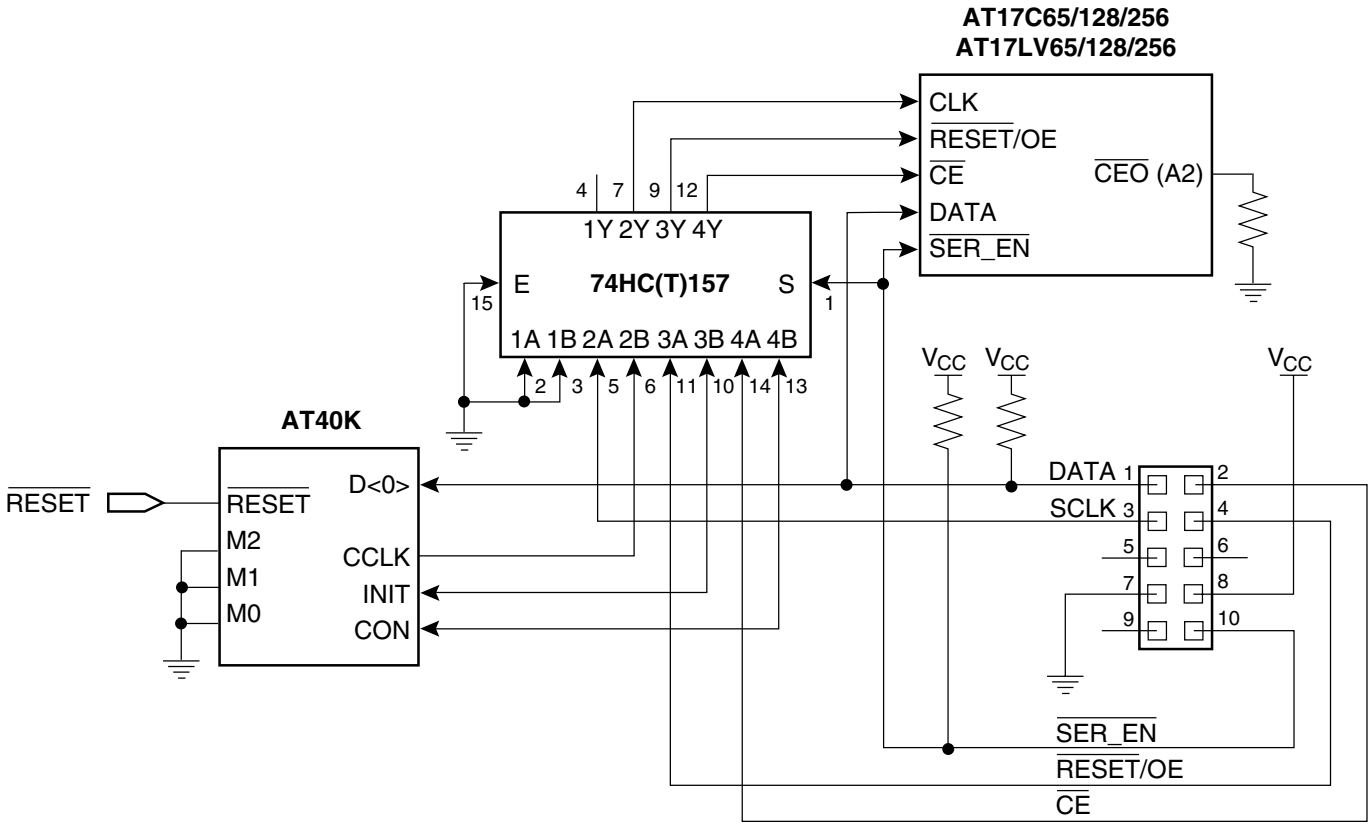
The pull-up resistor required on the line to CON is present on the input (internally) to the AT6K FPGA family.

Figure 3. ISP of the AT17C65/128/256 in an AT60xx FPGA Application



Notes: 1. 4.7 kΩ resistors used unless otherwise specified.
2. Reset polarity must be set active High.

Figure 4. ISP of the AT17C65/128/256 in an AT40K FPGA Application



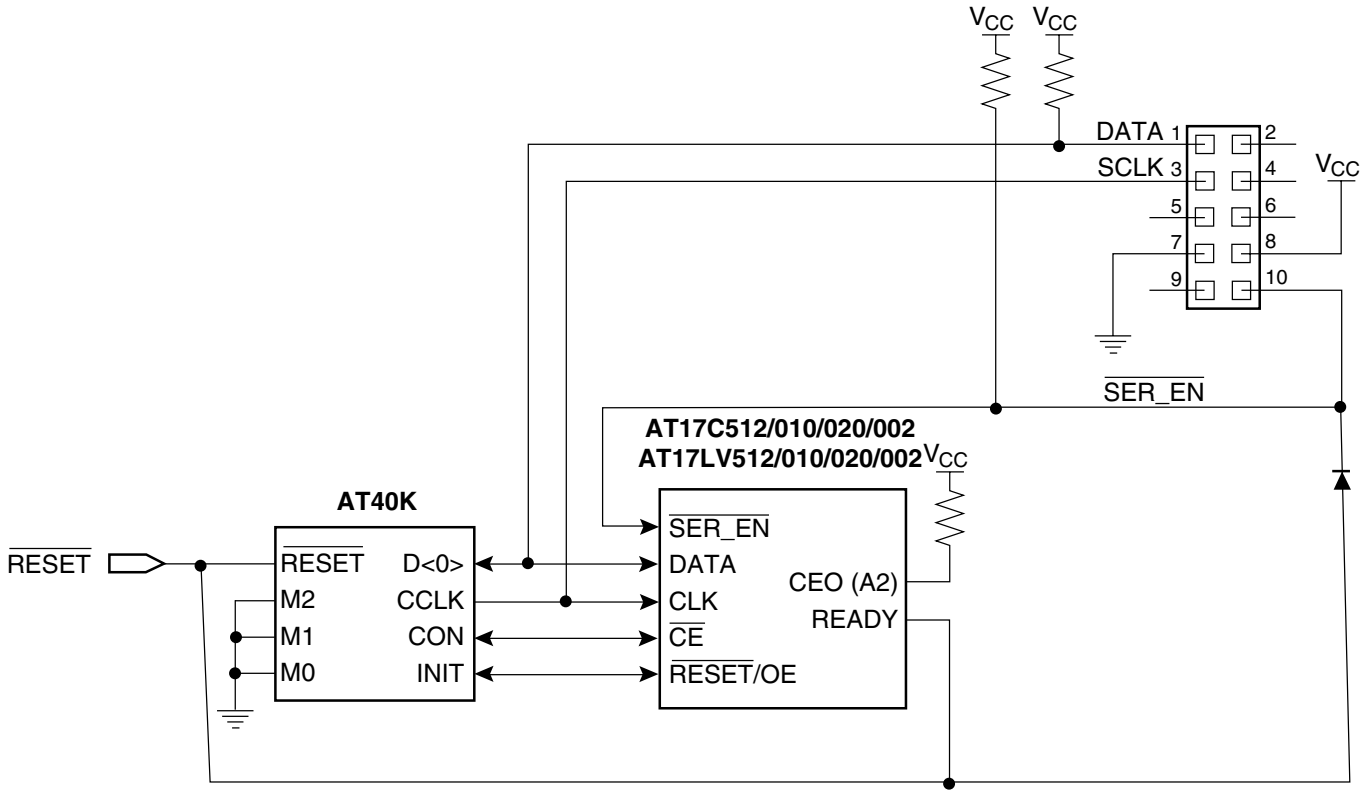
Notes: 1. 4.7 kΩ resistors used unless otherwise specified.
2. Reset polarity must be set active Low.

The complexity of the ISP circuit is significantly reduced with the high-density AT17 Configurators, as shown in Figure 5. The diode connection between the AT40K's $\overline{\text{RESET}}$ pin and the $\overline{\text{SER\_EN}}$ signal allows the external programmer to force the FPGA into a reset state during ISP. This eliminates the potential for contention on the SCLK line. The READY pin (optional feature) of the Configurator can also be connected to the AT40K's $\overline{\text{RESET}}$ pin to force the FPGA to wait in a reset state as the Configurator completes its power-on reset cycle.

The pull-up resistors required on the lines to $\overline{\text{RESET}}$, CON and INIT are present on the inputs (internally) to the AT40K FPGA family.

The dedicated WP1 and WP2 pins for the 512/010/002 parts, if left unconnected, have weak internal pull-down resistors that conveniently disable the Write Protection feature of these Configurators. Similarly, an external pull-down resistor is not required on the A2 input during ISP of 512/010/002 Configurators, since there is a weak internal pull-down resistor present on those pins.

Figure 5. ISP of the AT17C512/010/020/002 in an AT40K FPGA Application



Notes:
1. 4.7 kΩ resistors used unless otherwise specified.
2. Use of the READY pin function is optional.
3. Reset polarity must be set active Low.
4. The pull-up resistor on the A2 input of the Configurator is optional for 512/010/002 devices.

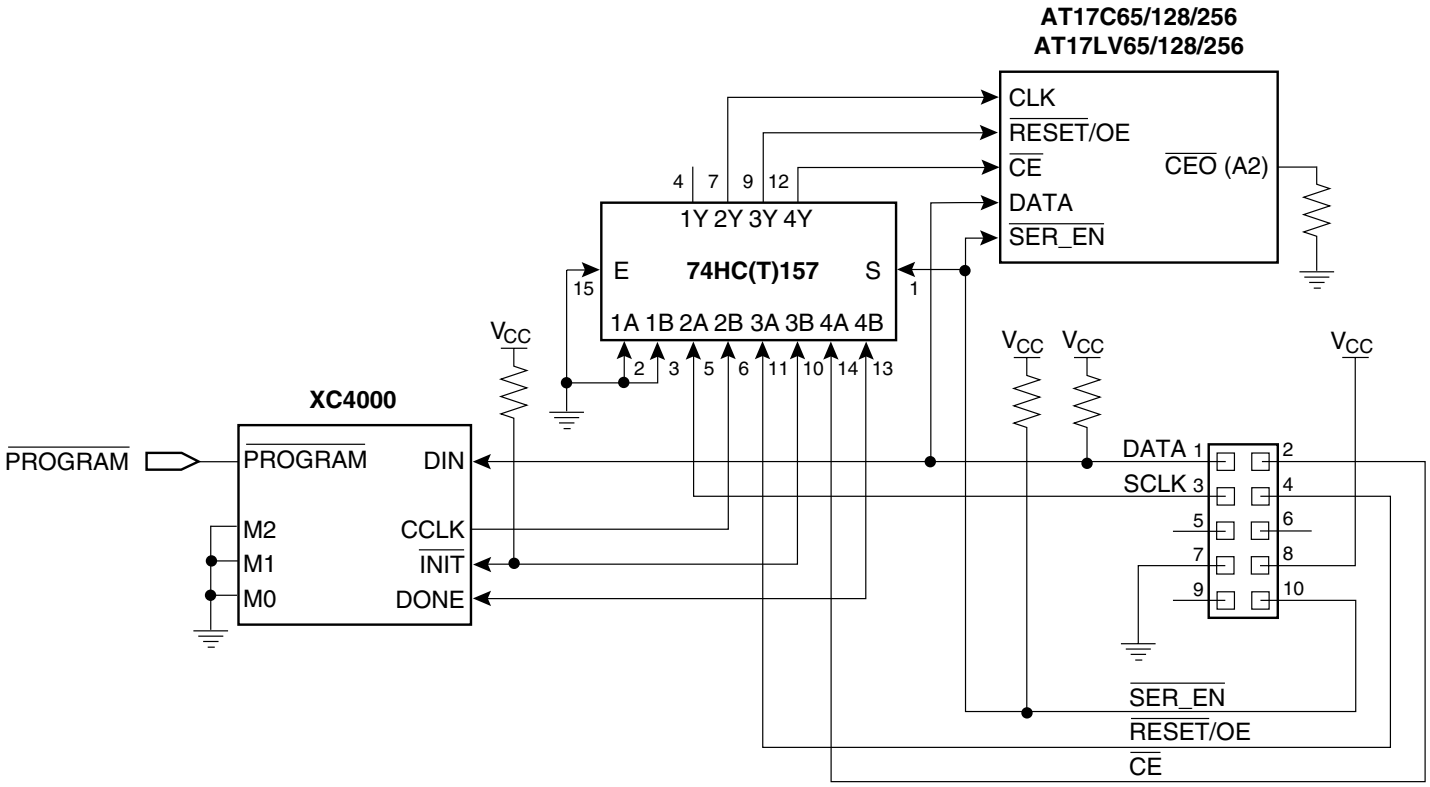
Xilinx Applications

Xilinx FPGAs (e.g., XC4000, Spartan®, Virtex®) can be configured with AT17 Series Configurators. The high-density AT17 Series Configurators (512K, 1M and 2M bit storage), however, introduce a simplified 3-wire interface that is highly desirable for ISP applications. For high-density or daisy-chained FPGAs, the AT17 Configurators can be cascaded to provide the necessary memory.

Figure 6 employs the low-density AT17 Configurator for a single XC4000 FPGA. The multiplexer IC "74HC(T)157" connects the Configurator signals to either the FPGA or the ISP header. The pull-down resistor on the A2 input pin of the Configurator provides the required addressing for the incoming bitstream messages during programming. $\overline{\text{SER\_EN}}$ serves as a control signal for the multiplexer select input and determines the operational mode of the EEPROM. For the low-density AT17 Configurators, control of the $\overline{\text{CE}}$ and RESET/$\overline{\text{OE}}$ pins is necessary for the programming of user data and setting of the reset polarity.

The pull-up resistor required on the lines to $\overline{\text{PROGRAM}}$ and DONE are present on the inputs (internally) to the XC4000 FPGA family.

Figure 6. ISP of the AT17C65/128/256 in an XC4000 FPGA Application

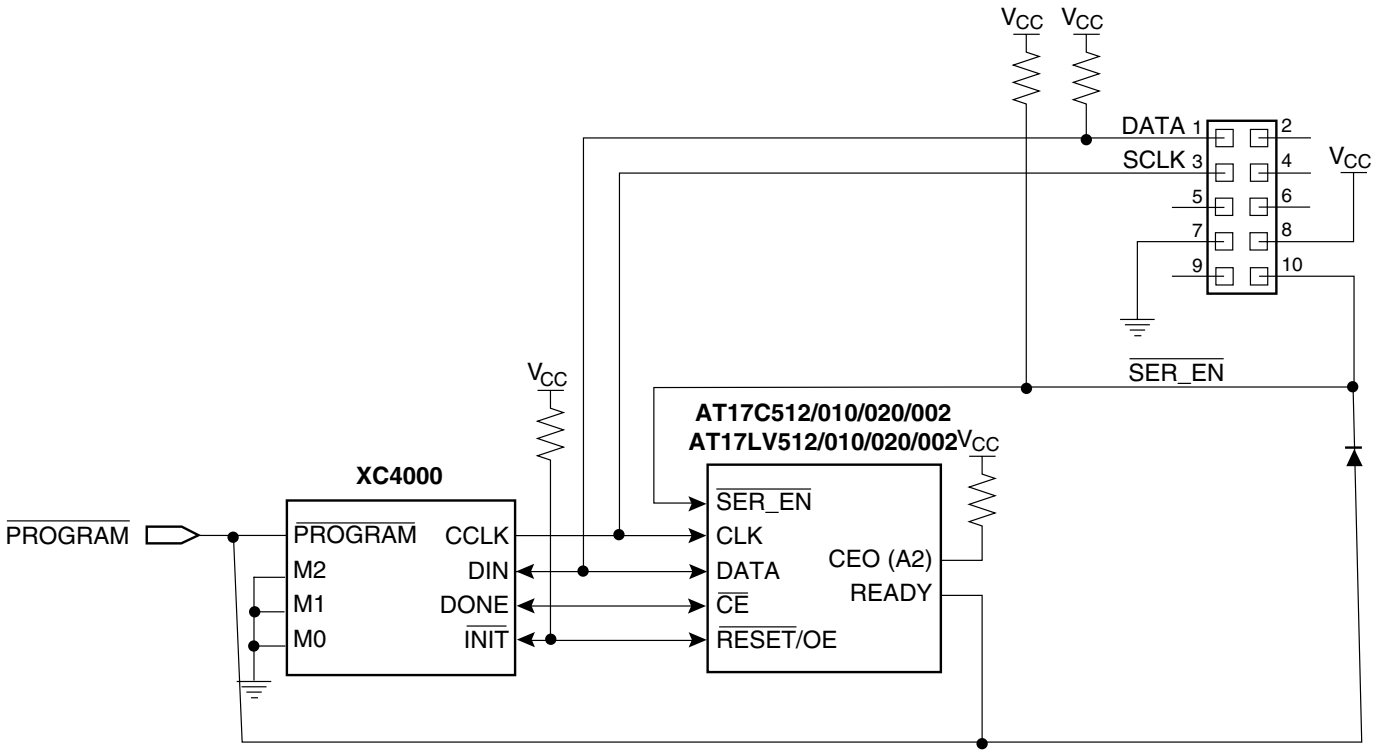


Notes: 1. 4.7 kΩ resistors used unless otherwise specified.
2. An optional internal pull-up resistor is enabled here for DONE.
3. Reset polarity must be set active Low.

The complexity of the ISP circuit is significantly reduced with the high-density AT17 Configurators, as shown in Figure 7. The diode connection between the XC4000's $\overline{\text{PROGRAM}}$ pin and the $\overline{\text{SER\_EN}}$ signal allows the external programmer to force the FPGA into a reset state during ISP. This eliminates the potential for contention on the SCLK line. The READY pin (optional feature) of the Configurator can also be connected to the XC4000's $\overline{\text{PROGRAM}}$ pin to force the FPGA to wait in a reset state as the Configurator completes its power-on reset cycle.

The pull-up resistors required on the lines to $\overline{\text{PROGRAM}}$ and DONE are present on the inputs (internally) to the XC4000 FPGA family. The internal pull-up resistor on the DONE input is available as an option to the user (via Xilinx bitstreaming tools).

Figure 7. ISP of the AT17C512/010/020/002 in an XC4000 FPGA Application



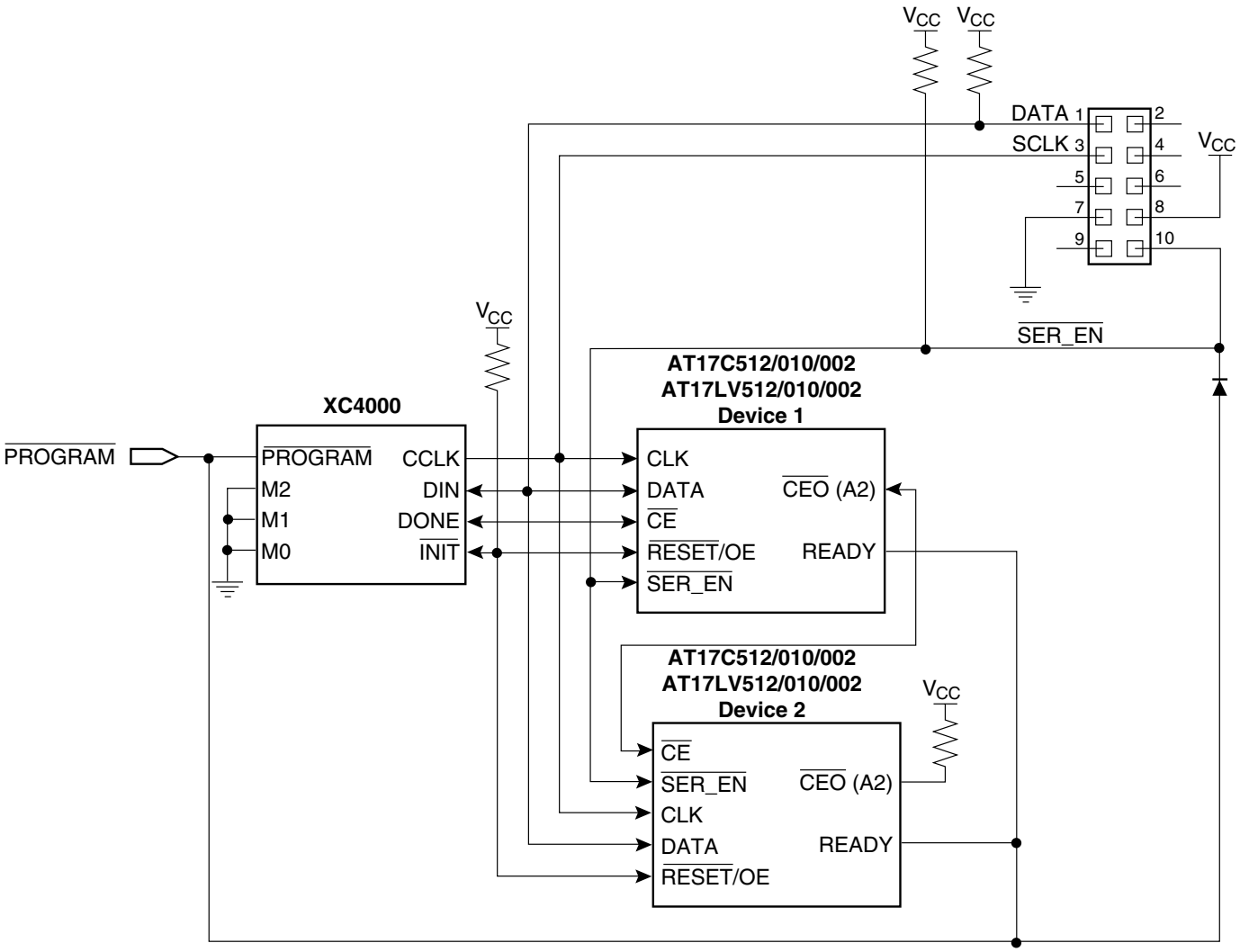
Notes:
1. 4.7 kΩ resistors used unless otherwise specified.
2. An optional internal pull-up resistor is enabled here for DONE.
3. Use of the READY pin function is optional.
4. Reset polarity must be set active Low.
5. The pull-up resistor on the A2 input of the Configurator is optional for 512/010/002 devices.

The dedicated WP1 and WP2 pins for the 512/010/002 parts, if left unconnected, have weak internal pull-down resistors that conveniently disable the Write Protection feature of these Configurators. Similarly, an external pull-down resistor is not required on the A2 input for 512/010/002 Configurators during ISP since there is a weak internal pull-down resistor present on those pins.

In simple cascaded Configurator applications involving two EEPROMs (Figure 8), the A2 input can be used as an addressing pin (set to logic level “0” for one EEPROM and logic level “1” for the other EEPROM). The programming utility can then modify the A2 bit sent in the bitstream messages to target one of the two EEPROMs.

Applications involving more than two EEPROMs must use the A2 input pin as a chip select. Pull-up resistors on each A2 input are required, in addition to an external decoder circuit, which must be able to selectively drive each A2 input Low. For further details please refer to the “Programming Cascaded Configurators” application note.

Figure 8. ISP of Two Cascaded AT17C512/010/002s in an XC4000 FPGA Application



Notes:
1. 4.7 kΩ resistors used unless otherwise specified.
2. An optional internal pull-up resistor is enabled here for DONE.
3. Use of the READY pin function is optional.
4. Reset polarity must be set active Low.
5. This schematic cannot be used with a 020 Configurator.

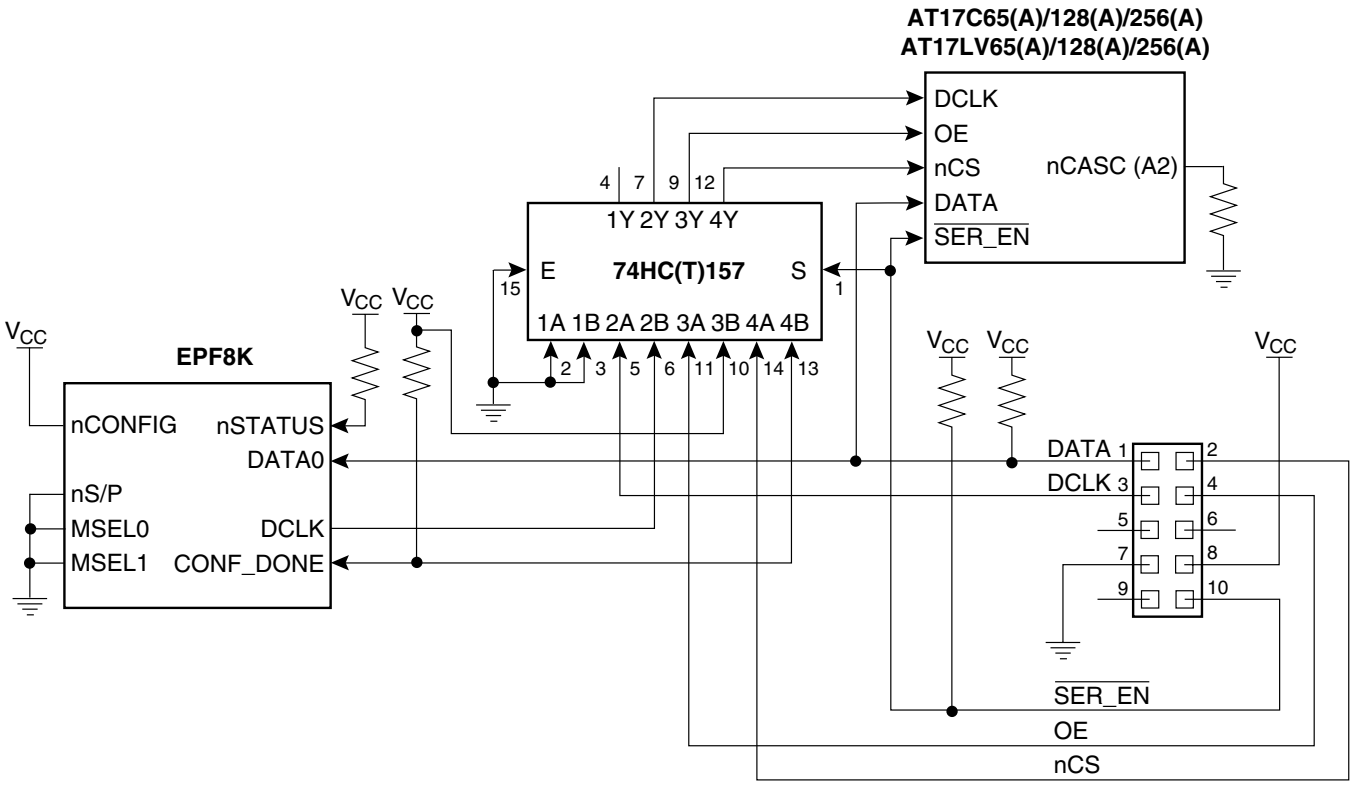
Altera Applications

Altera FLEX® devices (e.g., EPF10K, EPF6K, EPF8K) can be configured with AT17A Series Configurators. The high-density AT17A Series Configurators (512K, 1M and 2M bit storage), however, introduce a simplified 3-wire interface that is highly desirable for ISP applications. For high-density or daisy-chained FPGAs, the AT17A Configurators can be cascaded to provide the necessary memory.

Figures 9 and 10 employ the low-density AT17(A) Configurator for a single EPF8K and EPF6K device, respectively. The multiplexer IC (74HC(T)157) connects the Configurator signals to either the FPGA or the ISP header. The pull-down resistor on the A2 input pin of the Configurator provides the required addressing for the incoming bit-stream messages during programming. $\overline{\text{SER\_EN}}$ serves as a control signal for the multiplexer select input and determines the operational mode of the EEPROM. For the low-density AT17(A) Configurators, control of the nCS and OE pins is necessary for the programming of user data and setting of the reset polarity.

While the nCONFIG input pin can be connected directly to V_{CC}, we recommend the use of an RC delay or connection to an active Low system reset signal for Altera EPF10K/6K applications to ensure that the V_{CC} has entered into normal operating levels prior to initiating configuration.

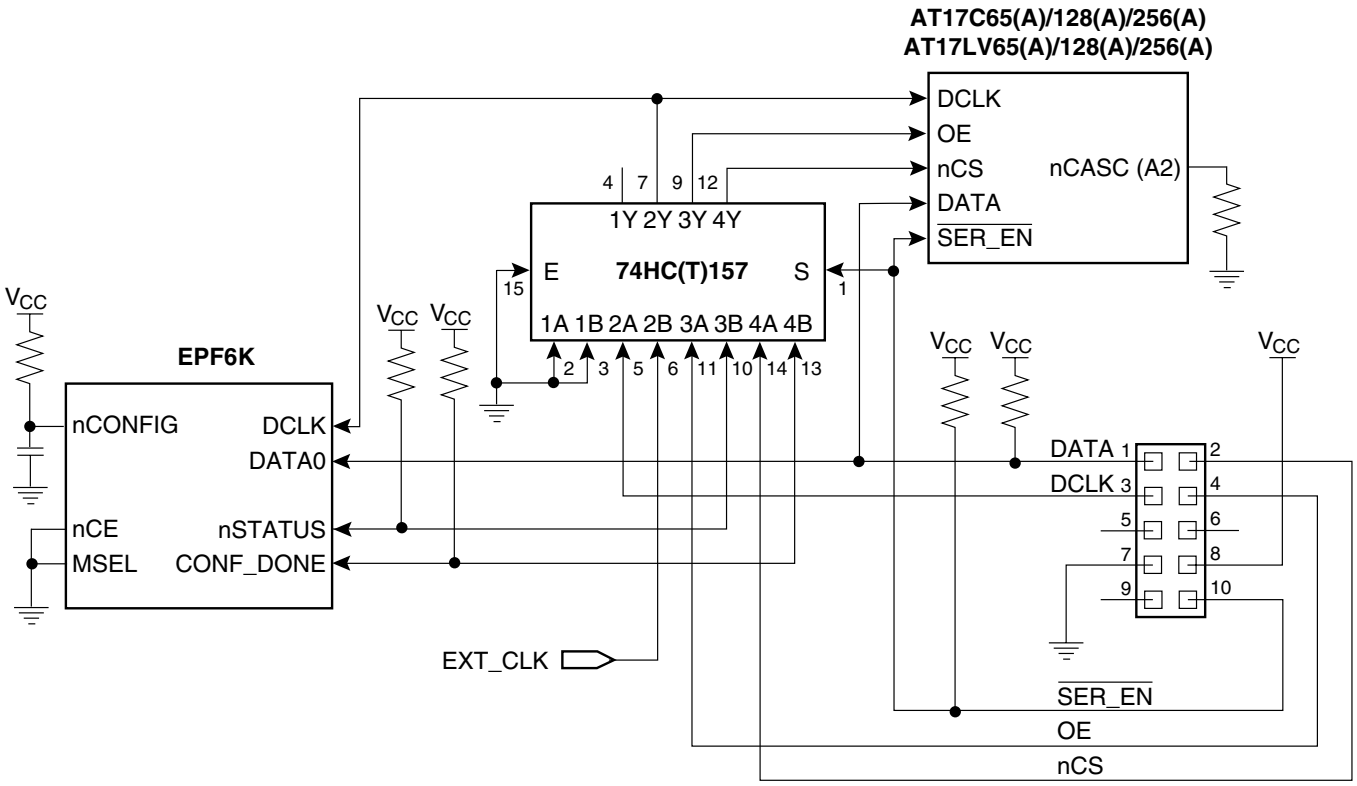
Figure 9. ISP of the AT17C65(A)/128(A)/256(A) in an Altera EPF8K Application



Notes: 1. 1.0 kΩ resistors used unless otherwise specified.

2. Reset polarity must be set active Low.

Figure 10. ISP of the AT17C65(A)/128(A)/256(A) in an Altera EPF6K Application



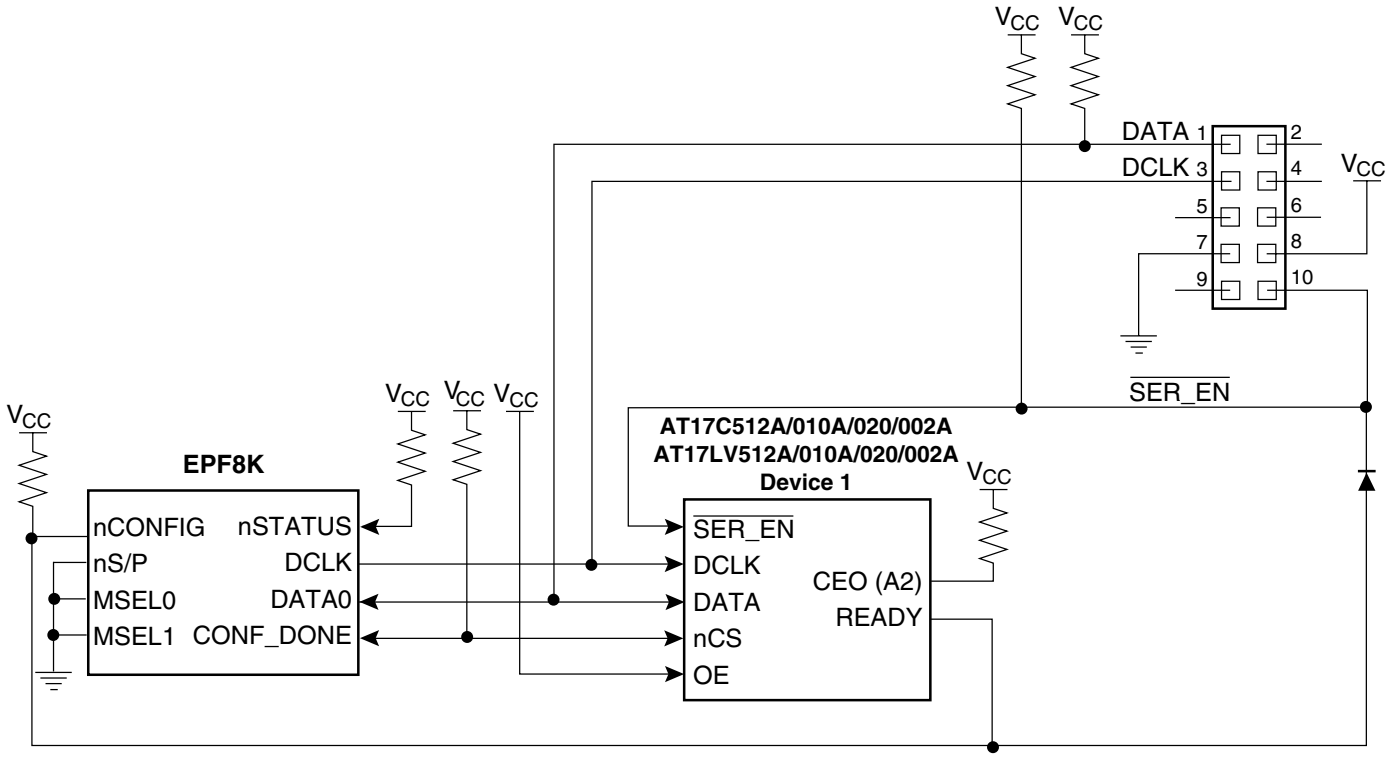
Notes:
1. 1.0 kΩ resistors used unless otherwise specified.
2. Applicable to EPF10K.
3. Reset polarity must be set active Low.
4. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable (nCONFIG can instead be connected to an active Low system reset signal).

Since the low-density AT17(A) Series Configurators cannot provide the necessary clock signal (i.e., act as system master) during configuration, a clock must be supplied externally or from the FPGA.

The complexity of the ISP circuit is significantly reduced with the high-density AT17A Configurators, as shown in Figures 11 and 12. The diode connection between the EPF8K's nCONFIG pin and the $\overline{\text{SER\_EN}}$ signal allows the external programmer to force the FPGA into a reset state during ISP. This eliminates the potential for contention on the SCLK line. The READY pin (optional feature) of the Configurator can also be connected to the FPGA's nCONFIG pin to force the FPGA to remain in a reset state as the Configurator completes its power-on reset cycle.

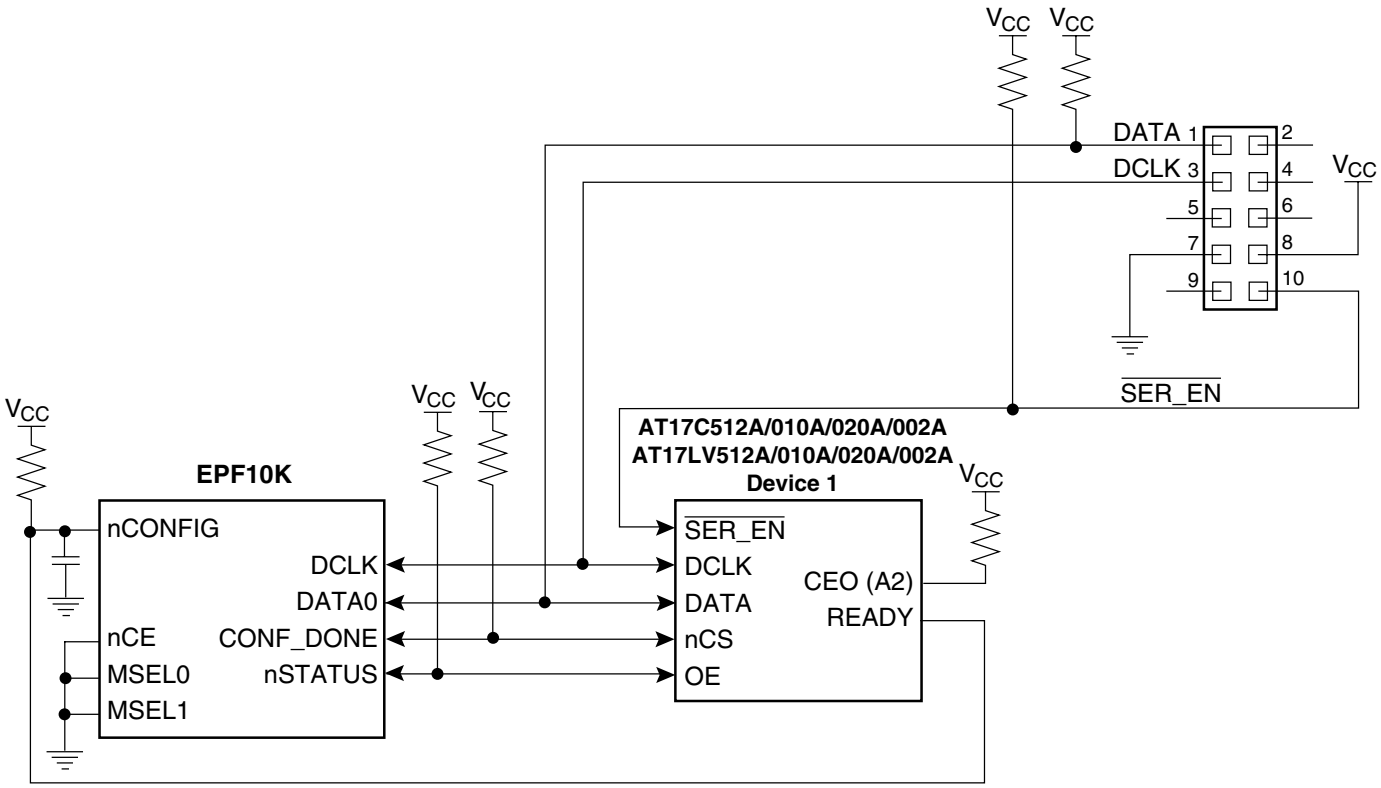
For the Altera EPF8K application in Figure 11, the internal oscillator of the high-density AT17A Configurator must be disabled. This need only be performed once before device insertion or during ISP by connecting nCS to the ISP header (not shown).

Figure 11. ISP of the AT17C512A/010A/020A/002A in an Altera EPF8K Application



Notes:
1. 1.0 kΩ resistors used unless otherwise specified.
2. The internal oscillator of the AT17A Configurator is disabled.
3. Reset polarity must be set active Low.
4. Use of the READY pin function is optional.
5. The pull-up resistor on the A2 input pin of 512A/010A/002A Configurators is optional.

Figure 12. ISP of the AT17C512A/010A/020A/002A in an Altera EPF10K or EPF6K Application



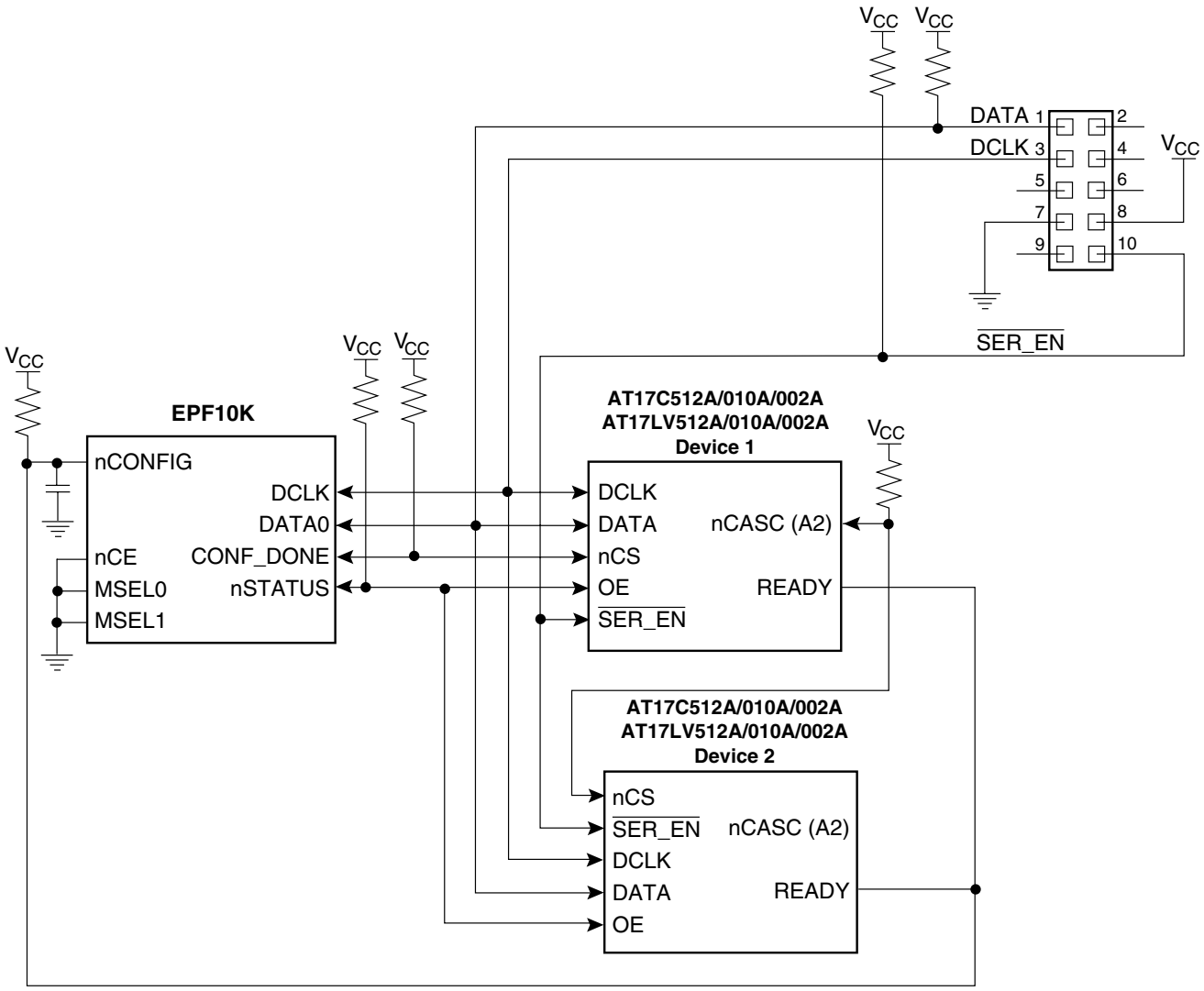
Notes:
1. 4. 7kΩ resistors used unless otherwise specified.
2. Applicable to EPF6K.
3. Reset polarity must be set active Low.
4. Use of the READY pin function is optional.
5. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable (nCONFIG can instead be connected to an active Low system reset signal).
6. The pull-up resistor on the A2 input pin of 512A/010A/002A Configurators is optional.

The dedicated WP1 pin for the 512A/010A/002A parts, if left unconnected, has a weak internal pull-down resistor that conveniently disables the Write Protection feature of these Configurators. Similarly, an external pull-down resistor is not required on the A2 input for 512A/010A/002A Configurators during ISP since there is a weak internal pull-down resistor present on that pin.

In simple cascaded Configurator applications involving two EEPROMs (Figure 13), the A2 input can be used as an addressing pin (set to logic level “0” for one EEPROM and logic level “1” for the other EEPROM). The programming utility can then modify the A2 bit sent in the bitstream messages to target one of the two EEPROMs.

Applications involving more than two EEPROMs must use the A2 input pin as a chip select. Pull-up resistors on each A2 input is required in addition to an external decoder circuit, which must be able to selectively drive each A2 input Low. For further details, please refer to the “Programming Cascaded Configurators” application note.

Figure 13. ISP of Two Cascaded AT17C/LV512A/010A/002As in an Altera FLEX10K Application



Notes:
1. 4.7 kΩ resistors used unless otherwise specified.
2. Use of the READY pin function is optional.
3. Reset polarity must be set active Low.
4. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable (nCONFIG can instead be connected to an active Low system reset signal).

DC Characteristics[4]

V_{CC} = 5.0V ± 5%, T_A = 15°C - 85°C[1][2][3]

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
I_{CC}	Supply Current	V_{CC} = 5V		2.0	5.0	mA
I_{LL}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	10	µA
V_{IH}	High-level Input Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage		-0.5		0.4	V
V_{OL}	Output Low-level Voltage	I_{OL} = 3 mA			0.4	V

Notes: 1. This parameter is characterized and is not 100% tested.
2. Commercial temperature range 15°C - 70°C
3. Industrial temperature range 15°C - 85°C
4. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)

AC Characteristics[4]

V_{CC} = 5.0V ± 5%, T_A = 15°C - 85°C[1][2][3]

Symbol	Parameter	Min	Max	Units
f_{CLOCK}	Clock Frequency, Clock		400	KHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.8		µs
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		µs
$t_{HD;STA}$	Start Hold Time	0.6		µs
$t_{SU;STA}$	Start Setup Time	0.6		µs
$t_{HD\ DAT}$	Data In Hold Time	0		µs
$t_{SU\ DAT}$	Data In Setup Time	0.1		µs
t_R	Inputs Rise Time		0.3	µs
t_F	Inputs Fall Time		0.3	µs
$t_{SU\ STO}$	Stop Setup Time	0.6		µs
t_{DH}	Data Out Hold Time	0.05		µs
t_{WR}	Write Cycle Time		10	ms

Notes: 1. This parameter is characterized and is not 100% tested.
2. Commercial temperature range 15°C - 70°C
3. Industrial temperature range 15°C - 85°C
4. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)

DC Characteristics[4]

V_{CC} = 3.3V ± 5%, T_A = 15°C - 85°C[1][2][3]

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Supply Current	V_{CC} = 3.6		2.0	3.0	mA
I_{LL}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	10	µA
V_{IH}	High-level Input Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage		-0.5		0.2	V
V_{OL}	Output Low-level Voltage	I_{OL} = 2.1 mA			0.4	V

Notes: 1. This parameter is characterized and is not 100% tested.
2. Commercial temperature range 15°C - 70°C
3. Industrial temperature range 15°C - 85°C
4. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)

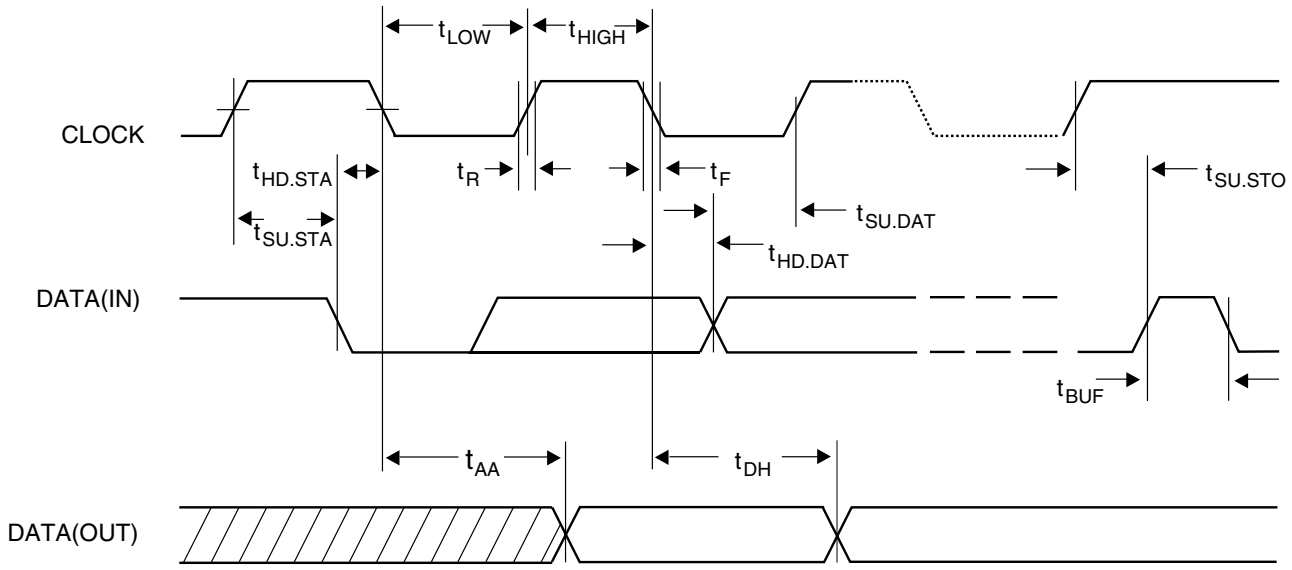
AC Characteristics[4]

V_{CC} = 3.3V ± 5%, T_A = 15°C - 85°C[1][2][3]

Symbol	Parameter	Min	Max	Units
f_{CLOCK}	Clock Frequency, Clock		100	KHz
t_{LOW}	Clock Pulse Width Low	4.0		µs
t_{HIGH}	Clock Pulse Width High	4.0		µs
t_{AA}	Clock Low to Data Out Valid	0.1	1.0	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.5		µs
$t_{HD;STA}$	Start Hold Time	2.0		µs
$t_{SU;STA}$	Start Setup Time	2.0		µs
$t_{HD\ DAT}$	Data In Hold Time	0		µs
$t_{SU\ DAT}$	Data In Setup Time	0.2		µs
t_R	Inputs Rise Time		0.3	µs
t_F	Inputs Fall Time		0.3	µs
$t_{SU\ STO}$	Stop Setup Time	2.0		µs
t_{DH}	Data Out Hold Time	0.1		µs
t_{WR}	Write Cycle Time		20	ms

Notes: 1. This parameter is characterized and is not 100% tested.
2. Commercial temperature range 15°C - 70°C
3. Industrial temperature range 15°C - 85°C
4. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)

Figure 14. Serial Data Timing Diagram



Pin Configurations

20-pin PLCC A Series Only[2]	20pin PLCC/SOIC Device	8-pin DIP Device[2]	Name	I/O	Description
2	2	1	DATA	I/O	Three-state DATA output for configuration. Open-collector bi-directional pin for programming.
4	4	2	CLK	I/O	CLOCK input/output. Used to increment the internal address and bit counter for reading and programming. Can be programmed as an output for the 512A/010A/002A only.
5[1]	5[1]	N/A	WP1 (512/010/002 only)	I/O	Write Protect (1). Used to inhibit Write instructions to blocks of memory (512/010/002 only). Can be combined with WP2, if available, to define portions of the memory that will not be overwritten.
8	6	3	RESET/$\overline{OE}$	I	RESET/$\overline{OE}$ input (when $\overline{SER\_EN}$ is High). A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This document describes the pin as RESET/$\overline{OE}$.
			RESET Polarity Select (65/128/256 only)	I	RESET Polarity Select input. During programming, when $\overline{CE}$ is High, this input is used to determine the polarity of the RESET pin (for operation when $\overline{SER\_EN}$ is High).
			WP (65/128/256 only)	I	Write Protect (WP) input (when $\overline{CE}$ is Low). When WP is Low or floating, the entire memory can be written. When WP is enabled (High), the lowest block of the memory cannot be written, i.e., 32K in 65 parts, 32K in 128 parts and 64K in 256 parts. Note that when WP is High, the chip will still acknowledge the receipt of data, but it will not write it into memory.
N/A	7[1]	N/A	WP2 (512/010/002 only)	I	Write Protect (2). Used to inhibit Write instructions to blocks of memory (512/010/002 only). Combined with WP1, this pin defines portions of the memory that will not be written.
9	8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection only when $\overline{SER\_EN}$ is High. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low-power mode. Note this pin will not enable/disable the device in the 2-wire Serial mode (i.e., when $\overline{SER\_EN}$ is driven Low). During programming of 65/128/256 parts, when $\overline{CE}$ is Low, the main array is read and written. When $\overline{CE}$ is High, the main array is deselected and a Serial WRITE operation will change the polarity of the RESET pin.

Pin Configurations (Continued)

20-pin PLCC A Series Only[2]	20pin PLCC/SOIC Device	8-pin DIP Device[2]	Name	I/O	Description
10	10	5	GND		Ground pin.
12	14[1]	6	$\overline{CEO}$	O	Chip Enable output when $\overline{SER\_EN}$ is High. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter, $\overline{CEO}$ will stay High until the entire PROM is read again.
			A2	I	Device selection input, A2. Used to enable (select) the device during programming. When $\overline{SER\_EN}$ is Low, this pin must be at either a logic level “1” or “0” (i.e., not tri-state) and the A2 bit of the Device Address must match the condition of this pin for the Configurator to be selected.
15	15	N/A	READY (512/010/020/002 only)	O	Ready output (512/010/020/002 only). This pin is an open-collector indicator of the device’s internal power-up RESET condition. It is driven Low until the power-up RESET is cleared, at which time it is released to a tri-state condition. This can be used with an external pull-up resistor for a Ready indication.
18	17	7	$\overline{SER\_EN}$	I	Serial enable is normally High during FPGA loading operations. Bringing $\overline{SER\_EN}$ Low enables the programming mode.
20	20	8	V_{CC}		Power Supply pin.

Notes: 1. This input pin contains a weak internal pull-down and, when forced High, will draw ~5 µA/pin current while $\overline{SER\_EN}$ is Low. It will draw no current when $\overline{SER\_EN}$ is High.
2. Refer to Altera conversion application note.

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