MOSFET – N-Channel, POWERTRENCH®

100 V, 12 A, 110 mΩ

FDMC3612, FDMC3612-L701

General Description

This N−Channel MOSFET is produced using ON Semiconductor’s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

Features

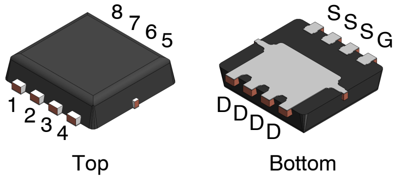
- Max $r_{DS(on)}$ = 110 mΩ at V_{GS} = 10 V, I_D = 3.3 A
- Max $r_{DS(on)}$ = 122 mΩ at V_{GS} = 6 V, I_D = 3.0 A
- Low Profile − 1 mm Max in Power 33
- 100% UIL Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

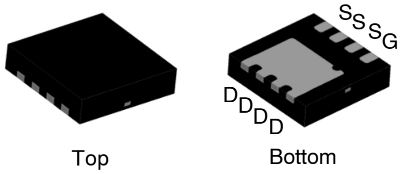
- DC − DC Conversion
- PSE Switch

ON Semiconductor®

www.onsemi.com

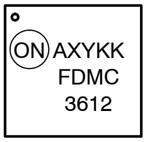


WDFN8 3.3x3.3, 0.65P
CASE 511DR
FDMC3612

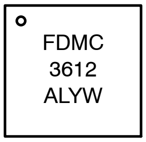


WDFN8 3.3x3.3, 0.65P
CASE 511DQ
FDMC3612−L701

MARKING DIAGRAM



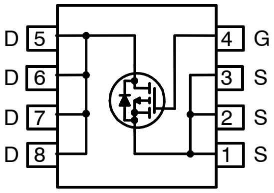
FDMC3612



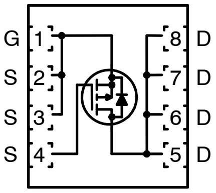
FDMC3612−L701

FDMC3612 = Specific Device Code
A = Assembly Location
XY = 2−Digit Date Code
KK = 2−Digit Lot Run Traceability Code
L = Wafer Lot Number
YW = Assembly Start Week

PIN ASSIGNMENT



FDMC3612



FDMC3612−L701

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

February, 2020 − Rev. 4

Publication Order Number:
FDMC3612/D

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

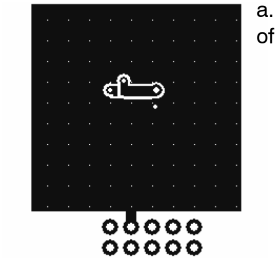
Symbol	Parameter			Rating	Unit
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current	Continuous (Package limited)	T_C = 25°C	16	A
		Continuous (Silicon limited)	T_C = 25°C	12	
		Continuous (Note 1a)	T_A = 25°C	3.3	
		Pulsed		15	
E_{AS}	Single Pulse Avalanche Energy (Note 2)			32	mJ
P_D	Power Dissipation		T_C = 25°C	35	W
	Power Dissipation (Note 1a)		T_A = 25°C	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

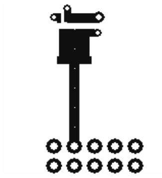
THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Starting T_J = 25°C; N−ch: L = 1 mH, I_{AS} = 8 A, V_{DD} = 90 V, V_{GS} = 10 V.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	109	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	2.5	4.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–7	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 3.3 A	–	92	110	mΩ
		V_{GS} = 6 V, I_D = 3.0 A	–	98	122	
		V_{GS} = 10 V, I_D = 3.3 A, T_J = 125°C	–	177	212	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.3 A	–	13	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	662	880	pF
C_{oss}	Output Capacitance		–	40	55	pF
C_{rss}	Reverse Transfer Capacitance		–	23	35	pF
R_g	Gate Resistance		–	1.3	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 3.3 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	7.4	15	ns
t_r	Rise Time		–	2.8	10	ns
$t_{d(off)}$	Turn−Off Delay Time		–	19	34	ns
t_f	Fall Time		–	2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 3.3 A	–	14.4	21	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 5 V, V_{DD} = 50 V, I_D = 3.3 A	–	7.9	12	nC
Q_{gs}	Total Gate Charge	V_{DD} = 50 V, I_D = 3.3 A	–	2.3	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	3.7	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.3 A (Note 3)	–	0.88	1.2	V
		V_{GS} = 0 V, I_S = 2 A (Note 3)	–	0.77	1.2	
t_{rr}	Reverse Recovery Time	I_F = 3.3 A, di/dt = 100 A/μs	–	34	55	ns
Q_{rr}	Reverse Recovery Charge		–	37	60	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

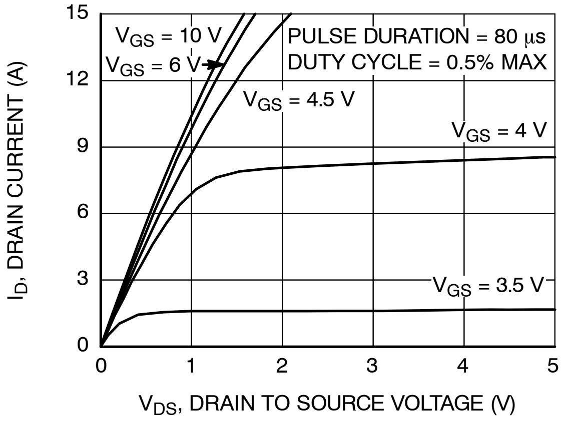


Figure 1. On Region Characteristics

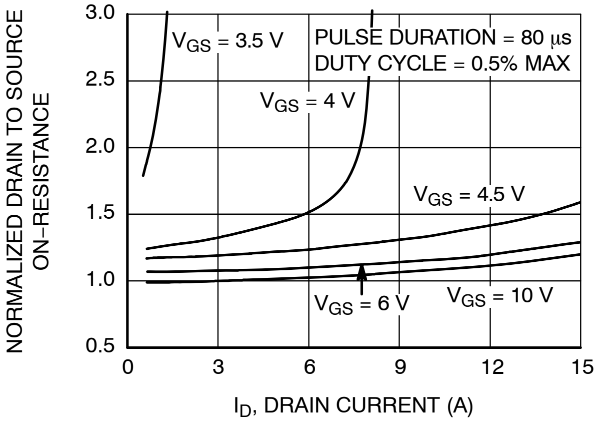


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

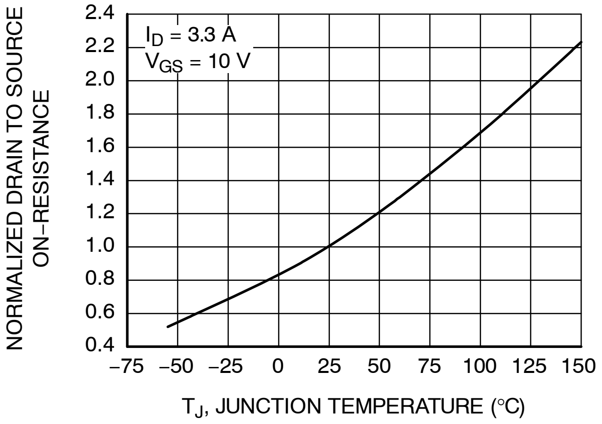


Figure 3. Normalized On Resistance vs. Junction Temperature

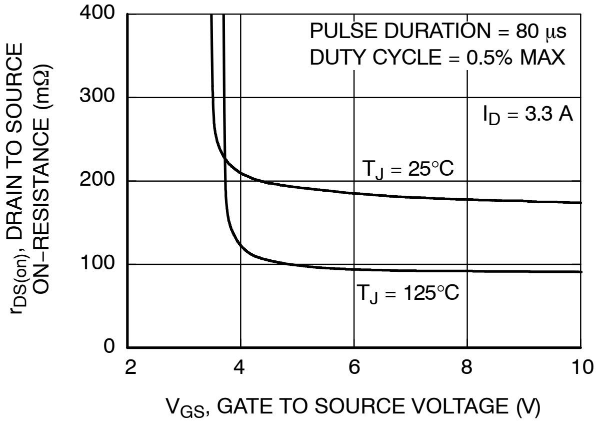


Figure 4. On−Resistance vs. Gate to Source Voltage

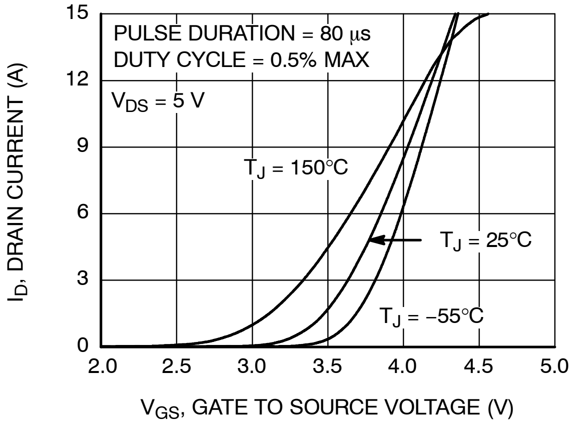


Figure 5. Transfer Characteristics

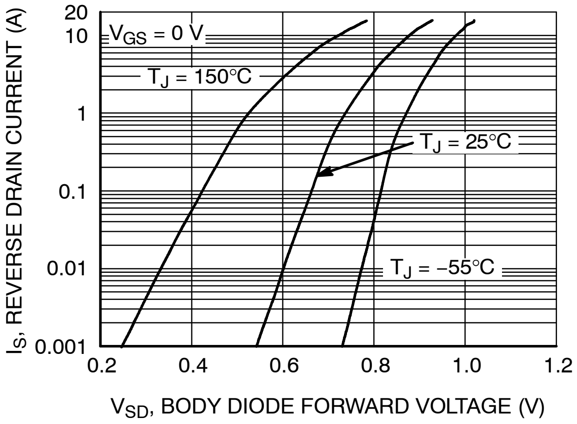


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

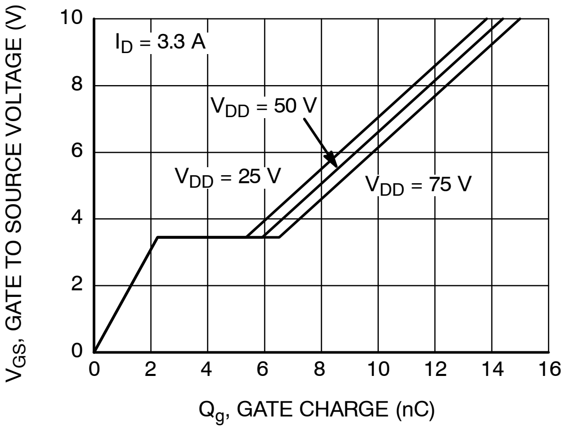


Figure 7. Gate Charge Characteristics

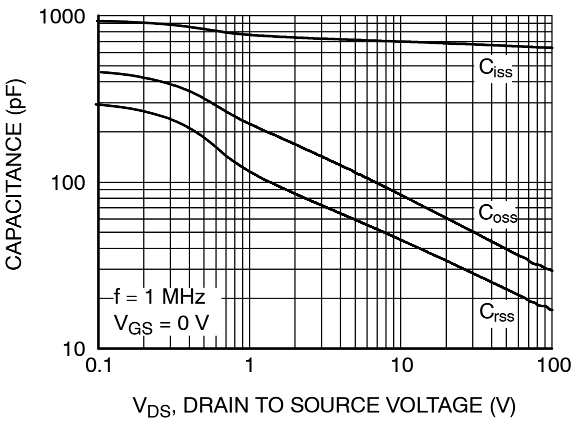


Figure 8. Capacitance vs. Drain to Source Voltage

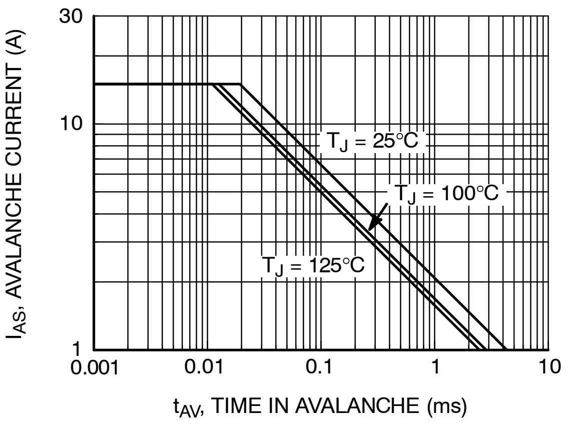


Figure 9. Unclamped Inductive Switching Capability

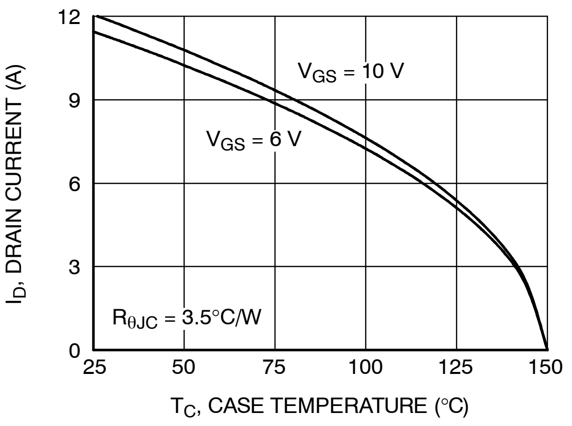


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

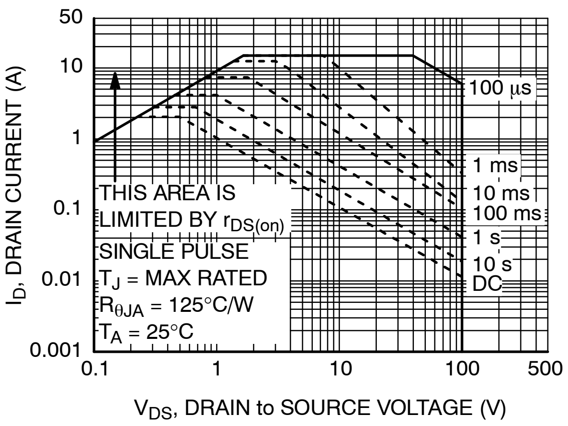


Figure 11. Forward Bias Safe Operating Area

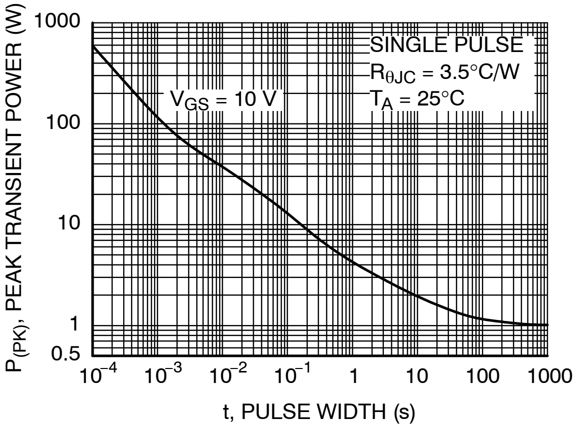


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

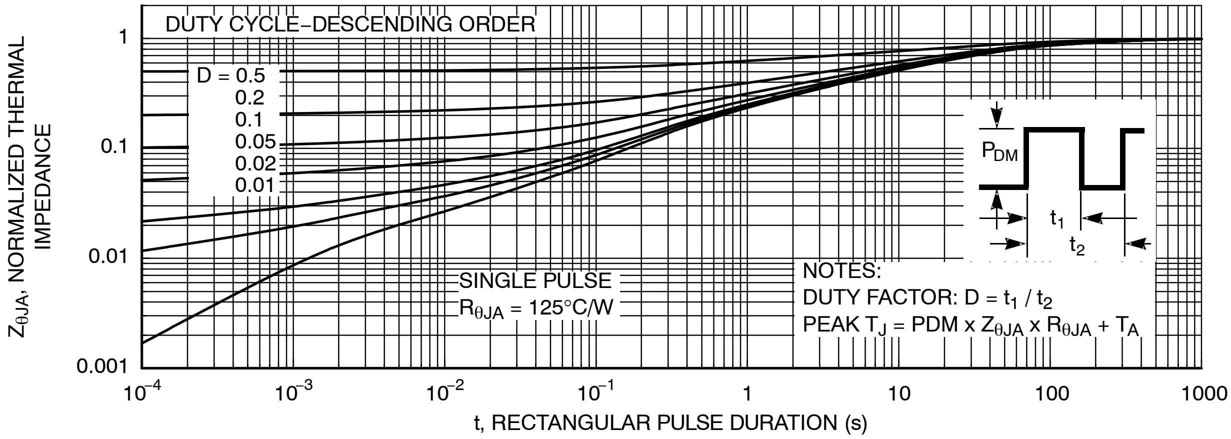


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

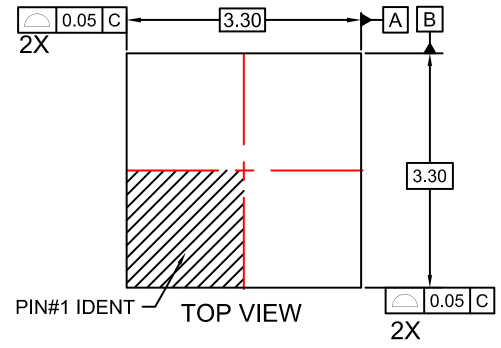
ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDMC3612	FDMC3612	WDFN8 3.3x3.3, 0.65P Power 33 (Pb−Free)	13”	12 mm	3000 / Tape & Reel
FDMC3612−L701	FDMC3612	WDFN8 3.3x3.3, 0.65P Power 33 (Pb−Free)	13”	12 mm	3000 / Tape & Reel

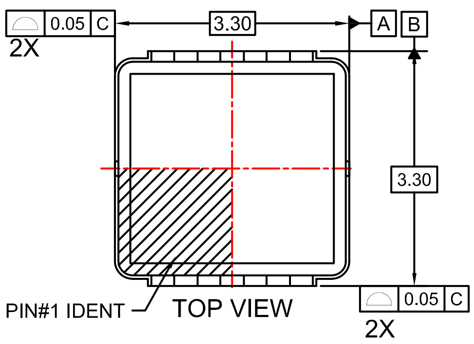
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN8 3.3x3.3, 0.65P
CASE 511DQ
ISSUE O

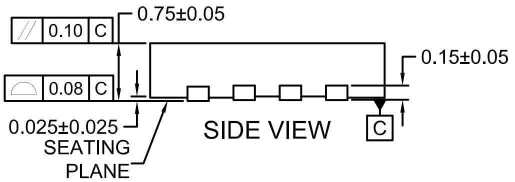
DATE 31 OCT 2016



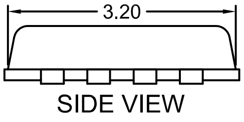
TOP VIEW



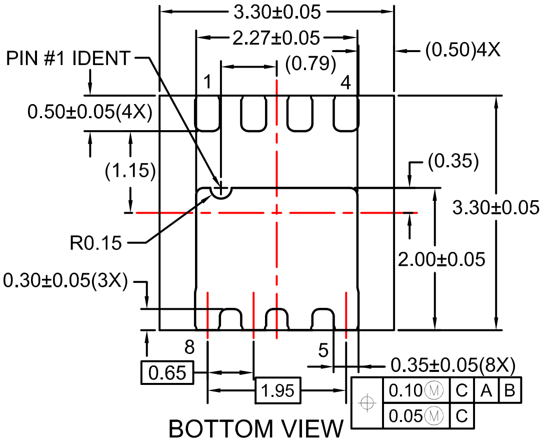
TOP VIEW



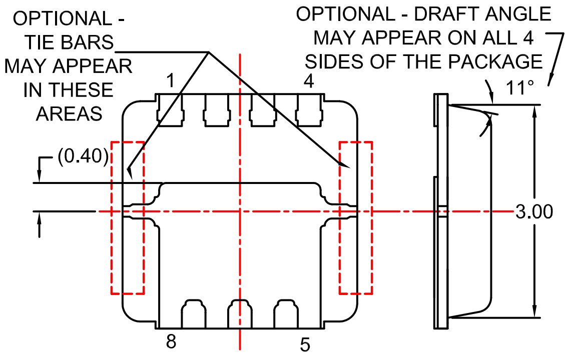
SIDE VIEW



SIDE VIEW

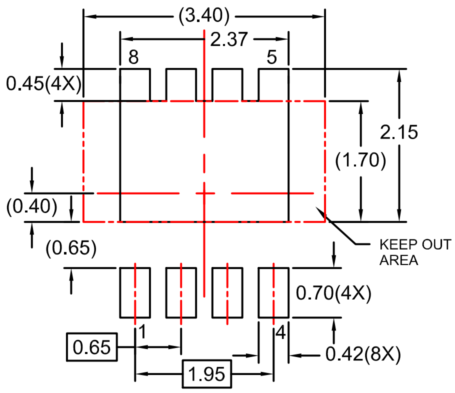


BOTTOM VIEW
(OPTION A)



ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION B)

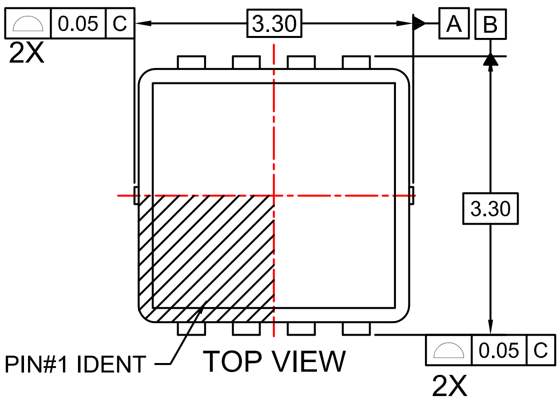


RECOMMENDED LAND PATTERN

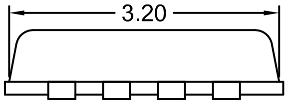
DOCUMENT NUMBER:	**98AON13648G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 2**

WDFN8 3.3x3.3, 0.65P
CASE 511DQ
ISSUE O

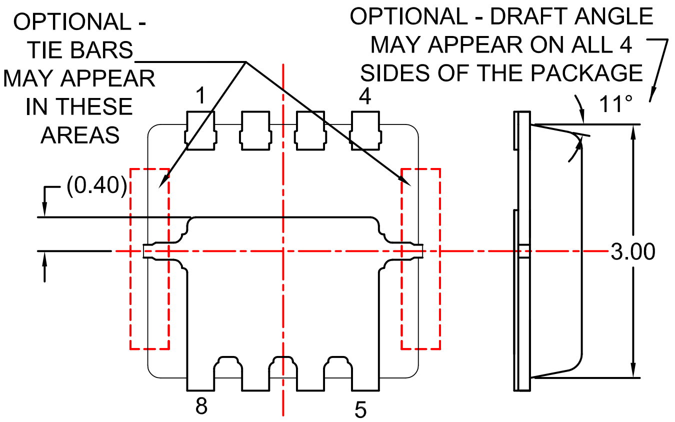
DATE 31 OCT 2016



TOP VIEW



SIDE VIEW



ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

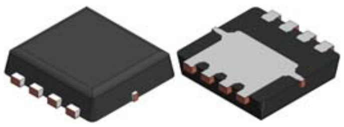
NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

DOCUMENT NUMBER:	**98AON13648G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 2 OF 2**

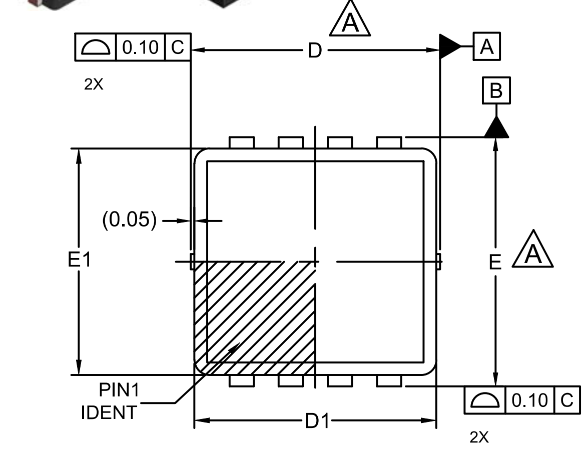
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

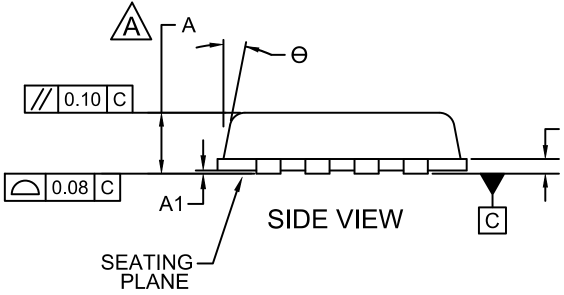


WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE A

DATE 18 SEP 2018



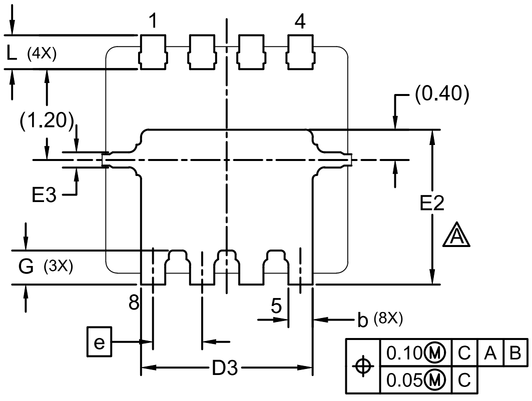
TOP VIEW



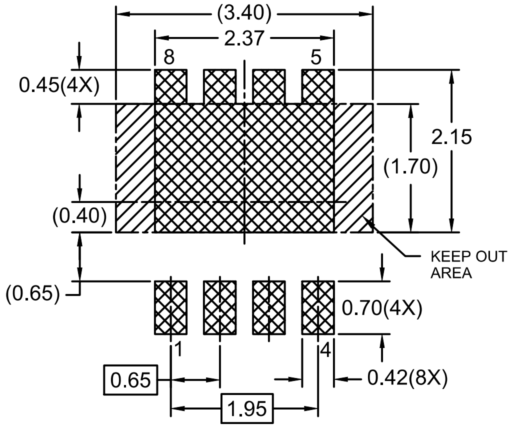
SIDE VIEW

NOTES:
A. DIMENSIONS ARE IN MILLIMETERS.
B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
C. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
D. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
e	0.65 BSC		
G	0.40	0.45	0.50
L	0.40	0.45	0.50
θ	0	-	12

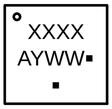


BOTTOM VIEW



RECOMMENDED LAND PATTERN

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13650G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WDFN8 3.3x3.3, 0.65P**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative