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# FDMT800152DC

## N-Channel Dual Cool™ 88 PowerTrench® MOSFET

150 V, 72 A, 9.0 mΩ

### Features

- Max  $r_{DS(on)}$  = 9.0 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 13\text{ A}$
- Max  $r_{DS(on)}$  = 11.5 mΩ at  $V_{GS} = 6\text{ V}$ ,  $I_D = 11\text{ A}$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- Low profile 8x8mm MLP package
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

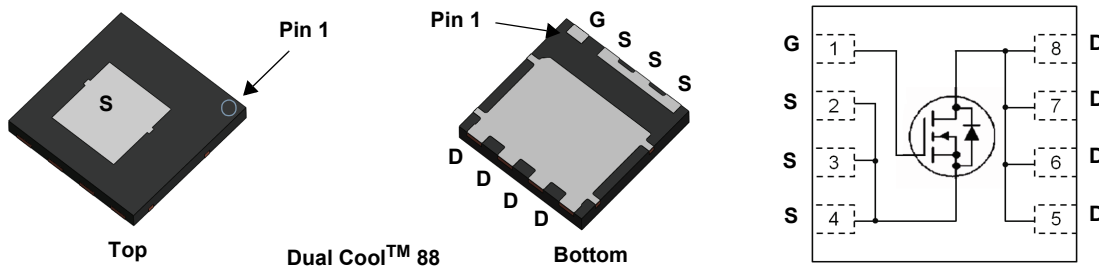


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

### Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$ (Note 5)	72
	-Continuous	$T_C = 100\text{ °C}$ (Note 5)	45
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	13
	-Pulsed	(Note 4)	413
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	726
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	113
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	3.2
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Top Source)	2.0	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Bottom Drain)	1.1	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1k)	9	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
800152DC	FDMT800152DC	Dual Cool™ 88	13"	13.3 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		114		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	2.9	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-11		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 13\text{ A}$		6.9	9.0	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 11\text{ A}$		8.6	11.5	
		$V_{GS} = 10\text{ V}$ , $I_D = 13\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		14.6	19	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 13\text{ A}$		41		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		4196	5875	pF
$C_{oss}$	Output Capacitance			379	530	pF
$C_{rss}$	Reverse Transfer Capacitance			16	30	pF
$R_g$	Gate Resistance		0.1	1.3	3.3	$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}$ , $I_D = 13\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		24	39	ns
$t_r$	Rise Time			13	23	ns
$t_{d(off)}$	Turn-Off Delay Time			36	58	ns
$t_f$	Fall Time			7.9	16	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 75\text{ V}$ , $I_D = 13\text{ A}$	59	83	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }6\text{ V}$		38	53	nC
$Q_{gs}$	Gate to Source Charge			18		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			12		nC

**Drain-Source Diode Characteristics**

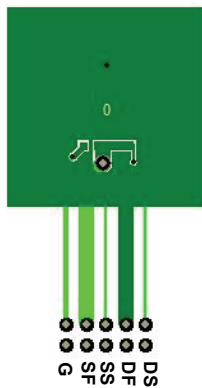
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.9\text{ A}$ (Note 2)		0.7	1.1	V
		$V_{GS} = 0\text{ V}$ , $I_S = 13\text{ A}$ (Note 2)		0.8	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		95	152	ns
$Q_{rr}$	Reverse Recovery Charge			187	299	nC

## Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Top Source)	2.0	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Bottom Drain)	1.1	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1e)	14	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1f)	16	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1h)	60	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1k)	9	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1l)	11	

### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below.  $R_{\theta CA}$  is determined by the user's board design.



a. 38  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 81  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 726 mJ is based on starting  $T_j = 25^{\circ}\text{C}$ ; N-ch: L = 3 mH,  $I_{AS} = 22\text{ A}$ ,  $V_{DD} = 150\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at L = 0.1 mH,  $I_{AS} = 69\text{ A}$ .

4. Pulsed Id please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

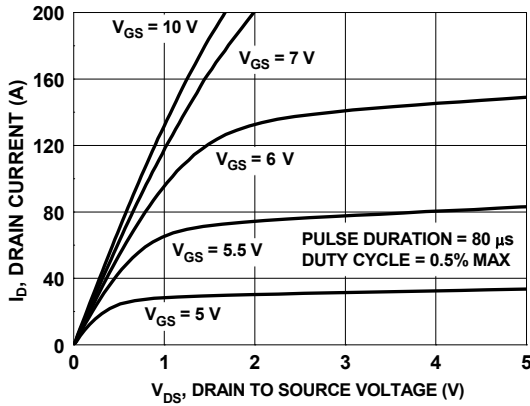


Figure 1. On-Region Characteristics

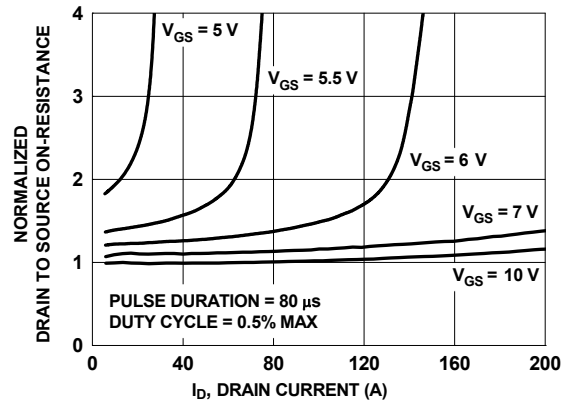


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

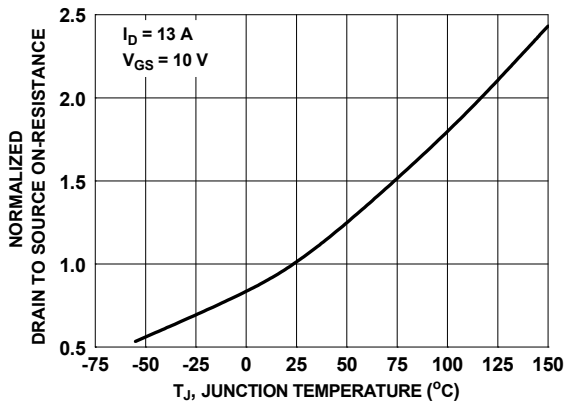


Figure 3. Normalized On-Resistance vs. Junction Temperature

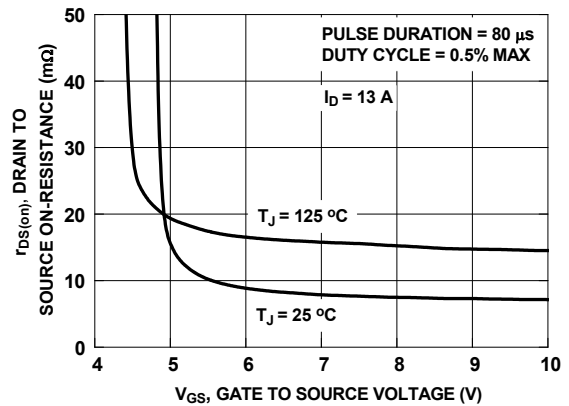


Figure 4. On-Resistance vs. Gate to Source Voltage

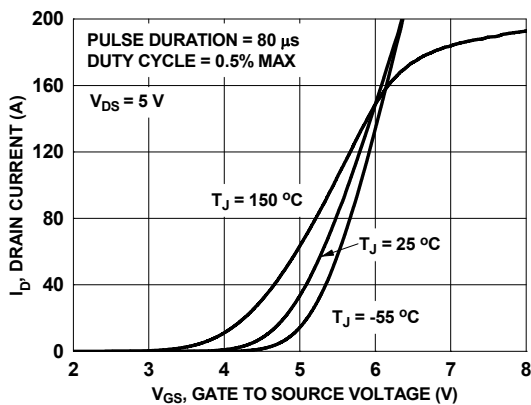


Figure 5. Transfer Characteristics

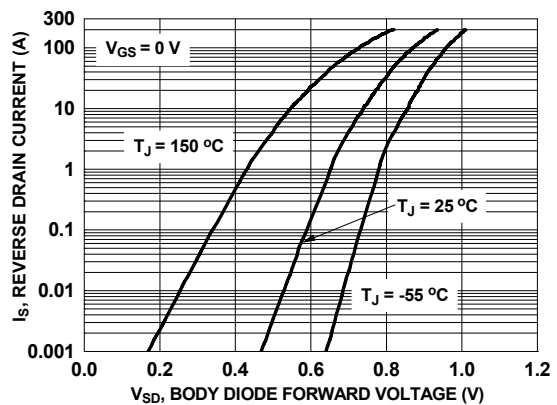
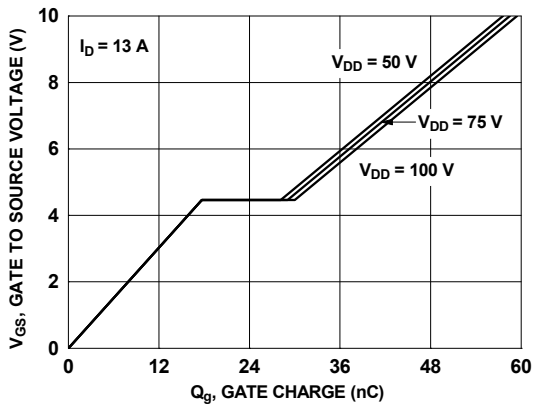
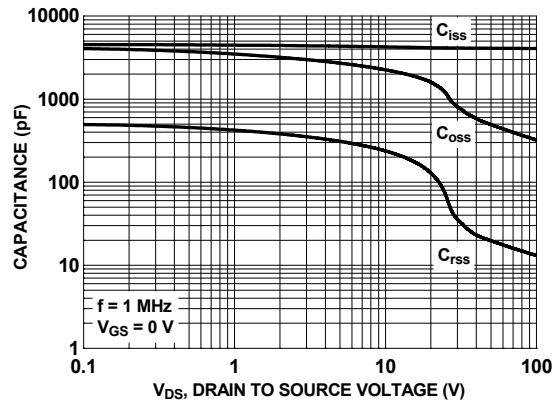


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

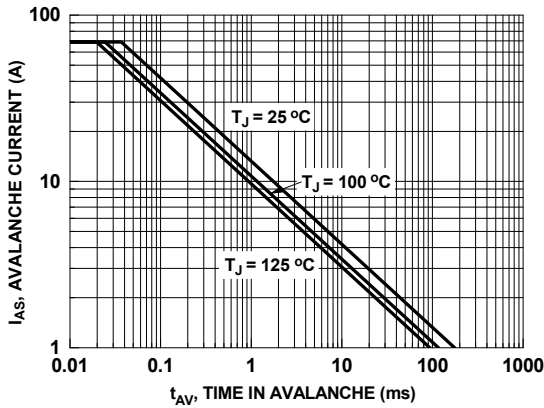
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



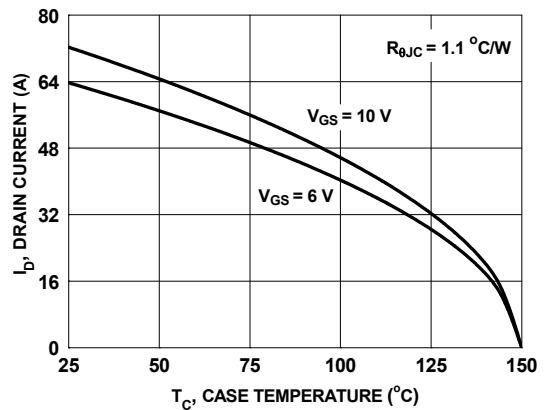
**Figure 7. Gate Charge Characteristics**



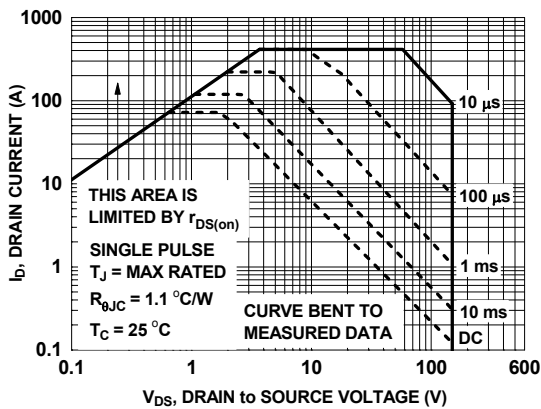
**Figure 8. Capacitance vs. Drain to Source Voltage**



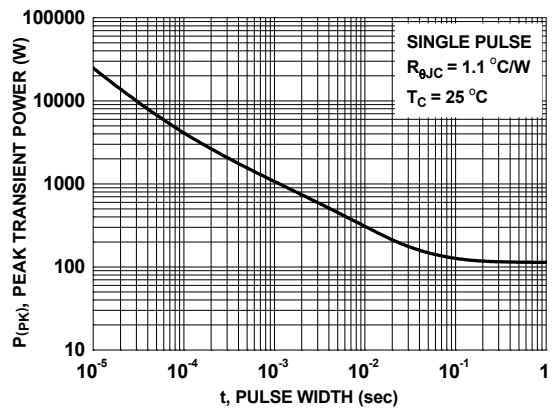
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

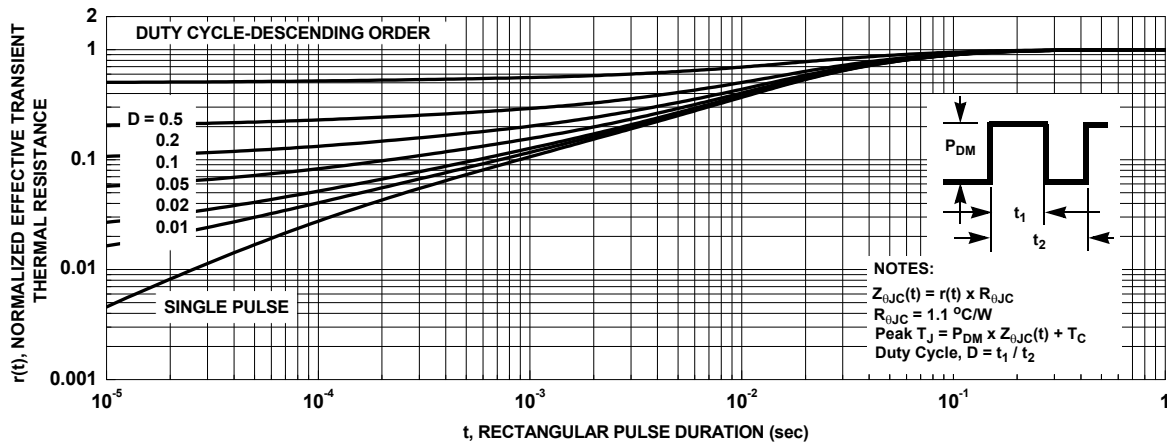


**Figure 11. Forward Bias Safe Operating Area**

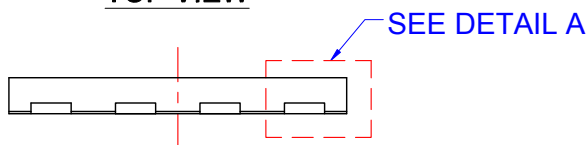
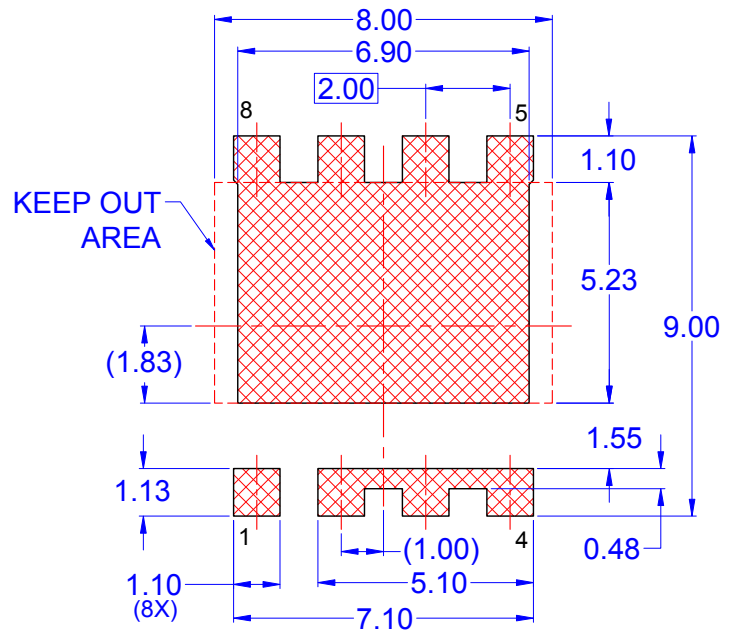
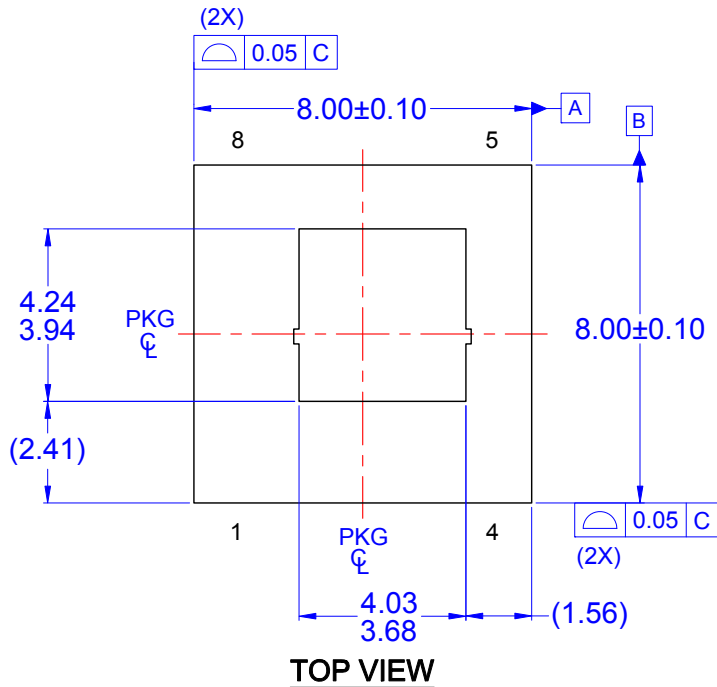


**Figure 12. Single Pulse Maximum Power Dissipation**

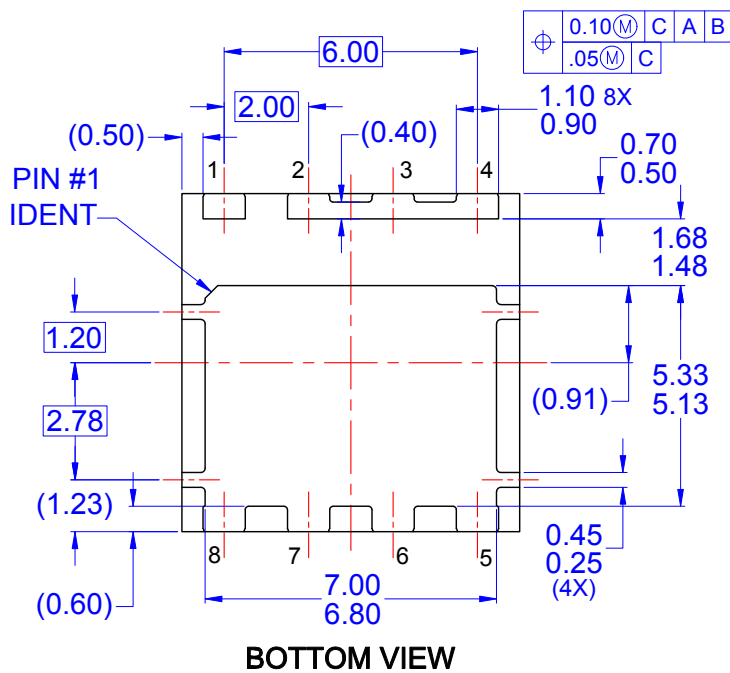
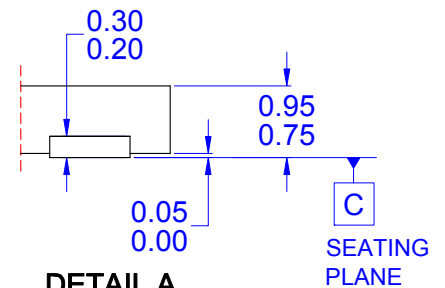
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



**Figure 13. Junction-to-Case Transient Thermal Response Curve**



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