

MOSFET – Power, Single, N-Channel, Logic Level, SOT-23

60 V, 155 mΩ

NTR5198NL

Features

- Small Footprint Industry Standard Surface Mount SOT-23 Package
- Low $R_{DS(on)}$ for Low Conduction Losses and Improved Efficiency
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

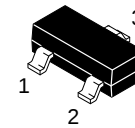
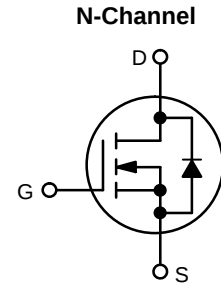
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	60	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 2, 3, 4, and 5)	Steady State	$T_A = 25^\circ\text{C}$	I_D 2.2 A
		$T_A = 100^\circ\text{C}$	1.6
		$T_A = 25^\circ\text{C}$	P_D 1.5 W
		$T_A = 100^\circ\text{C}$	0.6
Power Dissipation $R_{\Psi J-mb}$ (Notes 2 and 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D 1.7 A
		$T_A = 100^\circ\text{C}$	1.2
		$T_A = 25^\circ\text{C}$	P_D 0.9 W
		$T_A = 100^\circ\text{C}$	0.4
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	I_{DM} 27	A
Operating Junction and Storage Temperature	T_J , T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	1.9	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

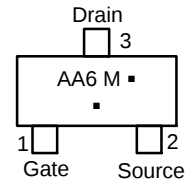
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
4. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
5. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
60 V	155 mΩ @ 10 V	2.2 A
	205 mΩ @ 4.5 V	



SOT-23
CASE 318
STYLE 21

MARKING DIAGRAM/ PIN ASSIGNMENT



AA6 = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

* For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping [†]
NTR5198NLT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

DISCONTINUED (Note 1)

NTR5198NLT3G	SOT-23 (Pb-Free)	10000 / Tape & Reel
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[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your onsemi representative for information. The most current information on this device may be available on www.onsemi.com.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Lead #3 – Drain (Notes 3 and 4)	$R_{\Psi J-mb}$	86	°C/W
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	139	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 250\text{ }\mu\text{A}$		70		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25\text{ }^{\circ}\text{C}$		1.0	μA
			$T_J = 125\text{ }^{\circ}\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.5		2.5	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 250\text{ }\mu\text{A}$		-6.5		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1\text{ A}$		107	155	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 1\text{ A}$		142	205	
Forward Transconductance	g_{FS}	$V_{DS} = 5.0\text{ V}, I_D = 1\text{ A}$		3		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		182		pF
Output Capacitance	C_{oss}			25		
Reverse Transfer Capacitance	C_{rss}			16		
Total Gate Charge	$Q_{G(TOT)}$	$V_{DS} = 48\text{ V}, I_D = 1\text{ A}$	$V_{GS} = 4.5\text{ V}$	2.8		nC
			$V_{GS} = 10\text{ V}$	5.1		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{DS} = 48\text{ V}, I_D = 1\text{ A}, V_{GS} = 10\text{ V}$		0.3		
Gate-to-Source Charge	Q_{GS}			0.8		
Gate-to-Drain Charge	Q_{GD}			1.5		
Plateau Voltage	V_{GP}			3.1		V
Gate Resistance	R_G			8		Ω

SWITCHING CHARACTERISTICS (Note 7)

Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 1\text{ A}, R_G = 10\text{ }\Omega$		5		ns
Rise Time	t_r			7		
Turn-Off Delay Time	$t_{d(off)}$			13		
Fall Time	t_f			2		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 1\text{ A}$	$T_J = 25\text{ }^{\circ}\text{C}$		0.8	1.2	V
			$T_J = 125\text{ }^{\circ}\text{C}$		0.6		
Reverse Recovery Time	t_{rr}	$I_S = 1\text{ A}_{dc}, V_{GS} = 0\text{ V}_{dc}, dI_S/dt = 100\text{ A}/\mu\text{s}$		12		ns	
Charge Time	t_a			9			
Discharge Time	t_b			3			
Reverse Recovery Stored Charge	Q_{RR}			6			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

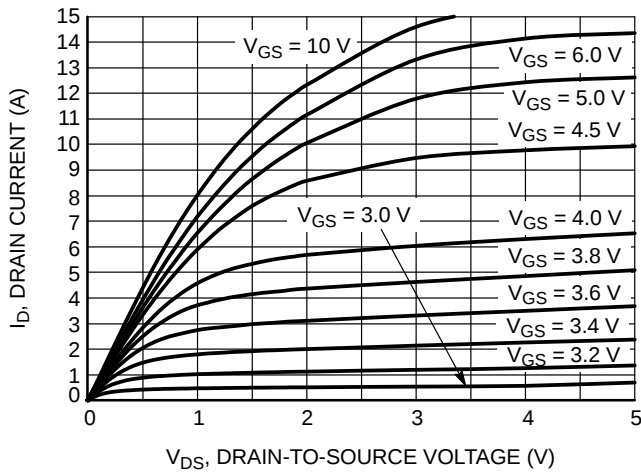


Figure 1. On-Region Characteristics

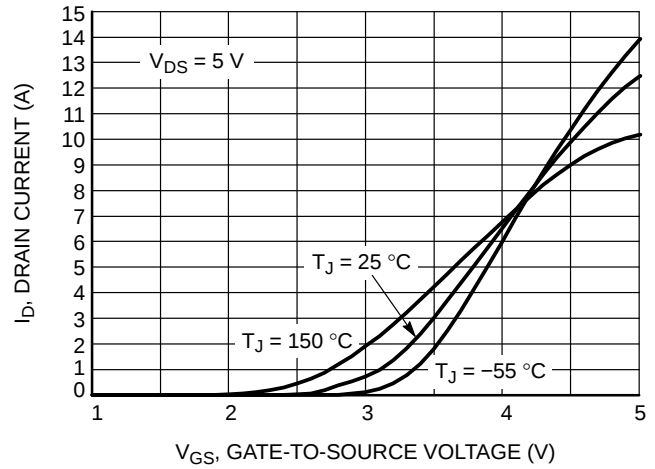


Figure 2. Transfer Characteristics

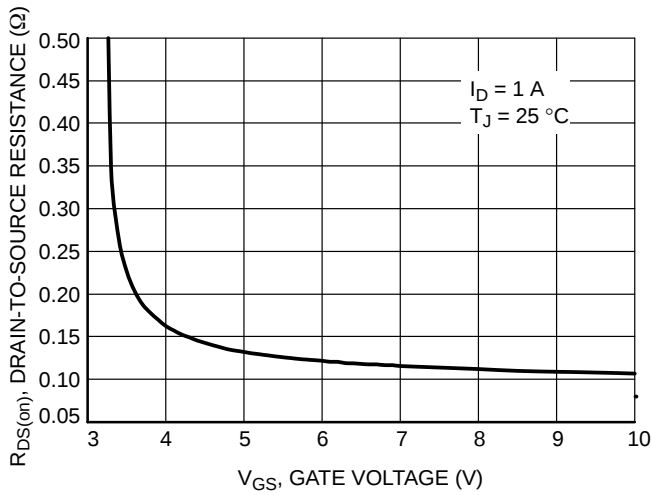


Figure 3. On-Resistance vs. Gate-to-Source Voltage

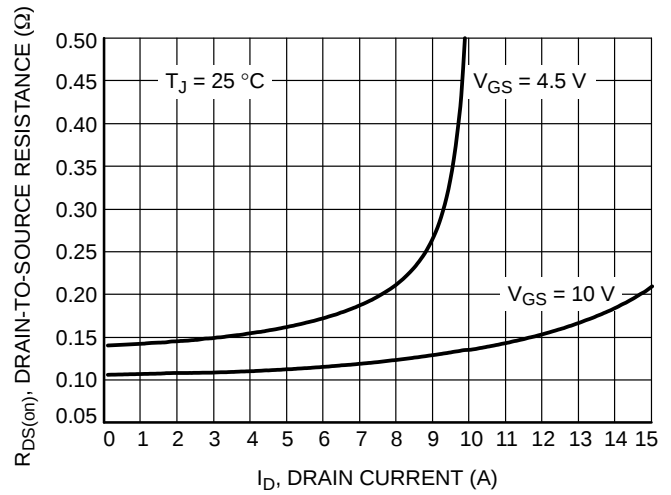


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

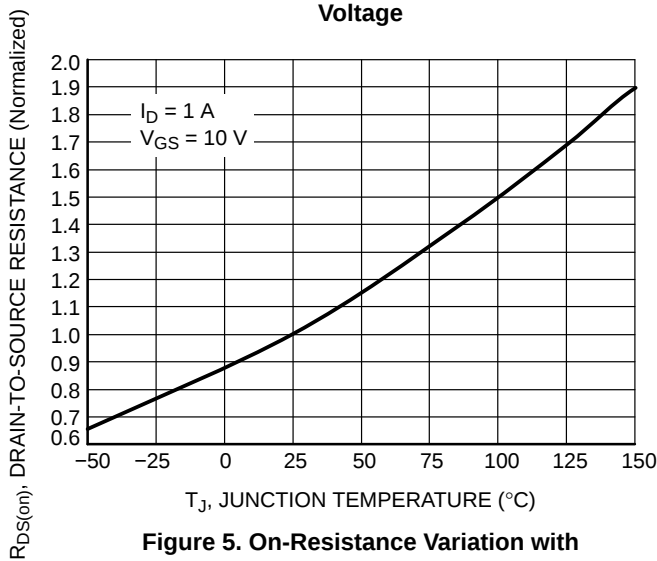


Figure 5. On-Resistance Variation with Temperature

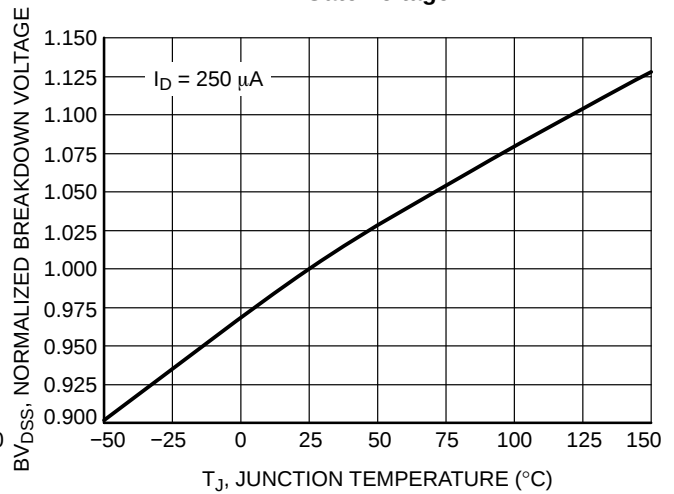


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

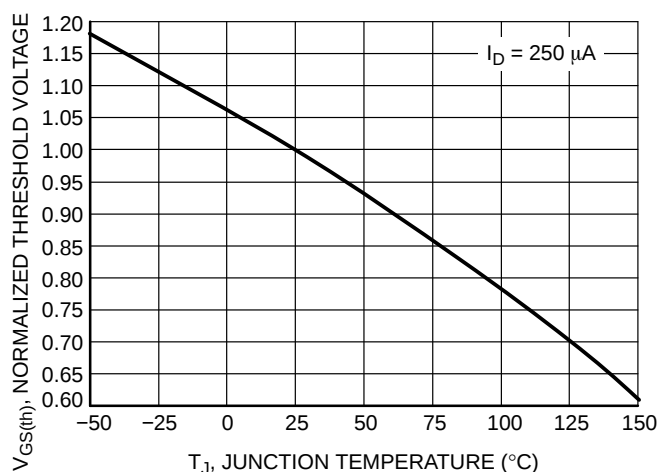


Figure 7. Threshold Voltage Variation with Temperature

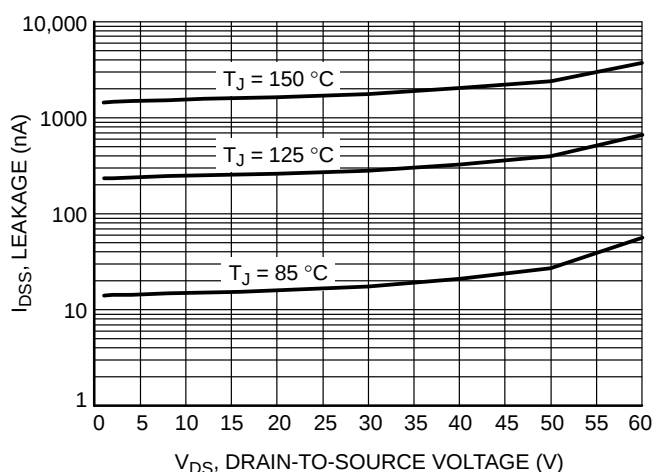


Figure 8. Drain-to-Source Leakage Current vs. Voltage

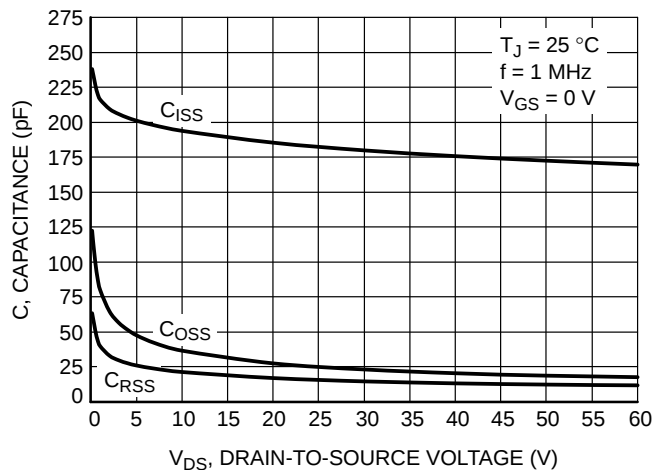


Figure 9. Capacitance Variation

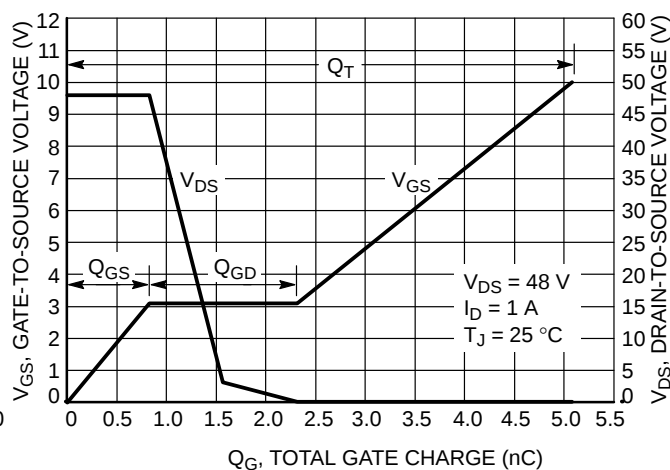


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

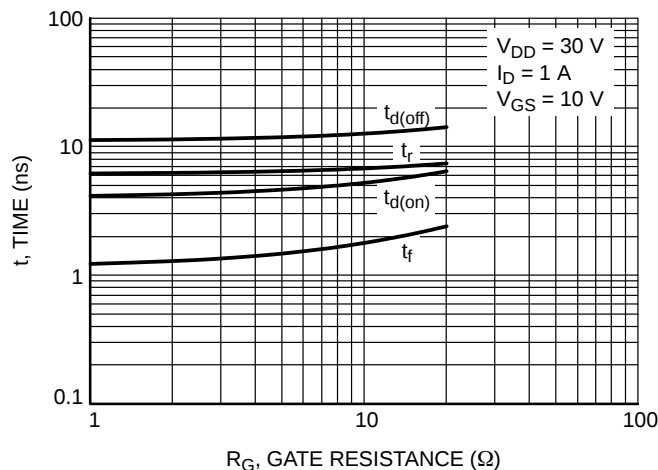


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

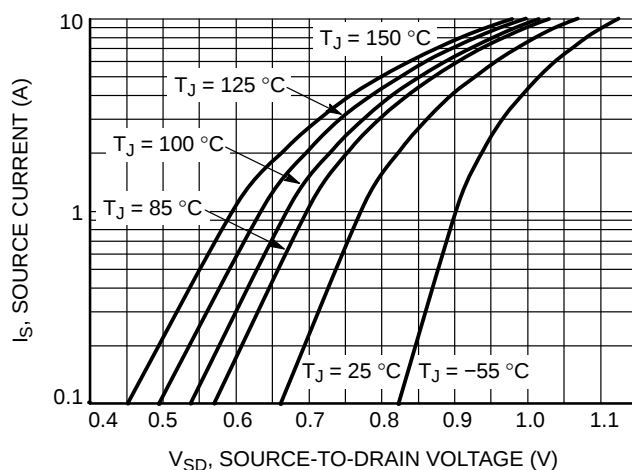


Figure 12. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

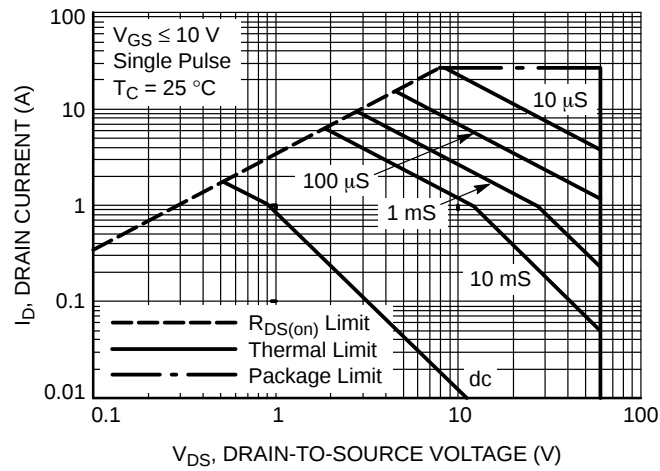


Figure 13. Maximum Rated Forward Biased Safe Operating Area

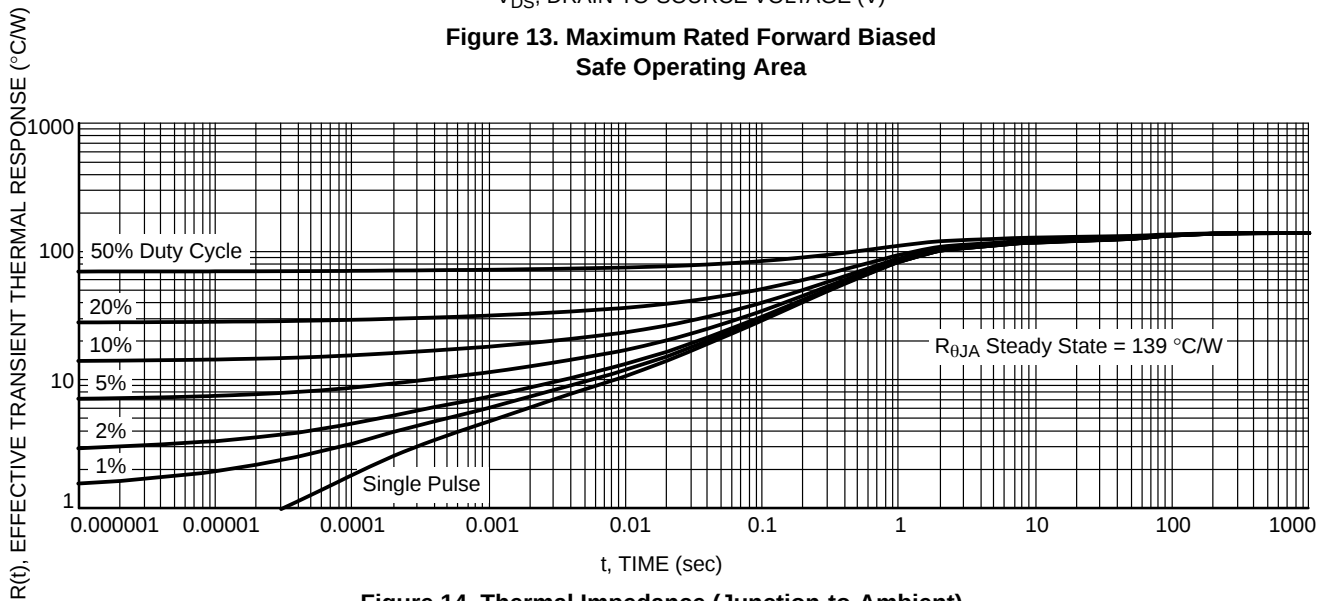


Figure 14. Thermal Impedance (Junction-to-Ambient)

NTR5198NL

REVISION HISTORY

Revision	Description of Changes	Date
3	Rebranded the Data Sheet to onsemi format. NTR5198NLT3G OPN marked as Discontinued.	10/22/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

STYLES ON PAGE 2

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CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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