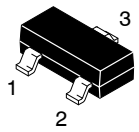
MOSFET – Power, Single N-Channel, Logic Level, SOT-23

60 V, 155 mΩ

NVR5198NL

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
60 V	155 mΩ @ 10 V	2.2 A
	205 mΩ @ 4.5 V	

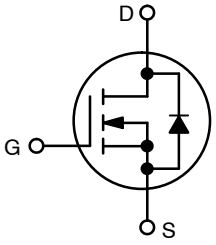


SOT-23
CASE 318
STYLE 21

Features

- Small Footprint Industry Standard Surface Mount SOT-23 Package
- Low $R_{DS(on)}$ for Low Conduction Losses and Improved Efficiency
- NVR Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

N-Channel



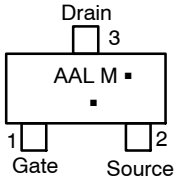
MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			60	V
V_{GS}	Gate-to-Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\Psi Jmb}$ (Notes 1, 2, 3, and 4)	Steady State	T_{mb} = 25 °C	2.2	A
			T_{mb} = 100 °C	1.6	
P_D	Power Dissipation $R_{\Psi Jmb}$ (Notes 1 and 3)		T_{mb} = 25 °C	1.5	W
			T_{mb} = 100 °C	0.6	
I_D	Continuous Drain Current $R_{\theta JA}$ (Note 1, 2, 3, and 4)	Steady State	T_A = 25 °C	1.7	A
			T_A = 100 °C	1.2	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1 and 3)		T_A = 25 °C	0.9	W
			T_A = 100 °C	0.4	
I_{DM}	Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		27	A
T_J, T_{stg}	Operating Junction and Storage Temperature			−55 to 150	°C
I_S	Source Current (Body Diode)			1.9	A
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm2, 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM/ PIN ASSIGNMENT



AAL = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

* For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
NVR5198NLT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel
NVR5198NLT3G	SOT-23 (Pb-Free)	10,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\Psi Jmb}$	Junction-to-Lead #3 - Drain (Notes 2 and 3)	86	°C/W
$R_{\theta JA}$	Junction-to-Ambient - Steady State (Note 3)	139	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		60	–	–	V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	Reference to 25 °C, I_D = 250 μA		–	70	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C	–	–	1.0	μA
			T_J = 125 °C	–	–	10	
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS (Note 5)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1.5	–	2.5	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient	Reference to 25 °C, I_D = 250 μA		–	–6.5	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 10 V, I_D = 1 A		–	107	155	mΩ
		V_{GS} = 4.5 V, I_D = 1 A		–	142	205	
g_{FS}	Forward Transconductance	V_{DS} = 5.0 V, I_D = 1 A		–	3	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{iss}	Input Capacitance	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V		–	182	–	pF
C_{oss}	Output Capacitance			–	25	–	
C_{rss}	Reverse Transfer Capacitance			–	16	–	
$Q_{G(TOT)}$	Total Gate Charge	V_{DS} = 48 V, I_D = 1 A	V_{GS} = 4.5 V	–	2.8	–	nC
			V_{GS} = 10 V	–	5.1	–	
$Q_{G(TH)}$	Threshold Gate Charge	V_{DS} = 48 V, I_D = 1 A V_{GS} = 10 V		–	0.3	–	
Q_{GS}	Gate-to-Source Charge			–	0.8	–	
Q_{GD}	Gate-to-Drain Charge			–	1.5	–	
V_{GP}	Plateau Voltage			–	3.1	–	V
R_G	Gate Resistance			–	8	–	Ω
SWITCHING CHARACTERISTICS (Note 6)							
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 1 A, R_G = 10 Ω		–	5	–	ns
t_r	Rise Time			–	7	–	
$t_{d(off)}$	Turn-Off Delay Time			–	13	–	
t_f	Fall Time			–	2	–	
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 1 A	T_J = 25 °C	–	0.8	1.2	V
			T_J = 125 °C	–	0.6	–	
t_{rr}	Reverse Recovery Time	I_S = 1 A_{dc}, V_{GS} = 0 V_{dc}, dI_S/dt = 100 A/μs		–	12	–	ns
t_a	Charge Time			–	9	–	
t_b	Discharge Time			–	3	–	
Q_{RR}	Reverse Recovery Stored Charge			–	6	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

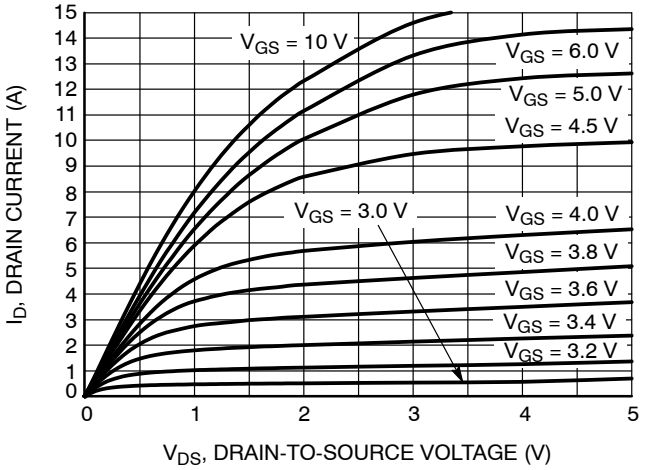


Figure 1. On-Region Characteristics

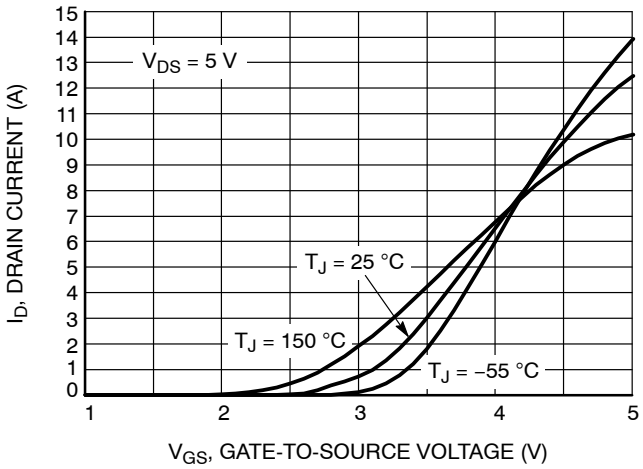


Figure 2. Transfer Characteristics

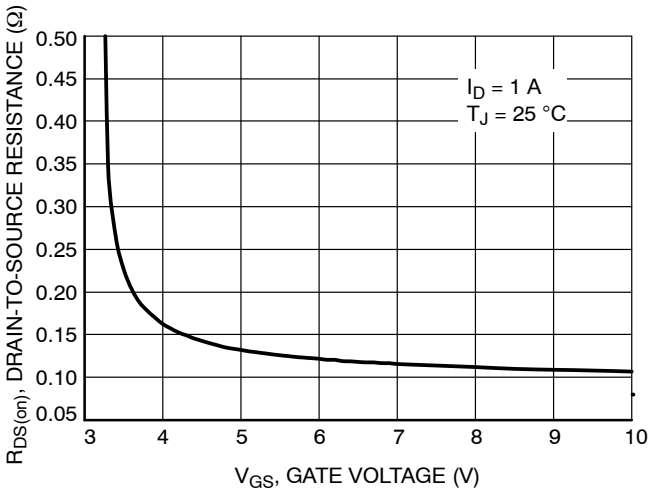


Figure 3. On-Resistance vs. Gate-to-Source Voltage

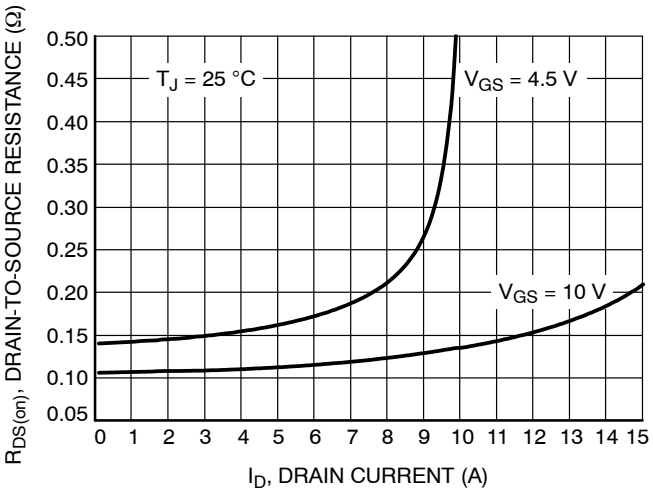


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

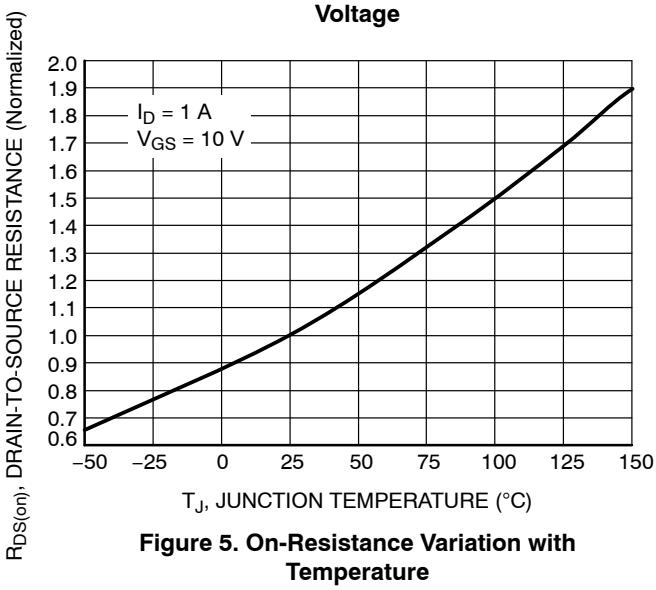


Figure 5. On-Resistance Variation with Temperature

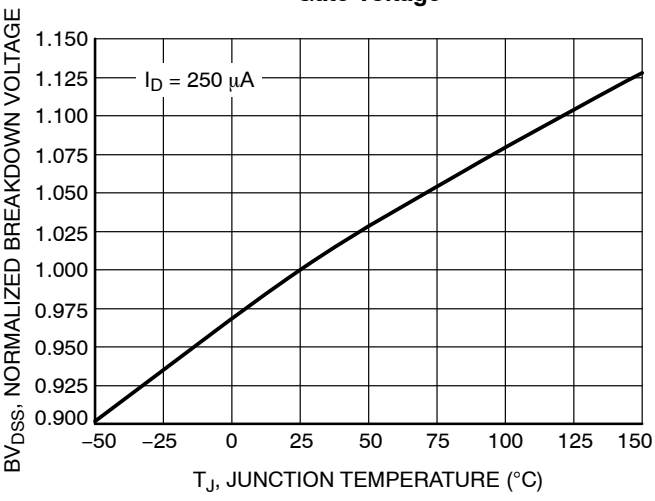


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS (continued)

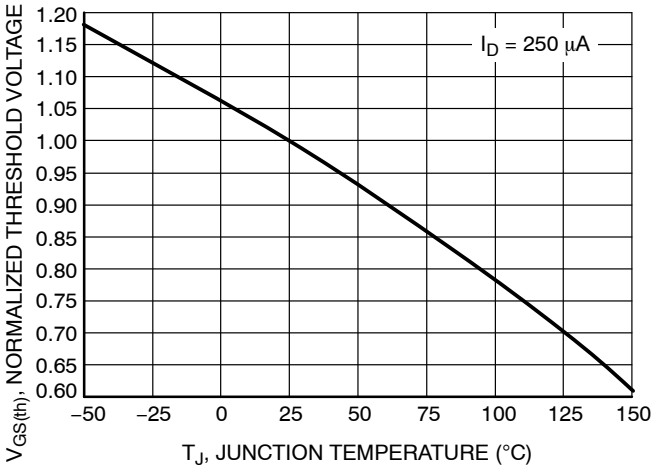


Figure 7. Threshold Voltage Variation with Temperature

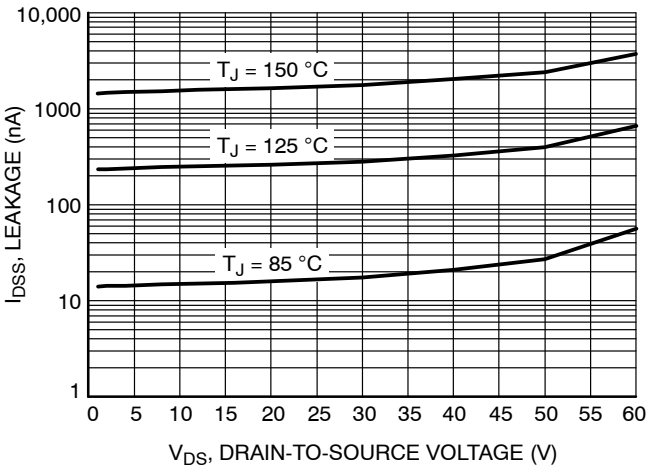


Figure 8. Drain-to-Source Leakage Current vs. Voltage

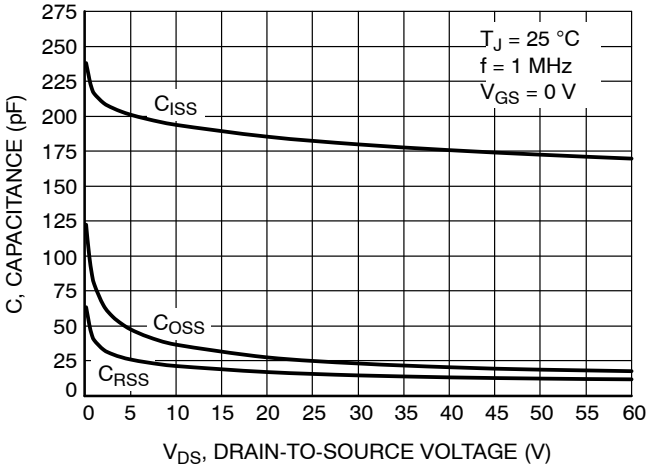


Figure 9. Capacitance Variation

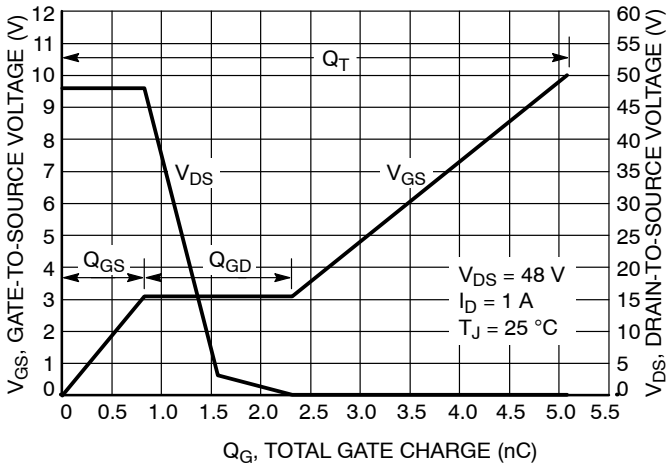


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

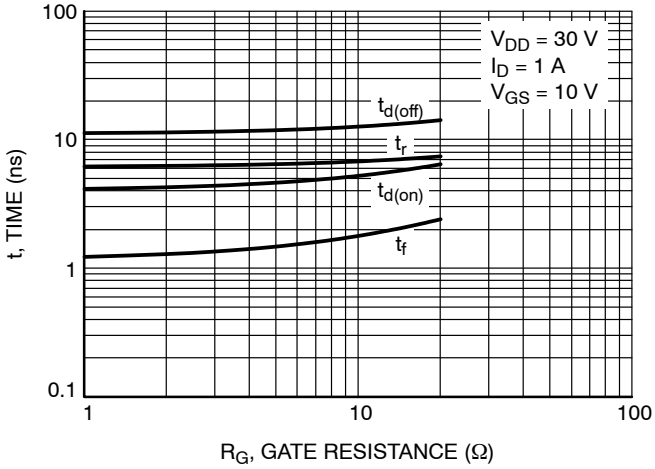


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

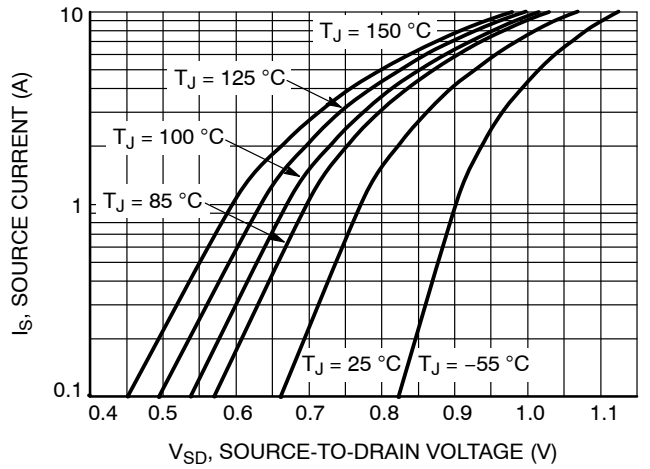


Figure 12. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (continued)

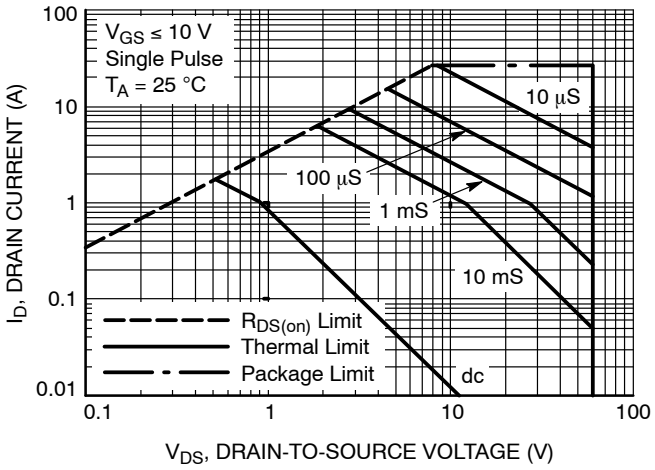


Figure 13. Maximum Rated Forward Biased Safe Operating Area

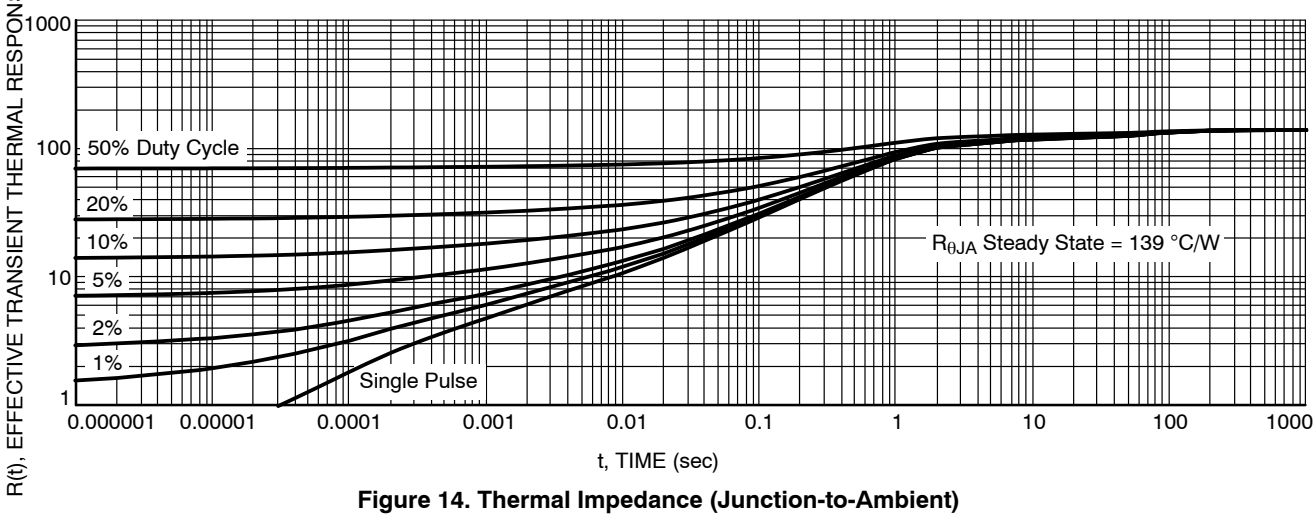
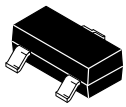


Figure 14. Thermal Impedance (Junction-to-Ambient)

REVISION HISTORY

Revision	Description of Changes	Date
4	Rebranded the Data Sheet to **onsemi** format.	12/10/2025

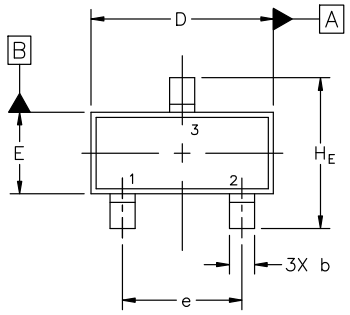
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



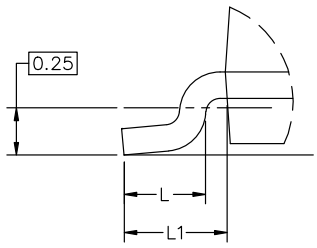
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

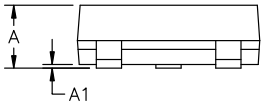
DATE 14 AUG 2024



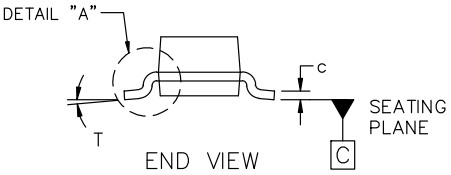
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

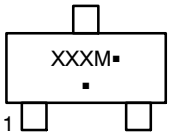


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

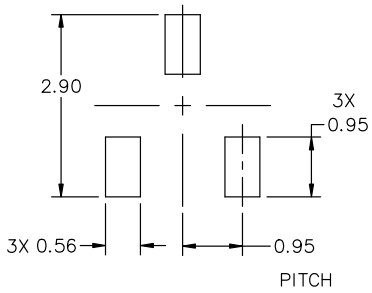
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**		**PAGE 1 OF 2**

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

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