P89C51Rx2/ 01

8-bit 80C51 Flash Microcontroller Family with In-System Programming and In-Application Programming Capability

Semiconductors

Description

The P89C51Rx2 series are 80C51 microcontrollers with up to 64 Kbytes Flash and 1024 bytes of data RAM.

A key feature of the P89CRx2 is its X2 mode option. The design engineer can choose to run the application with the conventional 80C51 clock rate (12-clocks per machine cycle) or select the X2 mode (6-clock per machine cycle) to achieve twice the throughput at the same clock frequency. Another way to benefit from this feature is to keep the same performance by reducing the clock frequency by half, thus dramatically reducing the EMI.

The Flash program memory supports both parallel programming and serial In-System Programming (ISP). Parallel programming mode offers gang-programming at high speed, reducing programming costs and time to market. ISP allows a device to be reprogrammed in the end product under software control. The capability to field/update the application firmware makes a wide range of applications possible.

The P89C51Rx2 family is also In-Application Programmable (IAP), allowing the Flash program memory to be reconfigured even while the application is running.

Features

- 80C51 Central Processing Unit
- On-chip Flash Program Memory with In-SystemProgramming (ISP) and In-Application Programming (IAP) capability
- Boot ROM contains low level Flash programming routines for downloading via the UART
- Programmable Counter Array (PCA)
  - PWM
  - Capture/compare
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Four 8-bit I/O ports
- Supports 12-clk/6-clk mode selection via software, ISP or parallel programmer (default clock mode after ChipErase is 12-clock)
- Peripherals (PCA, timers, UART) may use either 6-clock or 12-clock mode while the CPU is in 6-clock mode
- Speed up to 20 MHz with 6-clock cycles per machine cycle (40 MHz equivalent performance); up to 33 MHz with 12 clocks per machine cycle
- Power control modes
  - Clock can be stopped and resumed
  - Idle mode
  - Power down mode
- Programmable clock-out pin

Applications

- LCD Monitor
- Printer Panel
- Industrial Control

Benefits

- 6-clock mode provides twice the performance of the conventional 80C51
- Flexible clock selection options
- Supports additional 4 Kbyte Flash sector size

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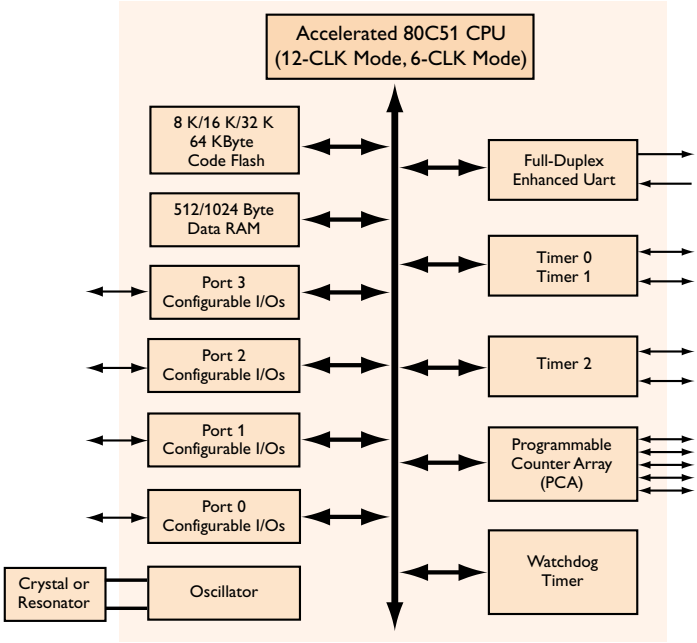
Ordering information

Part Number	Memory		Temp. Range & Package	Voltage	Frequency (MHz)	
	Flash	RAM			6-clk mode	12-clk mode
P89C51RA2BA/01	8 KB	512 B	0° to +70°C, PLCC	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RA2BBD/01	8 KB	512 B	0° to +70°C, LQFP	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RB2BA/01	16 KB	512 B	0° to +70°C, PLCC	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RB2BBD/01	16 KB	512 B	0° to +70°C, LQFP	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RC2BN/01	32 KB	512 B	0° to +70°C, PDIP	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RC2BA/01	32 KB	512 B	0° to +70°C, PLCC	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RC2FA/01	32 KB	512 B	-40° to +85°C, PLCC	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RC2BBD/01	32 KB	512 B	0° to +70°C, LQFP	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RC2FBD/01	32 KB	512 B	-40° to +85°C, PLCC	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RD2BN/01	64 KB	1024 B	0° to +70°C, PDIP	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RD2BA/01	64 KB	1024 B	0° to +70°C, PLCC	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RD2BBD/01	64 KB	1024 B	0° to +70°C, LQFP	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz
P89C51RD2FA/01	64 KB	1024 B	-40° to +85°C, PLCC	4.5-5.5 V	0 to 20 MHz	0 to 33 MHz

Device comparison table

Item Type Description	1st Generation of Rx2 Device P89C51Rx2Hxx(x)	2nd Generation of Rx2 Device (this leaflet) P89C51Rx2(x)	Difference No More Letter 'H'
Programming algorithm	When using a parallel programmer, be sure to select P89C51Rx2Hxx(x) devices	When using a parallel programmer, be sure to select P89C51Rx2(x) devices (no more letter 'H')	Different programming algorithm due to process change
Clock Mode (I)	**6-clk default, OTP** configuration bit to program to **12-clk** mode using parallel programmer (cannot be programmed back to 6-clk)	**12-clk default, FLASH** configuration bit to program to **6 - clk** mode using parallel programmer or ISP/IAP (can be programmed back to 12-clk)	More flexibility for the end user more compatibility to older P89C51Rx+ parts
Clock Mode (II)	N/A	6-clk/12-clk mode programmable "on the fly" by SFR bit X2 (CKCON.0)	Clock mode can be changed by software
Peripheral clock modes	N/A	Peripherals can be run in 12-clk mode while CPU runs in 6-clk mode	More flexibility lower power consumption
Flush block structure	Two 8-Kbyte blocks 1-3 16-Kbyte blocks	2-16 4-Kbyte blocks Also supported	More flexibility

P89C51Rx2 block diagram



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