ERRATA SHEET

Date: **September 04, 2002**
Document Release: **Version 1.0**
Devices Affected: **P89C51RA2 /01, P89C51RB2 /01, P89C51RC2 /01, P89C51RD2 /01**
(referenced to as P89C51Rx2 /01 in this document)

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2002 Sep 04

Philips Semiconductors

PHILIPS

On-chip Flash 8-bit microcontroller Errata Sheet

P89C51Rx2 /01

IDENTIFICATION:

The P89C51Rx2 /01 devices have the following top-side marking (PLCC44 package shown):

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89C51Rx2 /01:

Revision Identifier (R)	Comment
'B'	Initial release

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that same year.

NOTE: The P89C51Rx2 /01 devices discussed in this Errata Sheet belong to Philips' 2nd generation of Rx2 devices. This Errata Sheet does **not** apply to Philips' 1st generation of Rx2 devices, marked P89C51Rx2**H**.

FUNCTIONAL DEVIATIONS OF P89C51RX2 /01

ISP/IAP.1: ISP Mode entry during Power-On Reset w/ $\overline{\text{PSEN}}$ low

Problem: If a Power-On Reset is applied to the device while the $\overline{\text{PSEN}}$ pin is held low, the part will not enter ISP mode as expected but executes user code instead.

In this particular case, the user code will execute in 12-clk mode, even if the device had been previously programmed to 6-clk mode.

Workarounds: The following workarounds are available to allow ISP mode entry:

1.) Apply an additional "warm" reset (holding the RST pin HIGH for at least two machine cycles) after power-up while $\overline{\text{PSEN}}$ is low.

2.) Make V_{PP} rise slower with respect to V_{CC} during Power-up while $\overline{\text{PSEN}}$ is low by permanently connecting an RC circuit to V_{PP} as shown in Figure 1.

For V_{PP} = 5 V, choose R = 3.3 K and C = 10 μF.

For V_{PP} = 12 V, choose R = 10 K and C = 10 μF.

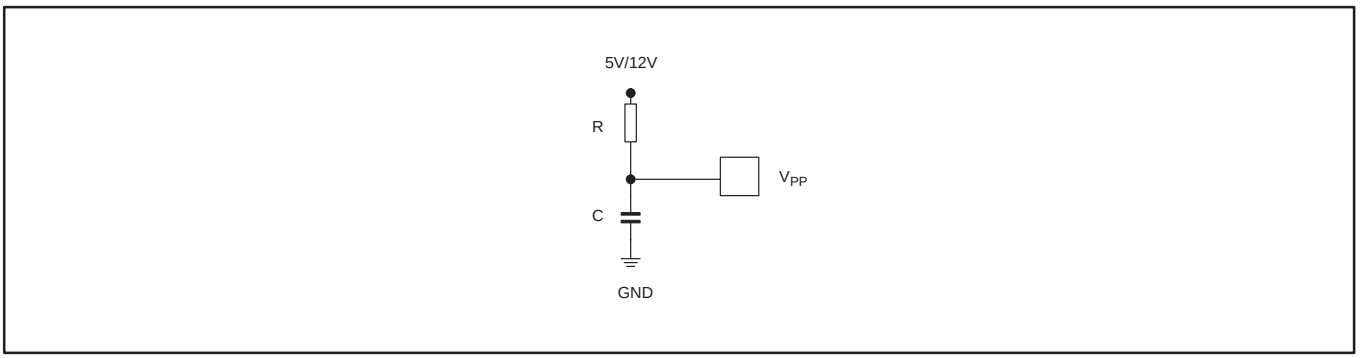

Figure 1.

3.) In case an external adapter or a jumper is used to force the device into ISP mode on Power-up:

Instead of holding $\overline{\text{PSEN}}$ low during power-up, delay $\overline{\text{PSEN}}$ going low with respect to Vcc by connecting an RC circuit to $\overline{\text{PSEN}}$ as shown in Figure 2.

Choose R = 3.3 K and C = 10 μF.

Please note that this RC circuit needs to be disconnected after ISP mode was entered and the chip has been programmed in order to have the chip execute user code after the next reset.

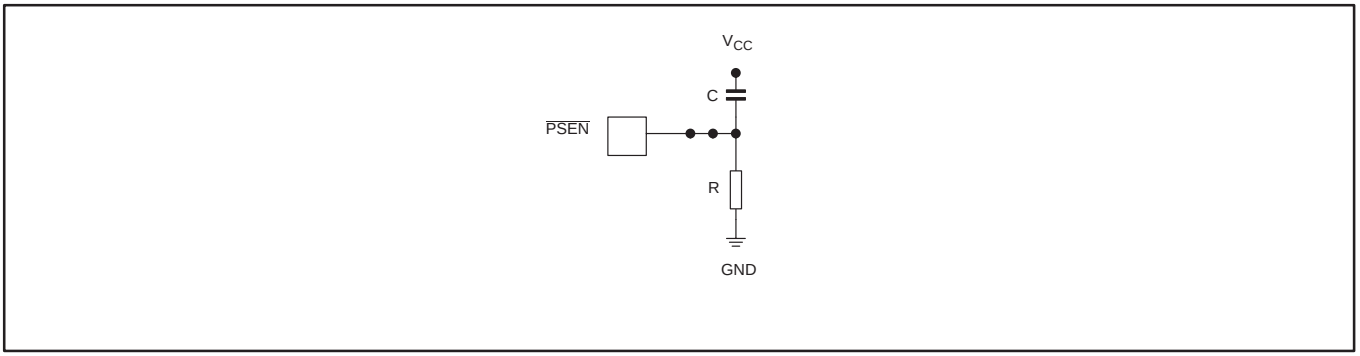

Figure 2.

ELECTRICAL AND TIMING SPECIFICATION DEVIATIONS OF P89C51RX2 /01

No known deviations at the release of this document.

ERRATA HISTORY - FUNCTIONAL PROBLEMS

Functional Problem	Short Description	problem occurs in device revision
ISP/IAP.1	ISP Mode entry during Power-On Reset w/ $\overline{\text{PSEN}}$ low	'B'

ERRATA HISTORY - AC/DC DEVIATIONS

AC/DC Deviation	Short Description	problem occurs in device revision
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