

SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

SCLS039D – DECEMBER 1982 – REVISED MARCH 2001

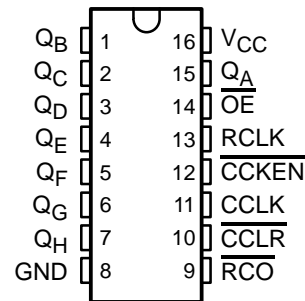
- 8-Bit Counter With Register
- High-Current 3-State Parallel Register Outputs Can Drive up to 15 LSTTL Loads
- Counter Has Direct Clear

description

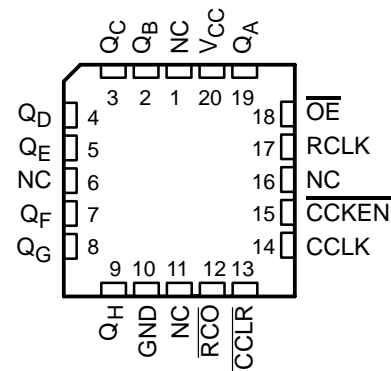
The 'HC590A devices contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features direct clear ($\overline{\text{CCLR}}$) and count-enable ($\overline{\text{CCKEN}}$) inputs. A ripple-carry output ($\overline{\text{RCO}}$) is provided for cascading. Expansion is accomplished easily for two stages by connecting $\overline{\text{RCO}}$ of the first stage to $\overline{\text{CCKEN}}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{\text{RCO}}$ of each stage to the counter clock ($\overline{\text{CCLK}}$) input of the following stage.

Both $\overline{\text{CCLK}}$ and the register clock ($\overline{\text{RCLK}}$) input are positive-edge triggered. If both clocks are connected together, the counter state always is one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

SN54HC590A . . . J OR W PACKAGE
SN74HC590A . . . D, DW, OR N PACKAGE
(TOP VIEW)



SN54HC590A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74HC590AN	SN74HC590AN
	SOIC – D	Tube	SN74HC590AD	HC590A
		Tape and reel	SN74HC590ADR	
	SOIC – DW	Tube	SN74HC590ADW	HC590A
Tape and reel		SN74HC590ADWR		
-55°C to 125°C	CDIP – J	Tube	SNJ54HC590AJ	SNJ54HC590AJ
	CFP – W	Tube	SNJ54HC590AW	SNJ54HC590AW
	LCCC - FK	Tube	SNJ54HC590AFK	SNJ54HC590AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

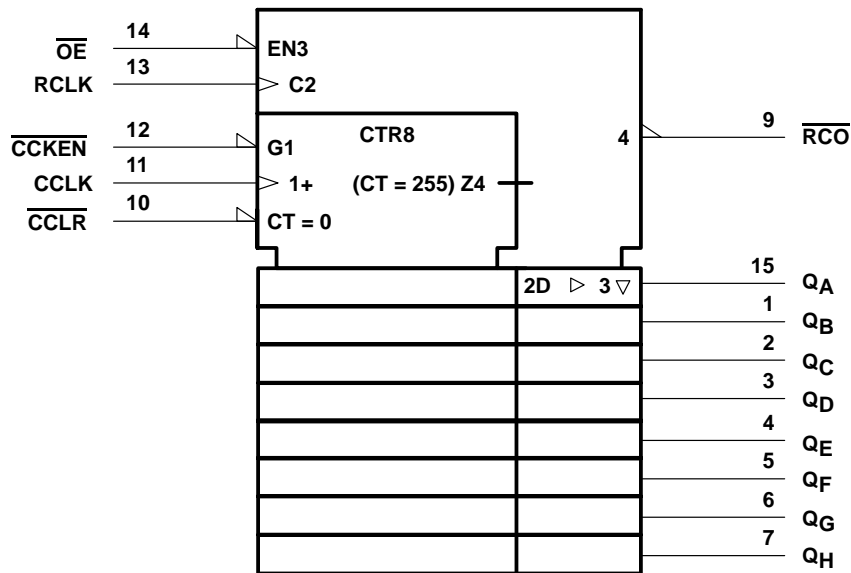
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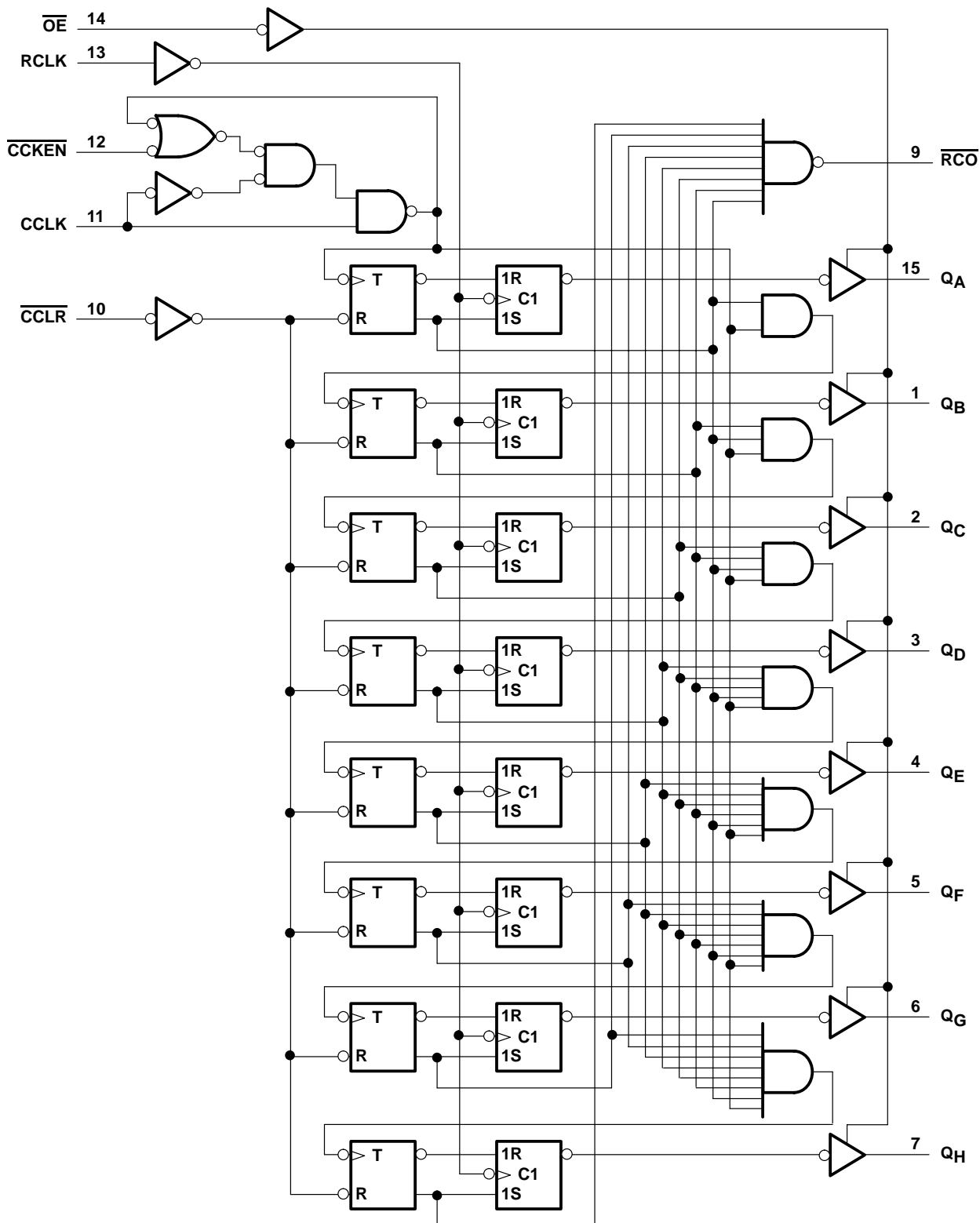
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DW, J, N, and W packages.

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SCLS039D – DECEMBER 1982 – REVISED MARCH 2001

logic diagram (positive logic)



Pin numbers shown are for the D, DW, J, N, and W packages.



SN54HC590A, SN74HC590A
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC590A		SN74HC590A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		4.5 V	\overline{RCO} , I _{OH} = -4 mA	3.98	4.3		3.7		3.84		
			Q _A -Q _H , I _{OH} = -6 mA	3.98	4.3		3.7		3.84		
		6 V	\overline{RCO} , I _{OH} = -5.2 mA	5.48	5.8		5.2		5.34		
			Q _A -Q _H , I _{OH} = -7.8 mA	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		V	
			4.5 V		0.001	0.1		0.1			
			6 V		0.001	0.1		0.1			
		4.5 V	\overline{RCO} , I _{OL} = 4 mA		0.17	0.26		0.4			0.33
			Q _A -Q _H , I _{OL} = 6 mA		0.17	0.26		0.4			0.33
		6 V	\overline{RCO} , I _{OL} = 5.2 mA		0.15	0.26		0.4			0.33
			Q _A -Q _H , I _{OL} = 7.8 mA		0.15	0.26		0.4			0.33
I _I	V _I = V _{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA	
I _{OZ}	V _O = V _{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V			8		160		80	μA	
C _i		2 V to 6 V		3	10		10		10	pF	

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS039D – DECEMBER 1982 – REVISED MARCH 2001

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC590A		SN74HC590A		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency	2 V	4		2.5		3.2		MHz	
		4.5 V	20		13		16			
		6 V	24		16		19			
t _w	Pulse duration	CCLK or RCLK high or low	2 V	125		200		155		ns
			4.5 V	25		38		31		
			6 V	21		32		26		
	$\overline{\text{CCLR}}$ low	2 V	100		150		125			
		4.5 V	20		30		25			
		6 V	17		26		21			
t _{su}	Setup time	$\overline{\text{CCKEN}}$ low before CCLK↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
	$\overline{\text{CCLR}}$ high (inactive) before CCLK↑	2 V	100		150		125			
		4.5 V	20		30		25			
		6 V	17		26		21			
	CCLK↑ before RCLK↑†	2 V	100		150		125			
		4.5 V	20		30		25			
		6 V	17		26		21			
t _h	Hold time	$\overline{\text{CCKEN}}$ low after CCLK↑	2 V	50		75		60		ns
			4.5 V	10		15		12		
			6 V	9		13		11		

† This setup time ensures that the register gets stable data from the counter outputs. The clocks may be tied together, in which case the register is one clock pulse behind the counter.



SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS
SCLS039D – DECEMBER 1982 – REVISED MARCH 2001

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
f_{\max}			2 V	4	8	2.5	MHz		
			4.5 V	20	35	13			
			6 V	24	40	16			
t_{pd}	CCLK \uparrow	\overline{RCO}	2 V	80	150	225	ns		
			4.5 V	20	31	45			
			6 V	15	26	38			
t_{PLH}	$\overline{CCLR}\downarrow$	\overline{RCO}	2 V	70	130	195	ns		
			4.5 V	18	28	39			
			6 V	14	23	33			
t_{pd}	RCLK \uparrow	Q	2 V	70	140	210	ns		
			4.5 V	18	31	42			
			6 V	14	25	36			
t_{en}	$\overline{OE}\downarrow$	Q	2 V	80	125	185	ns		
			4.5 V	20	30	37			
			6 V	15	28	31			
t_{dis}	$\overline{OE}\uparrow$	Q	2 V	80	125	185	ns		
			4.5 V	20	30	37			
			6 V	15	28	31			
t_t^*		\overline{RCO}	2 V	38	75	110	ns		
			4.5 V	8	15	22			
			6 V	6	13	19			
		Q	2 V	38	60	90			
			4.5 V	8	12	18			
			6 V	6	10	15			

* This parameter is not production tested for the SN54HC590A.

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS039D – DECEMBER 1982 – REVISED MARCH 2001

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74HC590A				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
f _{max}			2 V	4	8	3.2	MHz		
			4.5 V	20	35	16			
			6 V	24	40	19			
t _{pd}	CCLK↑	\overline{RCO}	2 V		80	150	190	ns	
			4.5 V		20	30	38		
			6 V		15	26	33		
t _{PLH}	\overline{CCLR} ↓	\overline{RCO}	2 V		70	130	165	ns	
			4.5 V		18	26	33		
			6 V		14	22	28		
t _{pd}	RCLK↑	Q	2 V		70	140	175	ns	
			4.5 V		18	28	35		
			6 V		14	24	30		
t _{en}	\overline{OE} ↓	Q	2 V		80	125	155	ns	
			4.5 V		20	25	31		
			6 V		15	21	26		
t _{dis}	\overline{OE} ↑	Q	2 V		80	125	155	ns	
			4.5 V		20	25	31		
			6 V		15	21	26		
t _t		\overline{RCO}	2 V		38	75	95	ns	
			4.5 V		8	15	19		
			6 V		6	13	16		
		Q	2 V		38	60	75		
			4.5 V		8	12	15		
			6 V		6	10	13		



SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS
 SCLS039D – DECEMBER 1982 – REVISED MARCH 2001

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
t_{pd}	RCLK \uparrow	Q	2 V	100	300	447	ns		
			4.5 V	24	60	90			
			6 V	20	51	77			
t_{en}	\overline{OE}	Q	2 V	90	200	300	ns		
			4.5 V	23	40	60			
			6 V	19	34	51			
t_t^*		Q	2 V	45	210	315	ns		
			4.5 V	17	42	63			
			6 V	13	36	53			

* This parameter is not production tested for the SN54HC590A.

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
t_{pd}	RCLK \uparrow	Q	2 V	100	300	380	ns		
			4.5 V	24	60	76			
			6 V	20	51	65			
t_{en}	\overline{OE}	Q	2 V	90	200	250	ns		
			4.5 V	23	40	50			
			6 V	19	34	43			
t_t		Q	2 V	45	210	265	ns		
			4.5 V	17	42	53			
			6 V	13	36	45			

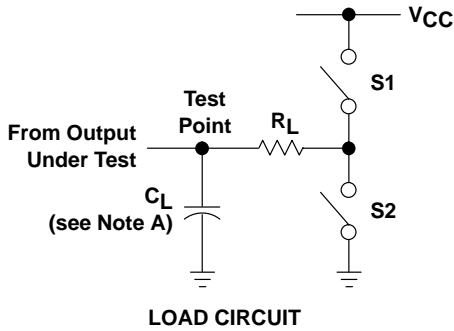
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	250	pF

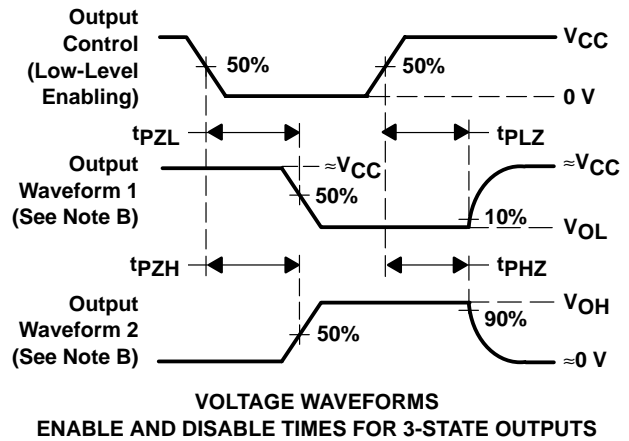
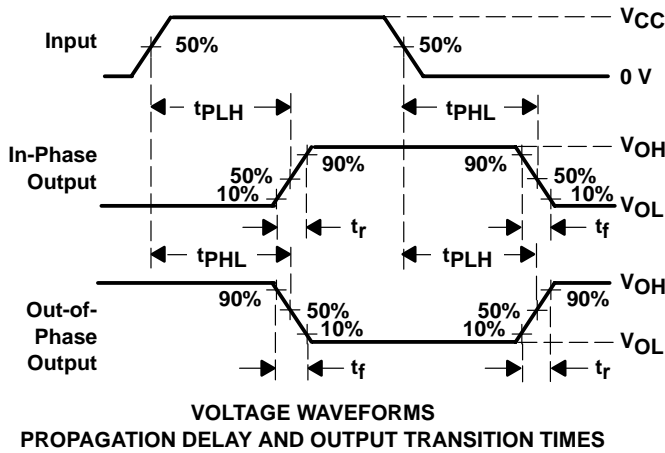
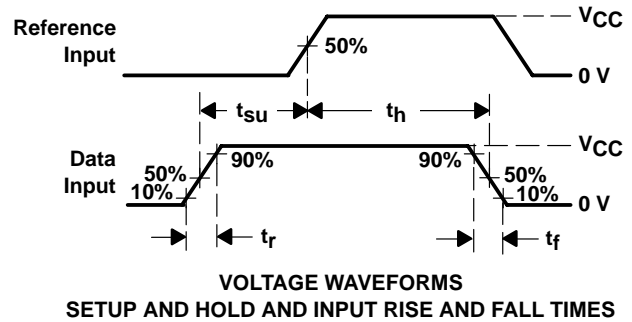
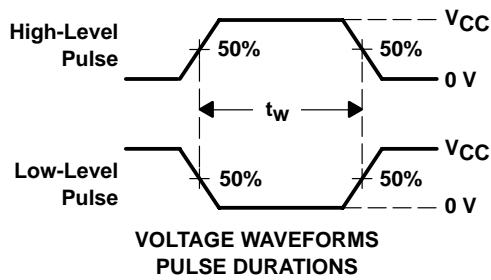
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PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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