

ULN2003B High-Voltage, High-Current Darlington Transistor Array

1 Features

- Greater Than 4x Reduction in Output Leakage (I_{CEX}) over ULN2003A
- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

2 Applications

- Relay Drivers
- Hammer Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

3 Description

The ULN2003B is a high-voltage, high-current Darlington transistor array. This device consists of seven NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability.

The ULN2003B has a 2.7-k Ω series base resistor for each Darlington pair for operation directly with TTL or CMOS devices.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ULN2003B	PDIP (16)	19.30 mm x 6.35 mm
	SOIC (16)	9.90 mm x 3.91 mm
	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

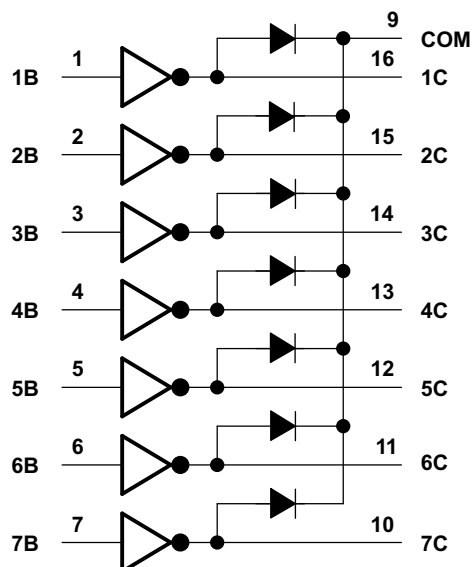


Table of Contents

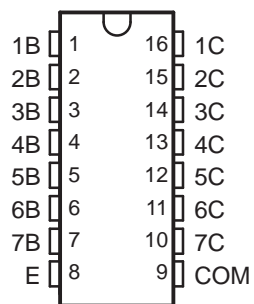
1	Features	1	9	Detailed Description	9
2	Applications	1	9.1	Overview	9
3	Description	1	9.2	Functional Block Diagram	9
4	Simplified Schematic	1	9.3	Feature Description	9
5	Revision History	2	9.4	Device Functional Modes	10
6	Pin Configuration and Functions	3	10	Application and Implementation	10
7	Specifications	4	10.1	Application Information	10
7.1	Absolute Maximum Ratings	4	10.2	Typical Application	10
7.2	Handling Ratings	4	11	Power Supply Recommendations	12
7.3	Recommended Operating Conditions	4	12	Layout	12
7.4	Thermal Information	4	12.1	Layout Guidelines	12
7.5	Electrical Characteristics, $T_A = 25^\circ\text{C}$	5	12.2	Layout Example	12
7.6	Electrical Characteristics, $T_A = -40^\circ\text{C}$ to 105°C	5	13	Device and Documentation Support	13
7.7	Switching Characteristics, $T_A = 25^\circ\text{C}$	5	13.1	Trademarks	13
7.8	Switching Characteristics, $T_A = -40^\circ\text{C}$ to 105°C	5	13.2	Electrostatic Discharge Caution	13
7.9	Typical Characteristics	6	13.3	Glossary	13
7.10	Thermal Information	7	14	Mechanical, Packaging, and Orderable Information	13
8	Parameter Measurement Information	8			

5 Revision History

Changes from Original (June 2014) to Revision A	Page
• Initial release of full version.	1

6 Pin Configuration and Functions

**D, N, OR PW PACKAGE
(TOP VIEW)**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
<1:7>B	1 - 7	Input	Channel 1 through 7 darlington base input
<1:7>C	16 - 10	Output	Channel 1 through 7 darlington collector output
E	7	–	Common Emmitter shared by all channels (typically tied to ground)
COM	8	Input/Output	Common cathode node for flyback diodes (required for inductive loads)

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

at 25°C free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Collector-emitter voltage		50	V
	Clamp diode reverse voltage ⁽²⁾		50	V
V _I	Input voltage ⁽²⁾		30	V
	Peak collector current ⁽³⁾⁽⁴⁾		500	mA
I _{OK}	Output clamp current		500	mA
	Total emitter-terminal current		-2.5	A
T _A	Operating free-air temperature range	-40	105	°C
θ _{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	D package	81	°C/W
		N package	49.7	
		PW package	105	
T _J	Operating virtual junction temperature		150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
- (3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	-65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _I		0	5	V
V _{CC}		0	50	V
T _J	Junction Temperature	-40	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	ULN2003B		UNIT	
	PW	D		
	16 PINS	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	105.4	81.2	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	32.9	40.3	
R _{θJB}	Junction-to-board thermal resistance	51.3	38.9	
ψ _{JT}	Junction-to-top characterization parameter	2.1	10.9	
ψ _{JB}	Junction-to-board characterization parameter	50.6	38.7	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS		ULN2003B			UNIT
				MIN	TYP	MAX	
$V_{I(on)}$ On-state input voltage	Figure 12	$V_{CE} = 2\text{ V}$	$I_C = 200\text{ mA}$			2.4	V
			$I_C = 250\text{ mA}$			2.7	
			$I_C = 300\text{ mA}$			3	
$V_{CE(sat)}$ Collector-emitter saturation voltage	Figure 11		$I_I = 250\ \mu\text{A}$, $I_C = 100\text{ mA}$		0.9	1.1	V
			$I_I = 350\ \mu\text{A}$, $I_C = 200\text{ mA}$		1	1.3	
			$I_I = 500\ \mu\text{A}$, $I_C = 350\text{ mA}$		1.2	1.6	
I_{CEX} Collector cutoff current	Figure 8	$V_{CE} = 50\text{ V}$, $I_I = 0$				10	μA
V_F Clamp forward voltage	Figure 14	$I_F = 350\text{ mA}$			1.7	2	V
$I_{I(off)}$ Off-state input current	Figure 9	$V_{CE} = 50\text{ V}$, $I_C = 500\ \mu\text{A}$		50	65		μA
I_I Input current	Figure 10	$V_I = 3.85\text{ V}$		0.93	1.35		mA
I_R Clamp reverse current	Figure 13	$V_R = 50\text{ V}$				50	μA
C_i Input capacitance		$V_I = 0$, $f = 1\text{ MHz}$		15	25		pF

7.6 Electrical Characteristics, $T_A = -40^\circ\text{C}$ to 105°C

PARAMETER	TEST FIGURE	TEST CONDITIONS		ULN2003B			UNIT
				MIN	TYP	MAX	
$V_{I(on)}$ On-state input voltage	Figure 12	$V_{CE} = 2\text{ V}$	$I_C = 200\text{ mA}$			2.7	V
			$I_C = 250\text{ mA}$			2.9	
			$I_C = 300\text{ mA}$			3	
$V_{CE(sat)}$ Collector-emitter saturation voltage	Figure 11		$I_I = 250\ \mu\text{A}$, $I_C = 100\text{ mA}$		0.9	1.2	V
			$I_I = 350\ \mu\text{A}$, $I_C = 200\text{ mA}$		1	1.4	
			$I_I = 500\ \mu\text{A}$, $I_C = 350\text{ mA}$		1.2	1.7	
I_{CEX} Collector cutoff current	Figure 8	$V_{CE} = 50\text{ V}$, $I_I = 0$				20	μA
V_F Clamp forward voltage	Figure 14	$I_F = 350\text{ mA}$			1.7	2.2	V
$I_{I(off)}$ Off-state input current	Figure 9	$V_{CE} = 50\text{ V}$, $I_C = 500\ \mu\text{A}$		30	65		μA
I_I Input current	Figure 10	$V_I = 3.85\text{ V}$		0.93	1.35		mA
I_R Clamp reverse current	Figure 13	$V_R = 50\text{ V}$				100	μA
C_i Input capacitance		$V_I = 0$, $f = 1\text{ MHz}$		15	25		pF

7.7 Switching Characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output			0.25	1	μs
t_{PHL} Propagation delay time, high- to low-level output			0.25	1	μs
V_{OH} High-level output voltage after switching	$V_S = 50\text{ V}$, $I_O \approx 300\text{ mA}$	$V_S - 20$			mV

7.8 Switching Characteristics, $T_A = -40^\circ\text{C}$ to 105°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output			1	10	μs
t_{PHL} Propagation delay time, high- to low-level output			1	10	μs
V_{OH} High-level output voltage after switching	$V_S = 50\text{ V}$, $I_O \approx 300\text{ mA}$	$V_S - 50$			mV

7.9 Typical Characteristics

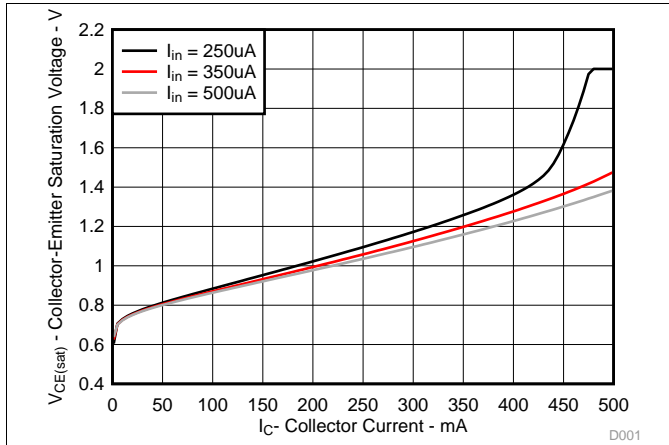


Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

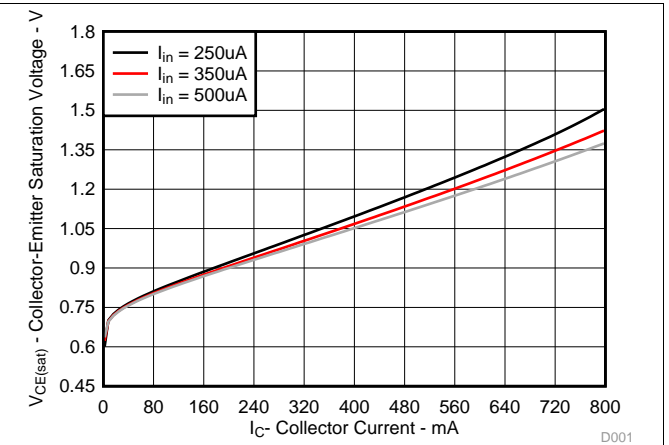


Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlington in Parallel)

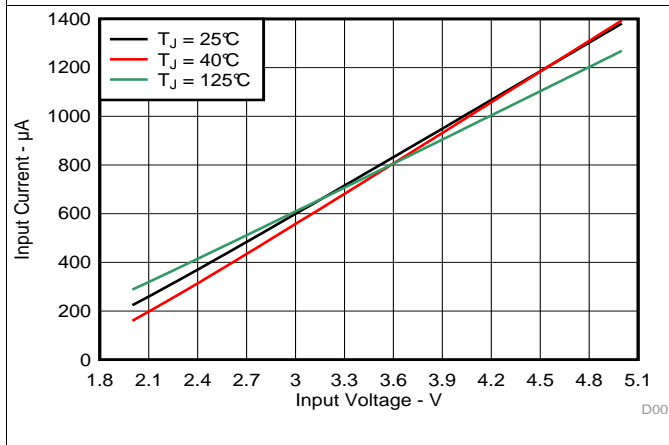


Figure 3. Input Current vs Input Voltage

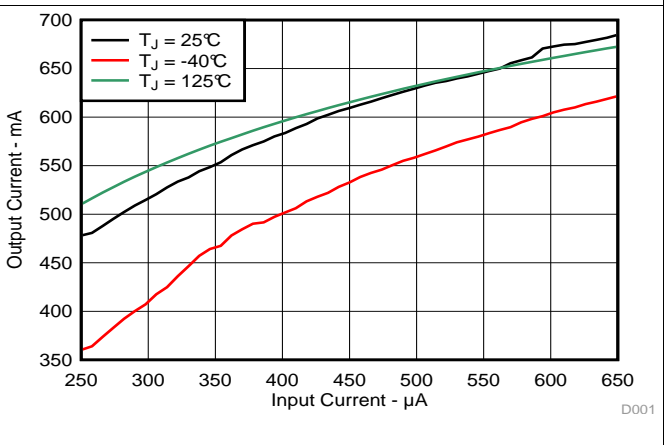


Figure 4. Output Current vs Input Current

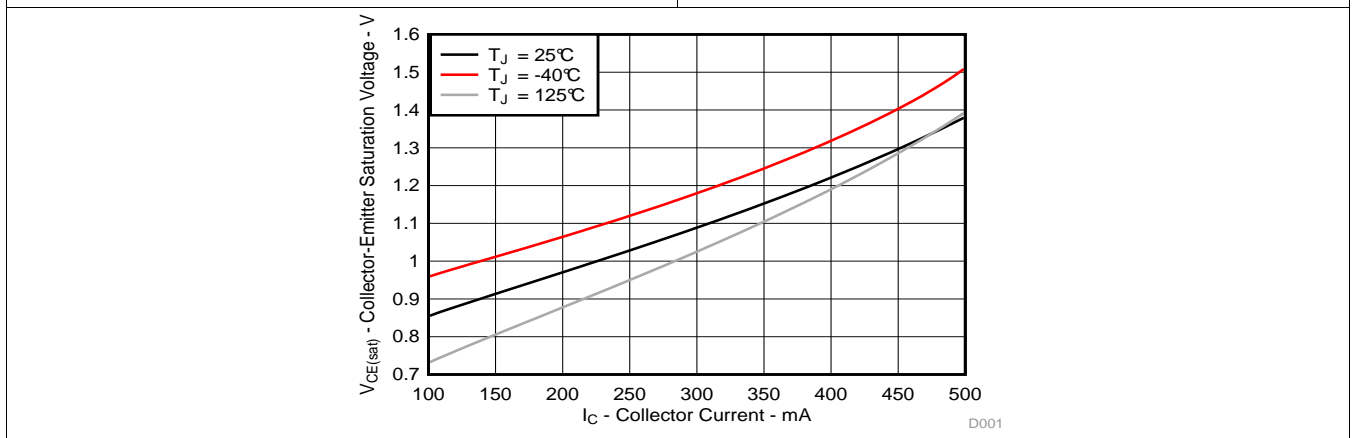
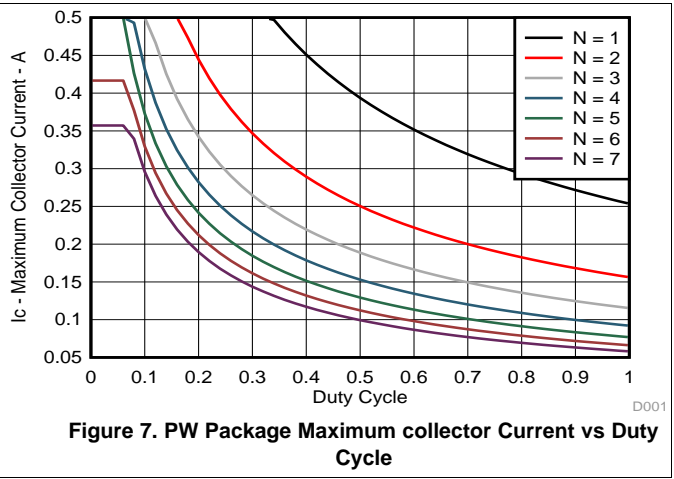
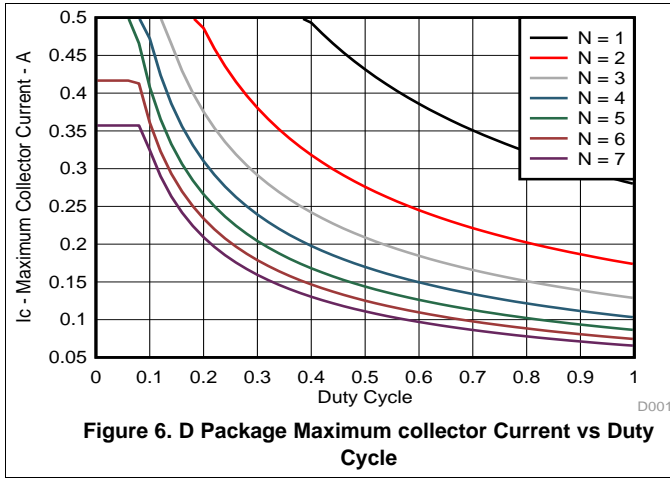


Figure 5. Collector-Emitter Saturation Voltage vs Collector Current

7.10 Thermal Information



8 Parameter Measurement Information

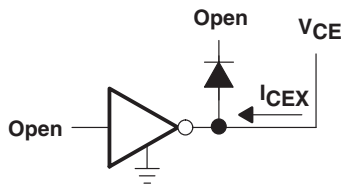


Figure 8. I_{CEX} Test Circuit

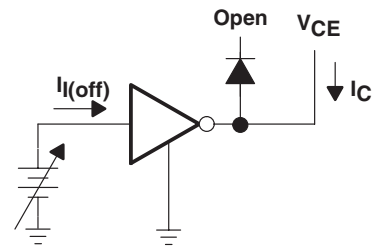


Figure 9. $I_{I(off)}$ Test Circuit

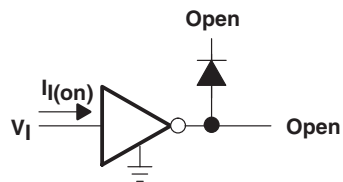


Figure 10. I_I Test Circuit

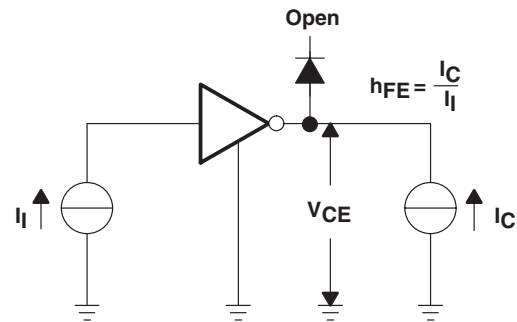


Figure 11. h_{fe} , $V_{CE(sat)}$ Test Circuit

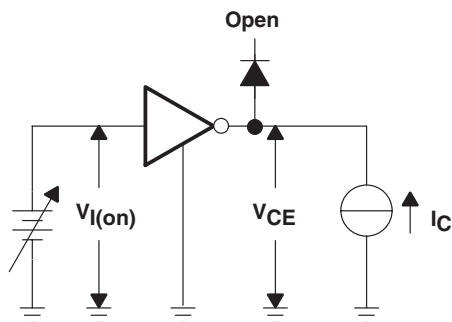


Figure 12. $V_{I(on)}$ Test Circuit

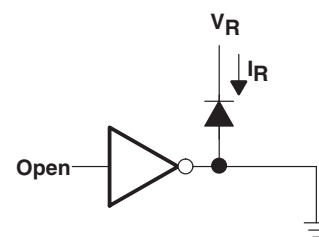


Figure 13. I_R Test Circuit

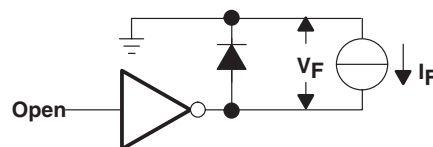


Figure 14. V_F Test Circuit

9 Detailed Description

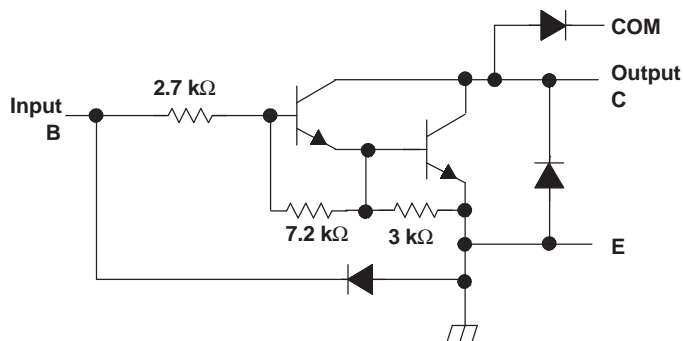
9.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its integration of 7 Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2003B comprises seven high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2003B has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0 V or 3.3 V. The ULN2003B offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to 105°C).

9.2 Functional Block Diagram



All resistor values shown are nominal.

Figure 15. Schematic (Each Comparator)

9.3 Feature Description

Each channel of ULN2003B consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high current gain (β_2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current via the 2.7 k Ω resistor connected between the input and base of the pre-driver Darlington NPN. The 7.2 k Ω & 3.0 k Ω resistors connected between the base and emitter of each respective NPN act as pull-downs and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply via the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diode are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

9.4 Device Functional Modes

9.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2003B is able to drive inductive loads and suppress the kick-back voltage via the internal free wheeling diodes.

9.4.2 Resistive Load Drive

When driving a resistive load, a pull-up resistor is needed in order for ULN2003B to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

ULN2003B will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2003B, driving inductive loads. This includes motors, solenoids & relays. Each load type can be modeled by what's seen in [Figure 16](#).

10.2 Typical Application

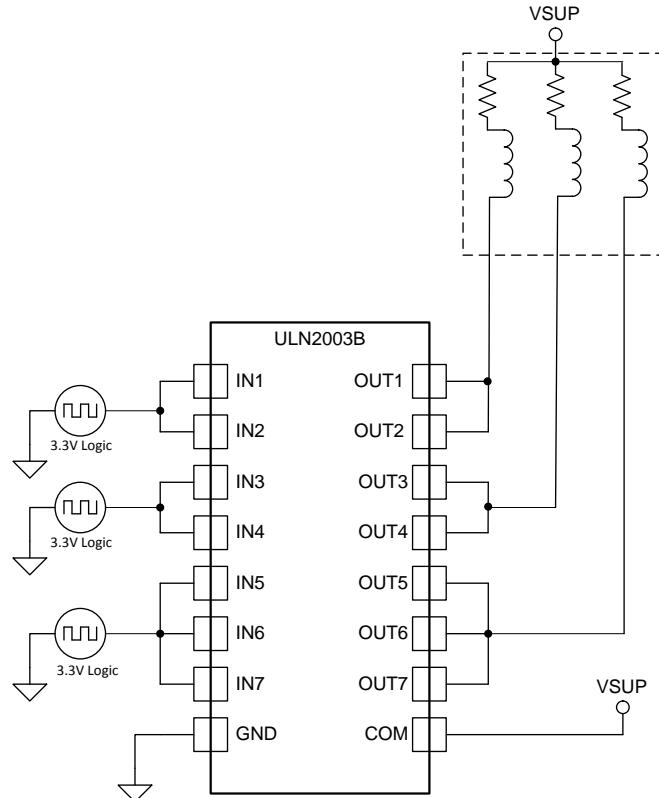


Figure 16. ULN2003B as Inductive Load Driver

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO Voltage	3.3 V or 5.0 V
Coil Supply Voltage	12 V to 48 V
Number of Channels	7
Output Current (R _{COIL})	20 mA to 300 mA per channel
Duty Cycle	100%

10.2.2 Detailed Design Procedure

When using ULN2003B in a coil driving application, determine the following:

- Input Voltage Range
- Temperature Range
- Output & Drive Current
- Power Dissipation

10.2.2.1 Drive Current

The coil current is determined by the coil voltage (V_{SUP}), coil resistance & output low voltage (V_{OL} or V_{CE(SAT)}).

$$I_{\text{COIL}} = (V_{\text{SUP}} - V_{\text{CE(SAT)}}) / R_{\text{COIL}} \quad (1)$$

10.2.2.2 Output Low Voltage

The output low voltage (V_{OL}) is the same thing as V_{CE(SAT)} and can be determined by, [Figure 1](#), [Figure 2](#), or [Figure 5](#).

10.2.2.3 Power Dissipation & Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by [Figure 6](#) or [Figure 7](#).

For a more accurate determination of number of coils possible, use the below equation to calculate ULN2003B on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^N V_{\text{OL}i} \times I_{\text{Li}}$$

Where:

N is the number of channels active together.

V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as V_{CE(SAT)} (2)

In order to guarantee reliability of ULN2003B and the system the on-chip power dissipation must be lower than or equal to the maximum allowable power dissipation (PD_(MAX)) dictated by below equation [Equation 3](#).

$$PD_{(\text{MAX})} = \frac{(T_{\text{J(MAX)}} - T_{\text{A}})}{\theta_{\text{JA}}}$$

Where:

T_{J(MAX)} is the target maximum junction temperature.

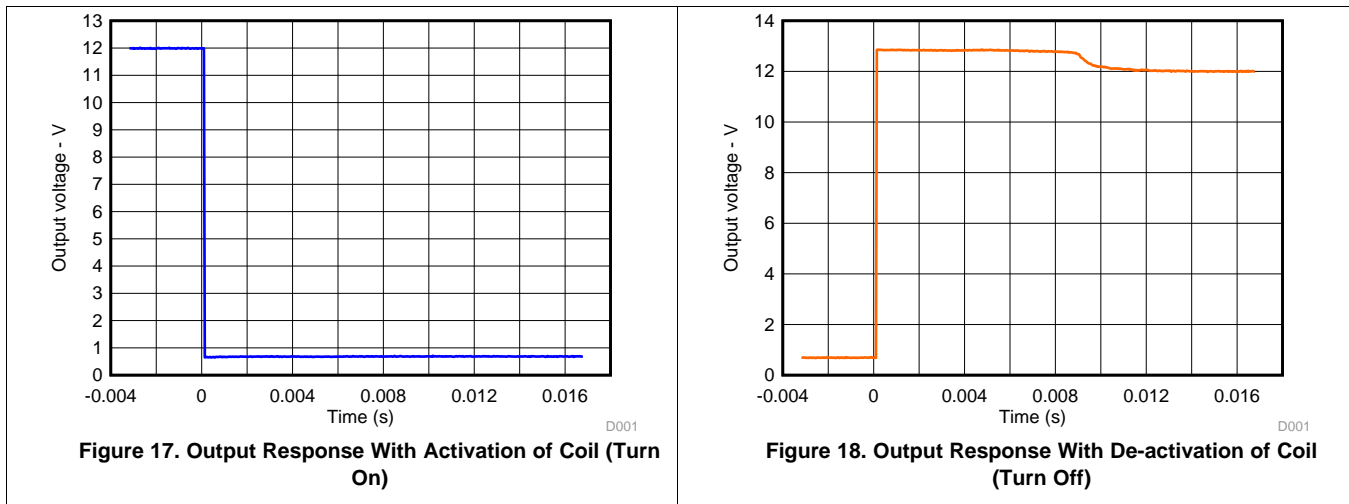
T_A is the operating ambient temperature.

θ_{JA} is the package junction to ambient thermal resistance. (3)

It is recommended to limit ULN2003B IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

10.2.3 Application Curves

The following curves were generated with ULN2003B driving an OMRON G5NB relay – $V_{in} = 5.0V$; $V_{sup} = 12 V$ & $R_{COIL} = 2.8 k\Omega$



11 Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, it is very important to make sure that the output voltage does not heavily exceed the COM pin voltage. This will heavily forward bias the fly-back diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or over-heating the part.

12 Layout

12.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive UNL2003B. Care must be taken to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive whatever high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

12.2 Layout Example

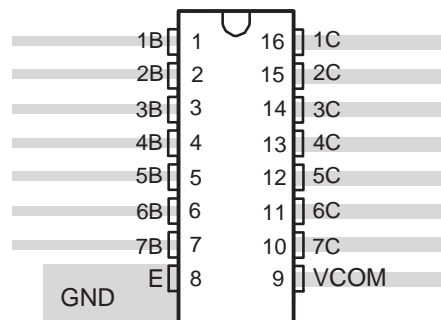


Figure 19. Package Layout

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2003BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 105	ULN2003B	Samples
ULN2003BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 105	ULN2003BN	Samples
ULN2003BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 105	UN2003B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2003BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003BDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ULN2003BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2003BDR	SOIC	D	16	2500	367.0	367.0	38.0
ULN2003BDR	SOIC	D	16	2500	364.0	364.0	27.0
ULN2003BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
ULN2003BPWR	TSSOP	PW	16	2000	364.0	364.0	27.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

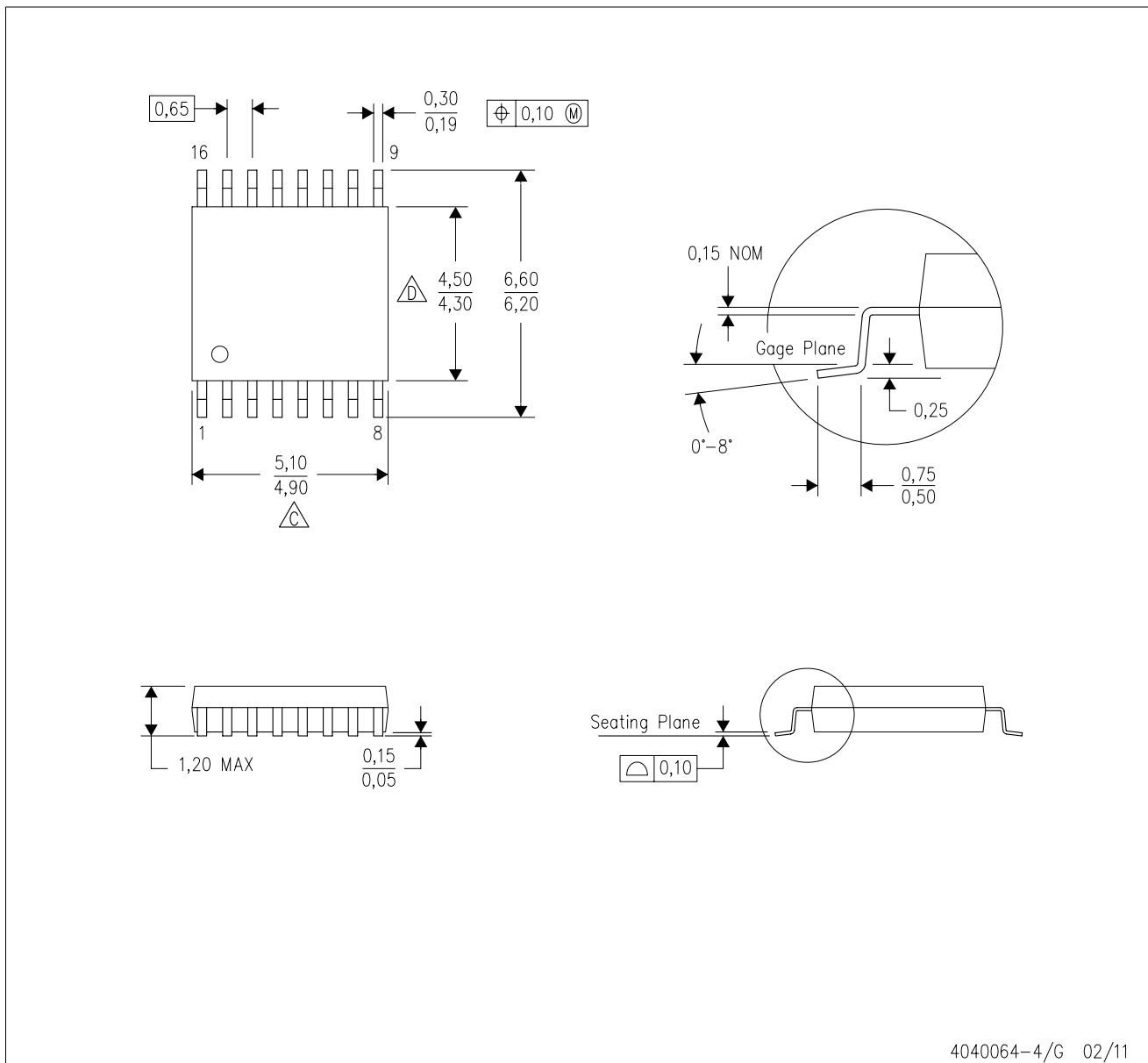
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

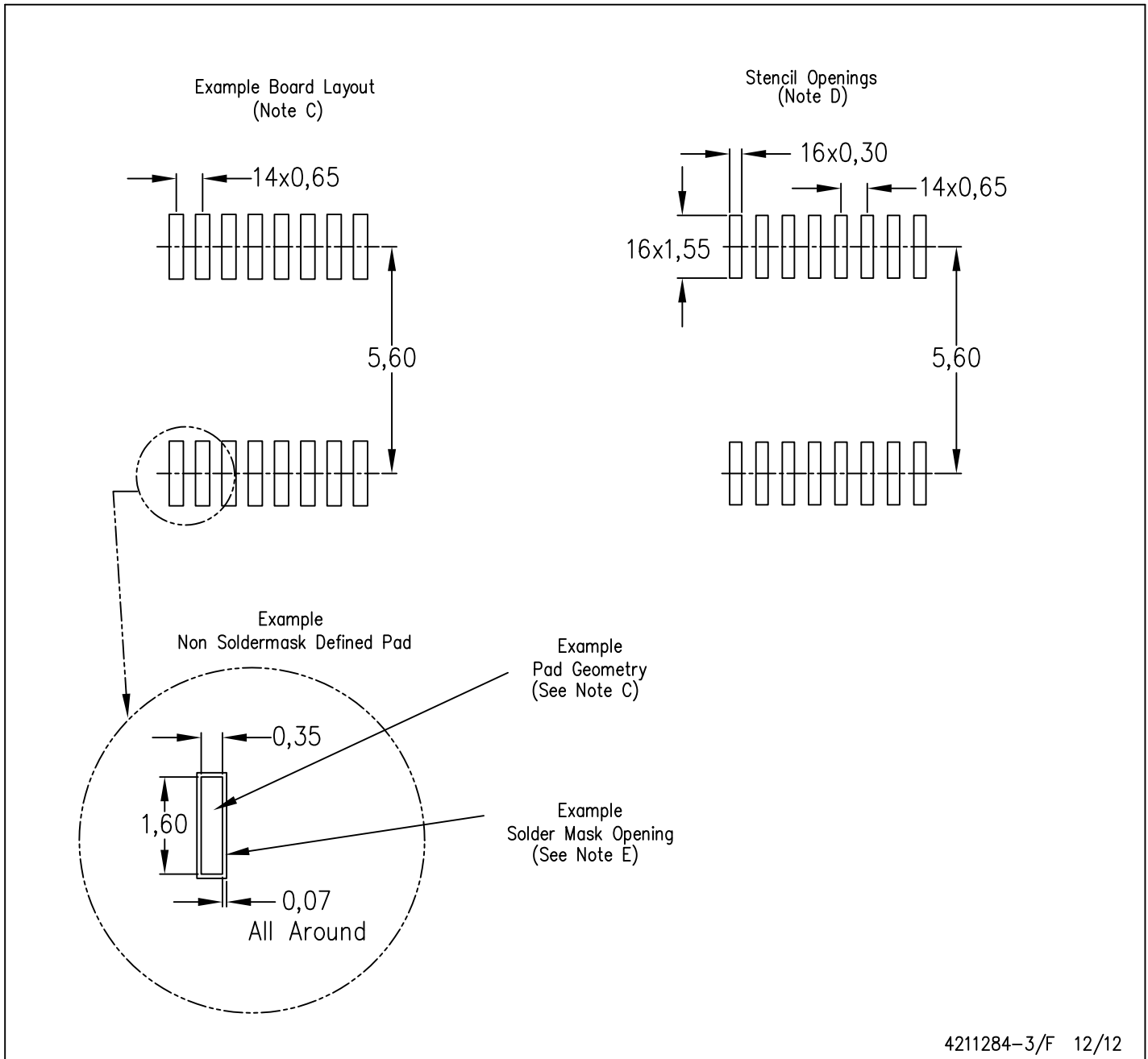


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com