N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0135 @ V_{GS} = 10 V	10
	0.020 @ V_{GS} = 4.5 V	8

FEATURES

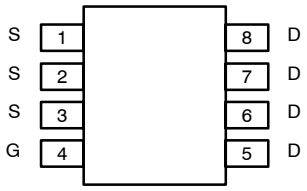
- TrenchFET® Power MOSFET
- 100% R_g Tested

APPLICATIONS

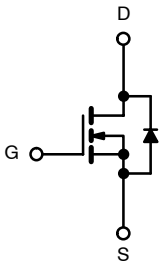
- Battery Switch
- Load Switch

Pb-free Available

SO-8



Top View



N-Channel MOSFET

Ordering Information: Si4410BDY
Si4410BDY—T1 (with Tape and Reel)
Si4410BDY—E3 (Lead (Pb)-Free)
Si4410BDY-T1—E3 (Lead (Pb)-Free with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	10	7.5	A
	T_A = 70°C		8	6	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	50		
Continuous Source Current (Diode Conduction)[a]		I_S	2.3	1.26	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	1.4	W
	T_A = 70°C		1.6	0.9	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	40	50	°C/W
	Steady State		70	90	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	25	30	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

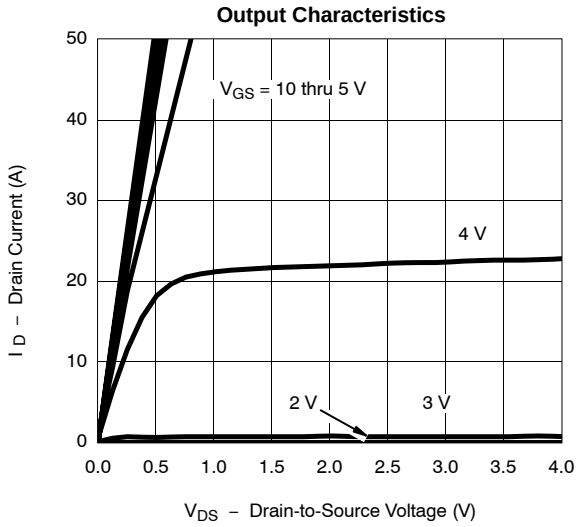
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

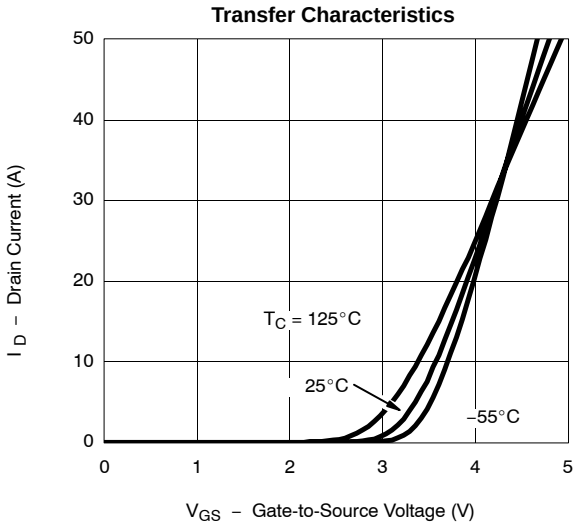
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	μA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A		0.011	0.0135	Ω
		V_{GS} = 4.5 V, I_D = 5 A		0.0165	0.020	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 10 A		25		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.3 A, V_{GS} = 0 V		0.76	1.1	V
Dynamic[b]						
Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 5 V, I_D = 10 A		13	20	nC
Total Gate Charge	Q_{gt}	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 10 A		25	40	
Gate-Source Charge	Q_{gs}			5.5		
Gate-Drain Charge	Q_{gd}			3.7		
Gate Resistance	R_g	f = 1 MHz	0.5	1.6	2.7	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		10	15	ns
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.3 A, di/dt = 100 A/μs		35	70	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

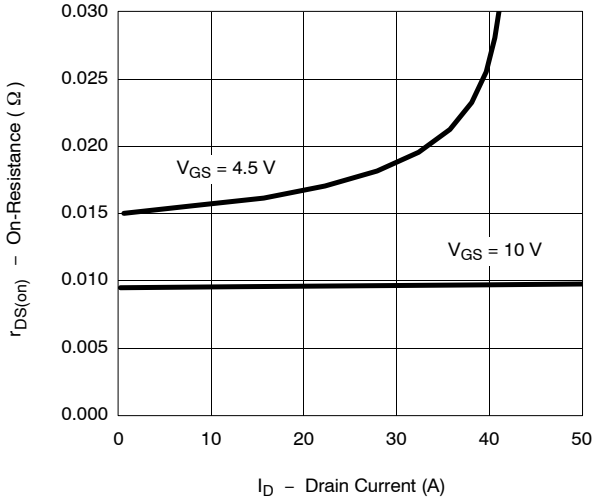
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



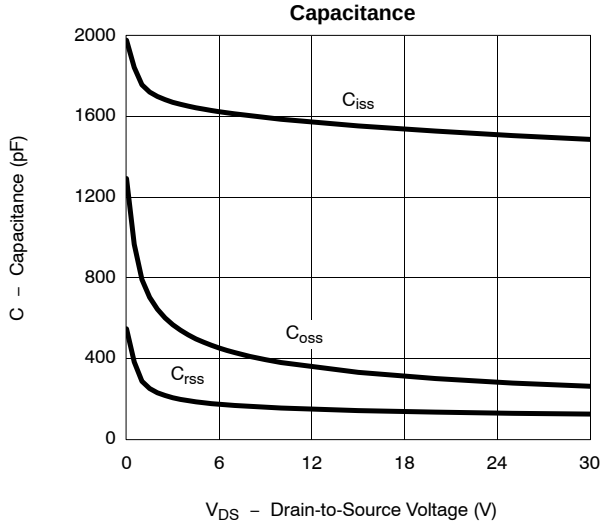


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

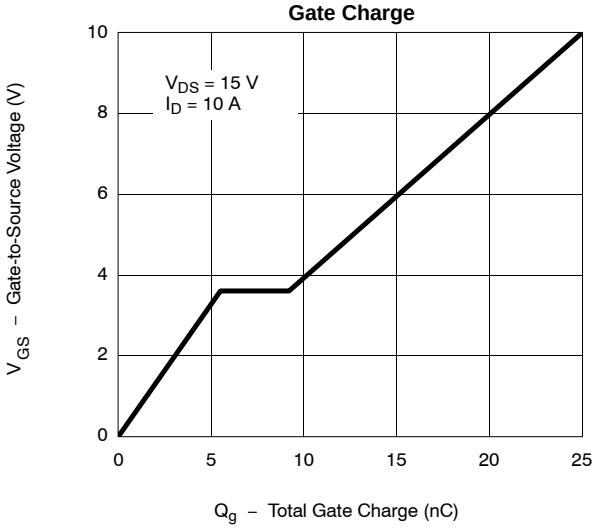
On-Resistance vs. Drain Current



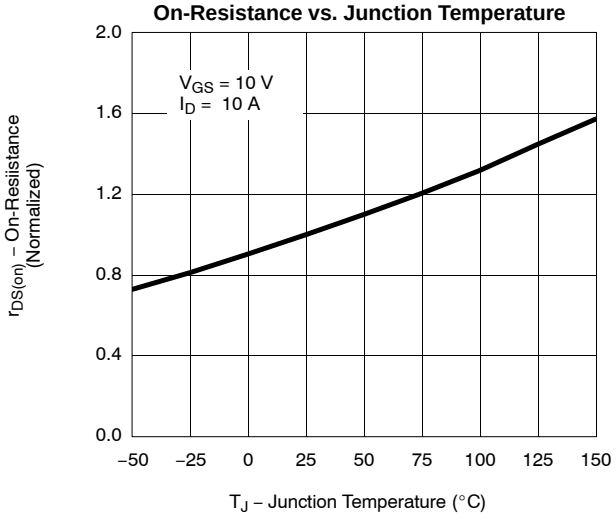
Capacitance



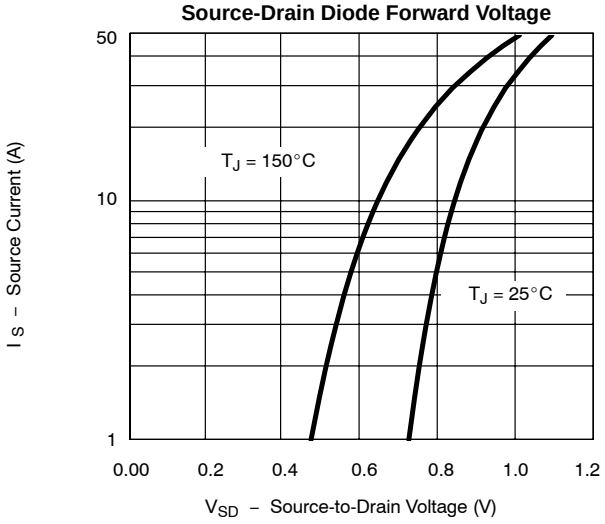
Gate Charge



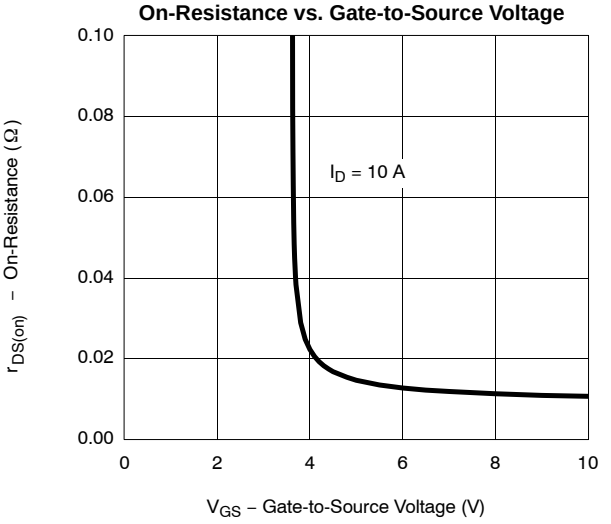
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

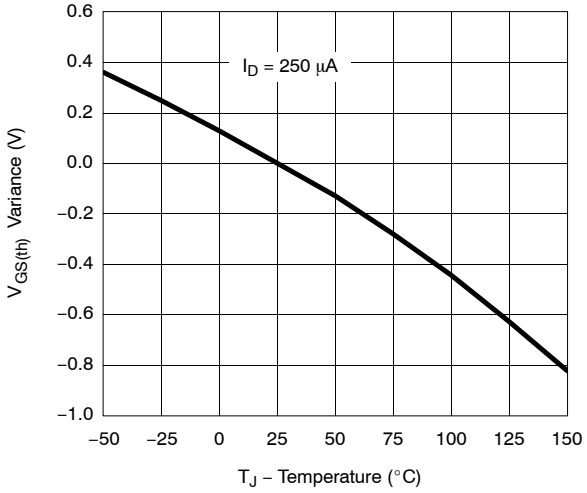


On-Resistance vs. Gate-to-Source Voltage

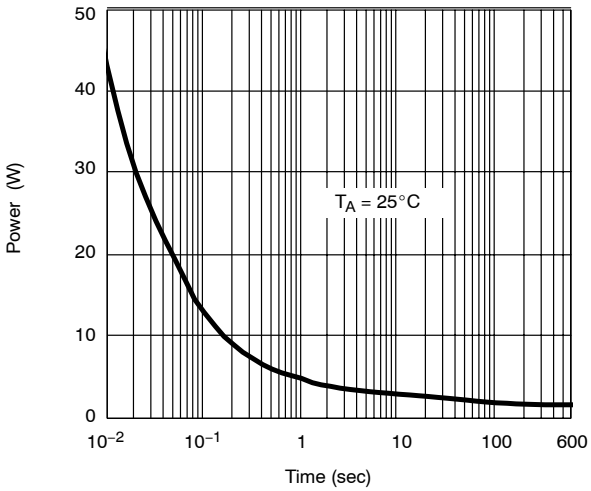


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

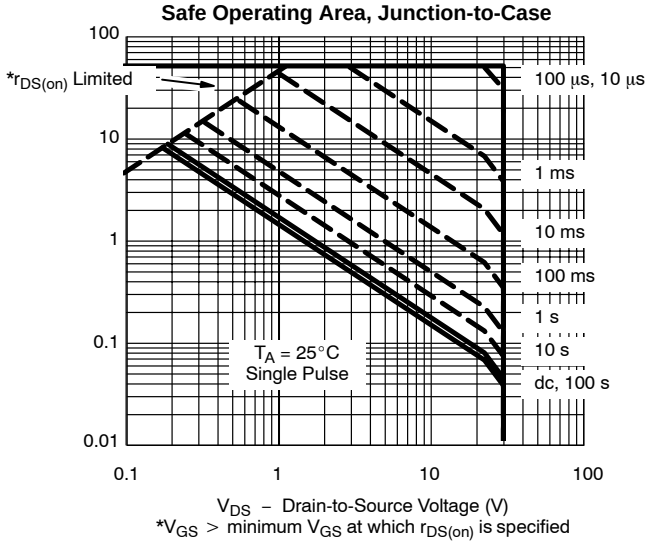
Threshold Voltage



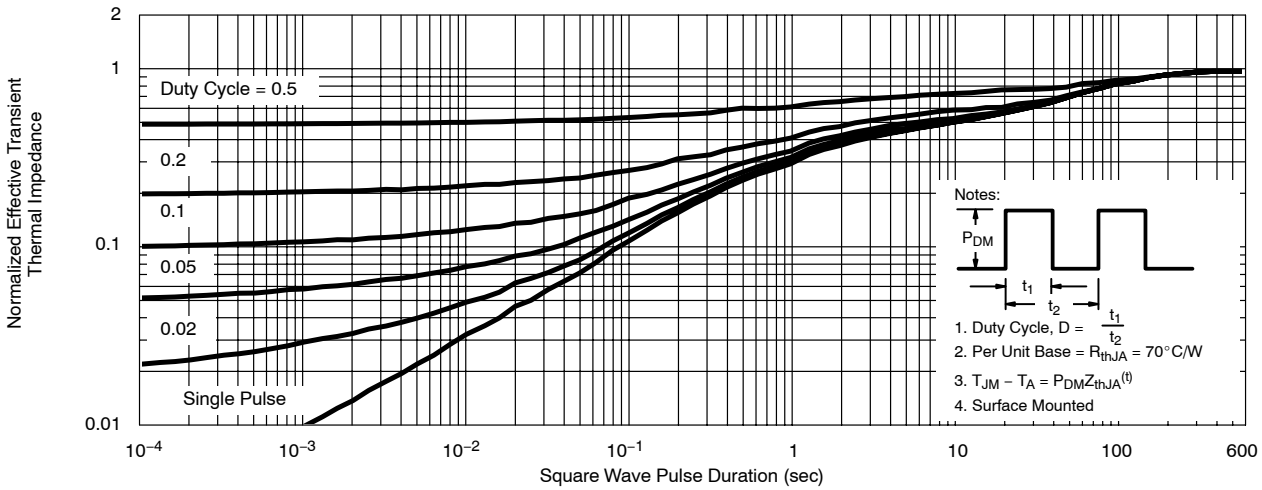
Single Pulse Power



Safe Operating Area, Junction-to-Case



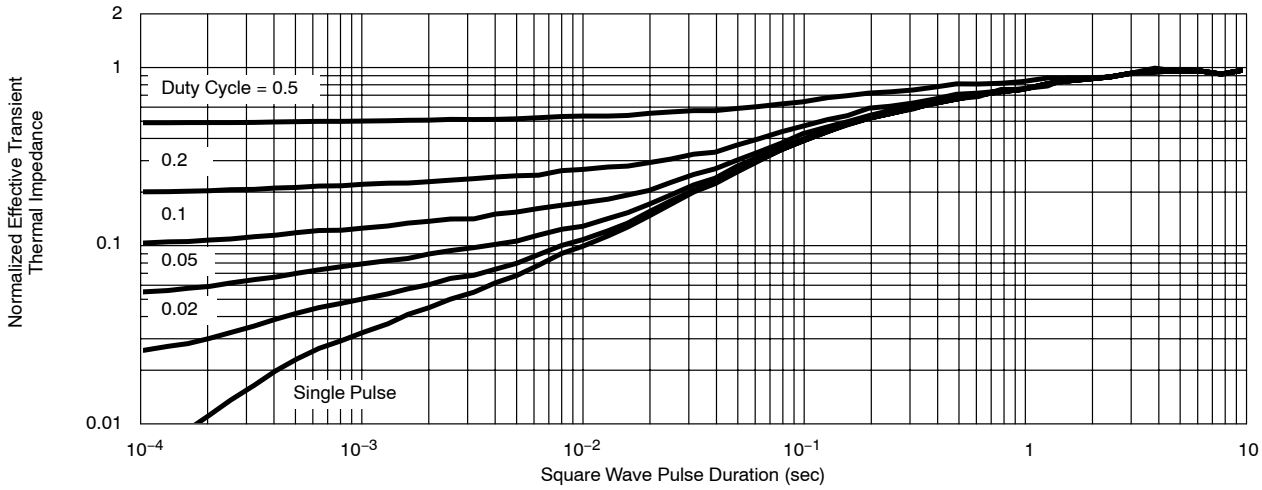
Normalized Thermal Transient Impedance, Junction-to-Ambient



Document Number: 72211
S-50366—Rev. C, 28-Feb-05

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Foot



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72211.